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0.3V Bulk-Driven Current Conveyor

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ABSTRACT This paper presents the design and the experimental results of a sub 0.5 V bulk-driven (BD) current conveyor (CCII) using 0.18 μm TSMC CMOS technology with a total chip area of 0.0134 mm^2. All transistors are biased in the subthreshold region for low-voltage low-power operation and the input transistors are controlled from their bulk terminals for rail-to-rail input voltage range. The circuit is designed to work with voltage supply (V_{DD} = 0.3V), which is much lower than the threshold voltage of the MOS transistor (V_{TH} =0.5V) while consuming 19 nW of power. The measurement results confirm the proper function of the proposed circuit.

INDEX TERMS Bulk-driven, low-voltage, low-power, sub 0.5-V circuits.

I. INTRODUCTION

Extremely low-voltage (LV) and low-power (LP) CMOS circuits have found a number of applications in contemporary portable and implantable electronic systems. In the last decades, various circuit techniques have been developed to overcome the design constraints associated with LV operation [1]. One of the techniques which attracted considerable attention in recent years depends on the application of subthreshold-biased bulk-driven (BD) MOS transistors, which allows designing circuits supplied with sub 0.5 V supply and rail-to-rail signal swing [2], [3].

The second generation current-conveyor (CCII) is a useful current-mode building block which has found a number of applications in low-voltage systems [4]–[11]. In the last years several low-voltage low-power CCIIs have been presented in the literature, for instance a CCII based on bulk-driven folded cascode OTA with ± 0.4 V voltage supply and 64 μW power consumption has been presented in [7], a CCII based on floating-gate folded cascode OTA with ± 0.5 V voltage supply and 10 μW power consumption has been presented in [8], a CCII based on bulk-driven voltage follower with 0.5 V voltage supply and 30 μW power consumption has been presented in [9], a gate-driven CCII using adaptive biasing technique with ±0.75 V voltage supply and 150 nW power consumption has been presented in [10], a gate-driven subthreshold CCII with 0.4 V voltage supply and 1.8 μ W power consumption has been presented in [11]. The performance of the all above mentioned LV LP CCIIs were confirmed by simulation only.

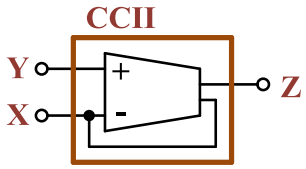

FIGURE 1. CCII based on two outputs op-amp.

This paper presents a new solution for a LV/LP BD CCII that can operate from V_{DD} of 0.3 V, while consuming only 19 nW of power and offering a rail-to-rail signal swing at the same time. The ultra-low V_{DD} has been achieved thanks to the use of a BD non-tailed differential amplifier. Moreover, the structure shows an improved 3-dB bandwidth of a current gain and can operate without any compensation capacitance, even for large loading capacitances, while offering precise voltage and current gain values at the same time.

The rest of the paper is organized as follows. In section II, the structure of the proposed bulk-driven CCII is described. Section III presents the experimental results. Finally, the conclusions are given in section IV.

II. BULK-DRIVEN CCII

The proposed positive CCII, as shown in Fig. 1, is based on two outputs op-amp operating in unity-gain feedback configuration that ensure $V_Y = V_X$ and $I_Z = I_X$.

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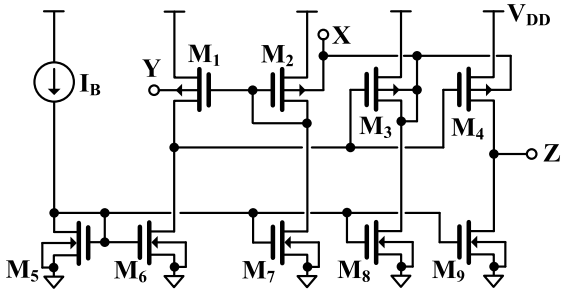

FIGURE 2. CMOS schematic of BD-CCII.

The schematic of the proposed CCII is shown in Fig. 2. The circuit consists of a precise Y-X voltage follower (M_1-M_3, M_5-M_8) and an additional current repetition circuit (M_4, M_9), that creates the unity-gain current amplifier and the Z output of the conveyor. The voltage follower was first proposed and validated by simulations in [12]. Let us remind briefly its principle of operation. The circuit can be considered as a simple two-stage op-amp operating in a unity-gain feedback configuration.

Transistors M_1 and M_2 form a simple non-tailed differential amplifier loaded by the current sinks M_6 and M_7. The second stage of the internal op-amp is created by the transistor M_3 loaded by the current sink M_8. The bulk terminals of M_2 and M_3 are shorted together and connected to the output of the op-amp. Such a connection closes a negative feedback loop, thus creating a unity-gain voltage buffer. Note, that shorting together the bulk terminals of M_2 and M_3 ensures that the threshold voltages of the two transistors are changing in the same way with the input signal. This improves the accuracy of the voltage gain. Without this connection the internal op-amp would have poor CMRR performance, which would affect the accuracy of the voltage gain of the resulting voltage follower, causing its value to be greater than unity. It is worth mentioning that the CCII can be simply extended to have multiple outputs with both polarities by using the cross-coupled current mirror technique.

The minimum supply voltage of the CCII can be expressed as follows:

$$V_{DDmin} = \max(V_{SG2} + V_{DSsat7};\ V_{SG3,4} + V_{DS6}) \tag{1}$$

where V_{DSsat} is the saturation voltage of an MOS transistor. Assuming $V_{SG2,3,4} = V_{DSsat}$ in a weak inversion region the minimum V_{DD} can be as low as $2V_{DSsat}$ (ca. 200 mV). In practical realizations however, the minimum V_{DD} has to be slightly increased due to the process/temperature variations and signal swing. Nevertheless, the minimum V_{DD} is around 1/3 lower as compared to traditional solutions based on long tail differential pairs.

Neglecting the parasitic pole associated with the drain/gate node of M_2:

$$\omega_p \approx -\frac{g_{m2}}{C_{gs1} + C_{gs2}} \tag{2}$$

namely assuming that the pole is located well above the gain bandwidth product (GBW) of the internal op-amp, the voltage gain of the follower can be expressed as:

$$A_v(s) = \frac{V_x(s)}{V_y(s)} = A_{vo}\frac{\omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{3}$$

where:

$$\omega_o = \sqrt{\omega_1\omega_2} \tag{4}$$

$$\omega_1 = \frac{1 + g_{m1}r_1}{C_1 r_1} \approx \frac{g_{m1}}{C_1} \tag{5}$$

$$\omega_2 = \frac{g_{mb3} + g_{ds3} + g_{ds8}}{C_x} \approx \frac{g_{mb3}}{C_x} \tag{6}$$

and:

$$Q = \frac{\sqrt{\frac{\omega_1}{\omega_2}}}{1 + \frac{\omega_1}{\omega_2(1+g_{m1}r_1)}} \tag{7}$$

where C_1, r_1 are the output capacitance and resistance of the first stage of the op-amp, and C_x is the capacitance of the X terminal.

As it can be concluded from the above equations it is relatively easy to provide stable operation of the follower even for large C_x and without any compensation capacitance inside the feedback loop, which is beneficial for silicon area. The quality factor Q is relatively low for $\omega_1 < \omega_2$, i.e. for small capacitance C_x, then it increases with increasing C_x (decreasing ω_2), achieves its maximum for $\omega_2 = \omega_1/(1+g_{m1}r_1)$, which is equal to $Q_{max} = (1+g_{m1}r_1)^{1/2}/2$ and then again starts to decrease. Thus, the circuit can operate even for very large C_x without any compensation capacitance, provided that the resulting slew-rate (SR) and Q_{max} will be sufficient for a given application.

The ease of frequency compensation may be attributed to the low open-loop voltage gain of the internal op-amp, which is lowered by the bulk-drain connection of M_3.

For $\omega_1 << \omega_2$, the 3-dB frequency of the Y-X follower may be approximated as:

$$f_{3dB} \approx \frac{g_{m1}}{2\pi C_1} \tag{8}$$

Assuming $g_{m1}/g_{mb1} = g_{m2}/g_{mb2}$, the dc voltage gain of the follower can be expressed as:

$$A_{vo} = \frac{A_{eq}}{1 + A_{eq}} \tag{9}$$

where A_{eq} is the voltage gain of an equivalent op-amp operating in a voltage follower configuration, which is given by [12]:

$$A_{eq} = \frac{g_{mb1}}{g_{o1}} \cdot \frac{g_{m3}}{g_{o3}} \cdot \frac{g_{m3} + g_{o3}}{g_{m3} + g_{mb3} + g_{o3}} \tag{10}$$

where $g_{o1} = g_{ds1} + g_{ds6}$ and $g_{o3} = g_{ds3} + g_{ds8}$. As it can be concluded from the above equation, the dc voltage gain of the Y-X follower is close to the voltage gain of the follower based on the unloaded two-stage internal op-amp, despite the drain-bulk connection in M_3. Even though the value of A_{eq} is subject to transistor mismatch, the voltage gain error

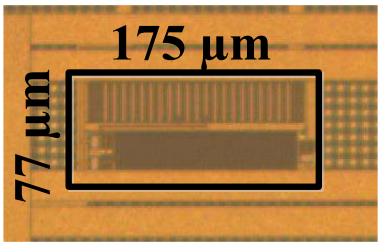

FIGURE 3. Chip microphotograph of the proposed BD-CCII.

with respect to unity can be maintained much below 1% for reasonable transistor sizes [12].

The output resistance of the voltage follower (i.e. the resistance R_x of the CCII) can be approximated as:

$$R_x \cong \frac{1}{g_{m3}\frac{g_{mb1}}{g_{o1}}} \tag{11}$$

thus, it is equal to the reciprocal value of the transconductance g_{m3} multiplied by the voltage gain of the input differential amplifier. Since the output resistance of the Z terminal is equal to $R_z = 1/g_{o4}$, where $g_{o4} = g_{ds4} + g_{ds9}$, then the R_z/R_x ratio is given by:

$$\frac{\boldsymbol{R_z}}{\boldsymbol{R_x}} \cong \frac{\mathbf{g_{m3}}}{\mathbf{g_{o4}}} \cdot \frac{\mathbf{g_{mb1}}}{\mathbf{g_{o1}}} \tag{12}$$

and can exceed $10^3\,\Omega/\Omega$. Given that $V_z = V_x$, the dc current gain I_z/I_x is equal to the ratio of transconductances g_{m4}/g_{m3} and is equal to unity as long as transistor mismatch is not considered.

Another interesting property of the proposed structure of the BD CCII is that the 3-dB frequency of the current amplifier can be much larger than the GBW product of an internal op-amp. This may be attributed to the additional feedforward path from X to Z terminals, through the bulk terminal of M_4. Since the bulks of M_3 and M_4 are shorted together, the two transistors form a BD current mirror which can transfer a current even for frequencies much above the GBW of the internal op-amp. Hence, the 3-dB frequency of the current amplifier for the Z terminal shorted to ground for ac signals and the X input excited with an ideal current source can be approximated as:

$$\omega_i \approx \frac{g_{mb3}}{C_x} \tag{13}$$

where C_x is the total capacitance associated with the X terminal of the CCII.

The input referred thermal noise of the considered CCII is determined by the input noise of the input differential amplifier (M_1, M_2, M_6, M_7) and can be approximated as:

$$\bar{v_n^2} = 2\frac{2nkT}{g_{mb1}^2}\left(g_{m1,2} + g_{m5,6}\right) \tag{14}$$

where n is the subthreshold slope factor (assumed identical for p- and n-channel transistor), k is the Boltzmann constant and T is the temperature.

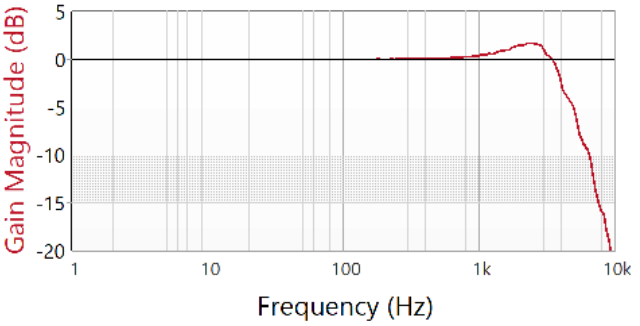

FIGURE 4. Measured frequency response of the voltage gain V_X/V_Y.

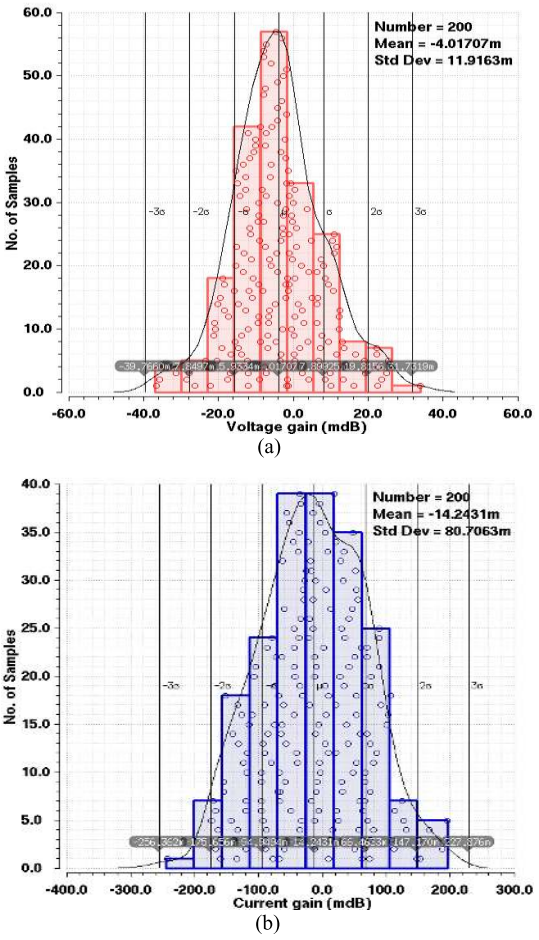

FIGURE 5. The histogram of the (a) voltage and (b) current gains @100Hz based on Monte Carlo analysis.

III. EXPERIMENTAL RESULTS

The proposed BD-CCII has been implemented in a standard 0.18 μm CMOS process from TSMC ($V_{TH} \approx +/-0.5$ V). The chip microphotograph is shown in Fig. 3 with total chip area of 0.0134 mm^2. The circuit was designed for $V_{DD} = 0.3$ V, $I_B = 2.5$ nA, nevertheless it can operate also from larger V_{DD} (up to 0.5 V) and larger biasing currents (up to around 100 nA), which would result in larger bandwidth. The value of the maximum biasing current depends on the V_{DD}/V_{TH} ratio, therefore, using processes with lower V_{TH} the biasing current could be significantly increased.

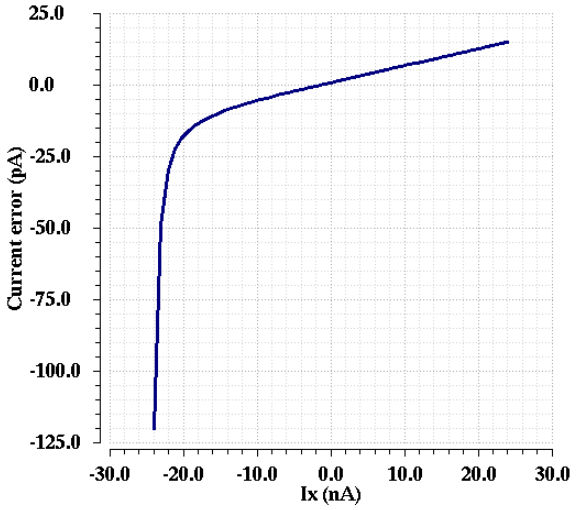

FIGURE 6. The simulated dc current error versus I_X.

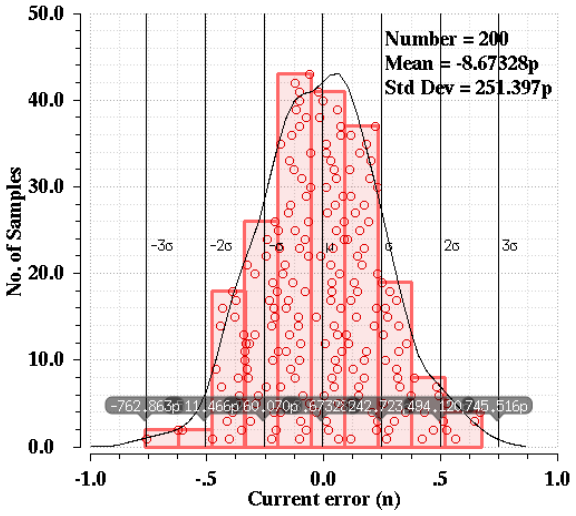

FIGURE 7. The histogram of the DC current error based on Monte Carlo analysis.

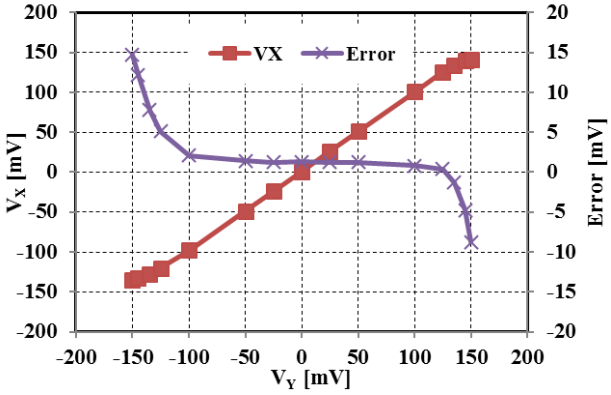

FIGURE 8. Measured DC characteristic of the BD-CCII.

In this design, the biasing current has been adjusted to obtain minimum V_{DD} for the given V_{TH} voltages, while taking into account also the possible process and temperature variations. The load capacitance was 30 pF. The transistor dimensions in μm/μm were as follows: M_1, M_2, M_5 = 50/1, M_3, M_4 = 5 × 50/1, M_6, M_7 = 100/1, M_8, M_9 = 5 × 100/1. The transistor channel lengths were chosen relatively large in order to decrease their output conductances and consequently improve the accuracy of the dc voltage and current gains and the R_Z/R_X ratio. The W/L ratios are also relatively large, to decrease the V_{GS} voltages of transistors for the given biasing currents, as well as to decrease their flicker noise and offset.

Once the channel lengths were set, the channel widths were determined during the simulation phase to meet the requirement $|V_{GSqi}| \approx V_{DD}/2$, where V_{GSqi} is the quiescent gate-source voltage of the i-th MOS transistor (i=1-9). This ensures the largest voltage headroom for possible

TABLE 1. Worst-case performances of the BD-CCII over process and temperature corners for V_{DD} =0.3 V, C_L =30 pF.

Parameter (T=27 °C)	SS	SF	TT	FS	FF
Power consumption [nW]	18.8	18.9	19	19.1	19.3
-3dB bandwidth I_Z/I_X [kHz]	37.66	39.18	39.2	39.29	40.99
-3dB bandwidth V_X/V_Y [kHz]	5.33	5.25	5.32	5.38	5.31
Current gain I_Z/I_X [-]	0.999	0.999	0.999	0.999	0.999
Voltage gains V_X/V_Y [-]	0.999	0.999	0.999	0.999	0.998

Parameter (TT corner)	-10°	27°	70°
Power consumption [nW]	18.7	19	21
-3dB bandwidth I_Z/I_X [kHz]	44.4	39.2	36
-3dB bandwidth V_X/V_Y [kHz]	5.8	5.32	4.7
Current gain I_Z/I_X [-]	0.999	0.999	0.997
Voltage gains V_X/V_Y [-]	0.998	0.999	0.991

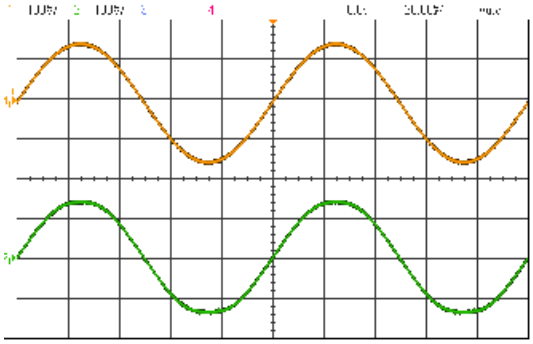

FIGURE 9. Measured sine wave responses V_Y and V_X of the CCII for rail-to-rail input and 100 Hz frequency.

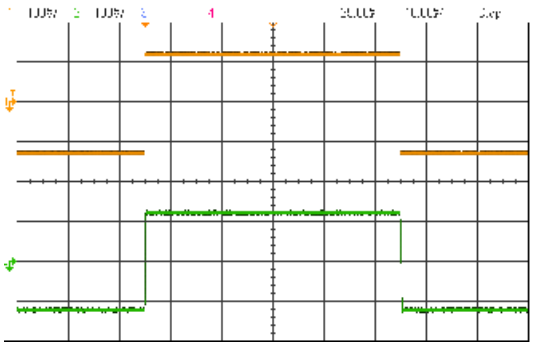

FIGURE 10. Measured step responses V_Y and V_X of the CCII with 100 Hz frequency.

TABLE 2. Experimental results of the BD-CCII and compared to others.

Parameter	This work BD-CCII		[7]	[8]	[9]	[11]
Supply voltage [V]	0.3	0.5	±0.4	±0.5	0.5	0.4
Bias current [nA]	2.5	40	-	-	-	-
Power consumption [nW]	19	509	64E3	10E3	30E3	1.8E3
Slew rate SR+ [V/ms]	2	45.2	-	-	-	-
Slew rate SR- [V/ms]	0.66	11.2	-	-	-	-
-3dB bandwidth I_Z/I_X [kHz]*	39.2	578	13E3	8.2E3	10E3	1.25E3
-3dB bandwidth V_X/V_Y [kHz]	4.1	56.4	14E3	4.8E3	11E3	1E3
Current gain I_Z/I_X [-]*	0.999	0.999	1	1	0.996	1
Voltage gains V_X/V_Y [-]	0.9987	0.999	1	1	0.998	1.004
Input current range [nA]	±24	±400	± 7E3	± 3E3	± 15E3	-
Input voltage range [mV]	300	500	± 380	± 500	60:460	-
Input thermal noise [$\mu V/Hz^{1/2}$]*	1.9	0.5	-	-	-	-
Input referred offset [mV] [(a)]	2	2	-	-	-	-
Current offset [pA] [(a)]	248	248	-	-	-	-
Parasitic resistance R_Y [MΩ]*	703	664	≈ ∞	≈ ∞	≈ ∞	-
Parasitic resistance R_X [Ω]*	56E3	3E3	27	42	260	106
Parasitic resistance R_Z [MΩ]*	94.7	8	0.89	53	0.113	-
$(V_{TH}/V_{DD})*100$ [%]	166	100	62	50	100	87
$(V_{in\text{-}max}/V_{DD})*100$ [%]	100		95	100	80	-
C_L [pF]	30		-	-	-	-
CMOS technology [µm]	0.18 TSMC		0.18 TSMC	0.18 TSMC	0.18 TSMC	0.09 TSMC
Chip area [mm^2]	0.0134		-	-	-	-
Results	Meas.		Sim.	Sim.	Sim.	Sim.

(*) Simulated

[(a)] standard deviation (MC 200 runs)

process/temperature variations and signal swing. The biasing currents of the input differential amplifier were set to ensure sufficiently low Y input referred thermal noise of the CCII. The proportions of currents $I_{D3}/I_{D1,2}$ were determined to ensure sufficient stability margin for the assumed load capacitance of the X terminal (sufficient value of g_{mb3}). For the given W/L ratios the parasitic pole associated with the drain/gate node of M_2 was much above the 3-dB frequency of the Y-X voltage follower, hence, its impact was negligible. Finally, the results of MC and noise analyses showed that the assumed transistor channel areas were sufficiently large to provide acceptable levels of input referred flicker noise, offsets and the voltage/current gains accuracies.

Selected post-layout simulation and measured results of the proposed BD-CCII are shown in Figs. 4-10. For the purpose of measurement a symmetrical supply voltage of $+/-0.15$ V was used. Fig. 4 shows the measured magnitude response of the voltage follower (V_X/V_Y) using the Vector Network Analyzer Bode 100. The dc voltage gain was -11 mdB (0.9987 V/V), which corresponds to the accuracy provided by a 57.7 dB op-amp operating in a unity-gain feedback configuration. This confirms experimentally, that a high-precision voltage follower can be realized using relatively low voltage gain of the internal op-amp.

The 3-dB cutoff frequency was 4.1 kHz, while the estimated Q factor (see (7)) was around 1.25. Note, that the above results were achieved for relatively large C_x (30 pF) and without any compensation capacitance, that confirms theoretical predictions.

Fig. 5 shows the histogram of the DC voltage and current gains of the CCII based on Monte Carlo analysis (200 runs). The standard deviation was 11.9 mdB and 80.7 mdB for the voltage and current gain, respectively. Note, that the maximum error of a voltage gain was 40 mdB (0.46 %), which is still acceptable in many applications. The maximum error of a current gain was larger and equal to around 2 %.

Fig. 6 shows the simulated DC current error ($I_Z - I_X$) versus the input current I_X. The current error was below 18 pA for I_X in range of ±20 nA. Fig. 7 shows the histogram of the DC current error based on Monte Carlo (200 runs). The standard deviation was 251 pA. Figs. 6 and 7 confirm acceptable current tracking accuracy.

Fig. 8 shows the measured DC transfer characteristic of the Y-X voltage follower and the voltage error. The voltage error was ranging from -8.7 mV to 14.6 mV for V_Y ranging from 150 mV to -150 mV respectively (i.e. rail-to-rail).

The measured sine-wave response of the follower with the input sine-wave of 300 mV peak-to-peak value (rail-to-rail)

and 100-Hz frequency is shown in Fig. 9. The THD was below 1% for $V_Y < 246\ mV_{pp}$.

Fig. 10 shows the measured step response of the BD-CCII when a 250 mV peak-to-peak and 100 Hz square wave was applied to the Y terminal. The slew rate SR+ was 2V/ms and SR- was 0.66 V/ms. The SR was limited mainly by the class A output stage, therefore it is unsymmetrical. This disadvantage could be overcome applying a class AB output stage.

Table 1 shows the worst case performances of the BD-CCII over process and temperature variation. The process corners for MOS transistor were fast-fast (FF), fast-slow (FS), slow-fast (SF) and slow-slow (SS); and the temperature corners were -10 °C, 27 °C and 70 °C. The results in Table 1 confirm the robustness of the design over process and temperature corners.

Table 2 summarizes the measured results of the proposed BD-CCII for $V_{DD} = 0.3$ V and 0.5 V and compare them with other LV LP CCIIs. The proposed BD-CCII offers the lowest voltage supply and power consumption and the highest V_{TH}/V_{DD} and V_{in-max}/V_{DD} ratios. As it was predicted theoretically, the 3-dB bandwidth of the current gain was much larger than the 3-dB frequency of the voltage gain. The input current range was limited by the biasing current of M_3 (M_4). The thermal noise was dominant for frequencies larger than around 5 Hz. The R_Z/R_X ratio for the considered CCII was around 1.7E3, which seems to be sufficient for many applications. Note, that the larger value of V_{DD} (larger V_{DD}/V_{TH} ratio) allows increasing both, the voltage and the current gain bandwidth, since larger biasing currents are possible. Therefore, applying the low V_{TH} CMOS processes, one could achieve much higher frequency range using the same structure. In such a case also the cascode/self cascode connections could be used, thus further improving the accuracy of the resulting CCII.

Note, that the CCII is suitable to serve in portable or implementable biomedical applications (e.g. filters, oscillators, amplifiers) where the frequency range of the biological signals is from sub-hertz up to 10 kHz and the low-voltage supply low-power consumption are the main demand.

IV. CONCLUSION

The paper presents the measured results for an ultra-low voltage low-power CCII based on bulk-driven technique. The proposed structure is simple and capable to work with 0.3 V supply while consuming 19 nW of power. The very low minimum V_{DD} was achieved thanks to the application of non-tailed differential stage. The circuit offers good accuracy of the voltage gain with relatively low dc voltage gain of an internal op-amp, which allows neglecting a compensation capacitance even for large capacitance C_x. The 3-dB frequency of the current gain is increased due to the additional feedforward path, which is an additional advantage of the proposed structure. The measured results are close to the simulated ones and confirm the attractive features of the proposed circuit.

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