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0.5-V High Linear and Wide Tunable OTA for Biomedical Applications

FABIAN KHATEB[1,2], TOMASZ KULEJ[3], MEYSAM AKBARI[4], AND MONTREE KUMNGERN[5]

[1]Department of Microelectronics, Brno University of Technology, 60190 Brno, Czech Republic
[2]Faculty of Biomedical Engineering, Czech Technical University in Prague, 27201 Kladno, Czech Republic
[3]Department of Electrical Engineering, Czestochowa University of Technology, 42-201 Czestochowa, Poland
[4]Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan
[5]Department of Telecommunications Engineering, School of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand

Corresponding author: Fabian Khateb (khateb@vutbr.cz)

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ABSTRACT This paper presents a low-voltage nano-power multiple-input operational transconductance amplifier (MI-OTA) with high linearity performance and increased input voltage swing. The enhanced performances are achieved thanks to employing several techniques as the bulk-driven, source-degeneration, self-cascode and negative conductance along with the concept of the input signal attenuation formed by multiple-input MOS transistor. The MI-OTA is widely tunable that serves for biological signals processing. A 3rd-order Butterworth band-pass filter (BPF) for electrocardiogram (ECG) signal processing with 55.8 dB dynamic rang is presented. The MI-OTA circuit is designed for 0.5V voltage supply and offers a 0.22% total harmonic distortion (THD) for 0.2V$_{pp}$ input signal with total power consumption of 13.4nW. Extensive simulation results including Monte Carlo analysis and process, voltage, temperature (PVT) corners using the 0.18μm CMOS technology from TSMC confirm the characteristics of the proposed MI-OTA and the filter.

INDEX TERMS Operational transconductance amplifier (OTA), bulk-driven MOS transistor, multiple-input OTA, high-order filters.

I. INTRODUCTION

The transconductor or the operational transconductance amplifier (OTA) is a basic block for analog integrated circuit design [1]–[10]. A wide range of transconductance adjustment, high linear characteristic, wide input signal swing with low distortion under low-voltage supply are the key features for OTAs serving in modern wearable electronics, predominantly the biomedical ones. The high power efficiency is essential for these applications to minimize the battery size and extend its lifetime. For biomedical low-frequency applications, the operation in subthreshold region using the bulk-driven differential pair efficiently increases its linear range and reduces its transconductance, resulting in desirable low time constants for G$_m$-C biomedical filters [9], [10]. However, due to the low bulk transconductance g_{mb} compared to the gate g_m one the total DC gain of the OTA is reduced [11]–[19]. Another way to increase the linear input voltage swing is the concept of the input signal attenuation formed by either capacitive or resistive divider [1]. In a capacitive divider, the multiple-input floating-gate (MIFG) MOS transistor is used [2]–[4]. However, the MIFG, which originally served for digital memory applications, comes with several disadvantages. It is based on charge conservation; hence, it cannot be used in modern nano-scale CMOS technologies with gate leakage [5]. The realization of MIFG MOS transistor requires technology with double poly-silicon that obstruct its using in one poly-silicon technologies that are widely used. In addition, although there are several techniques to eliminate the charge trapped in the floating gate, the MIFG based CMOS structures still suffer from higher voltage offset compared to conventional gate-driven designs. To eliminate the MIFG disadvantages, an alternative technique called the multiple-input MOS transistor (MI-MOST) has been recently presented and experimentally verified by Khateb *et al.* [20]–[22]. Unlike the MIFG transistor the MI-MOST can be implemented in any standard CMOS technology, a combination of capacitive-resistive divider forms the attenuation and hence it has no floating-gate, nor trapped charge or extra voltage offset [20]–[29]. It is worth noting that due to input voltage attenuation of the multiple-input techniques (MIFG or MI-MOST) the total equivalent

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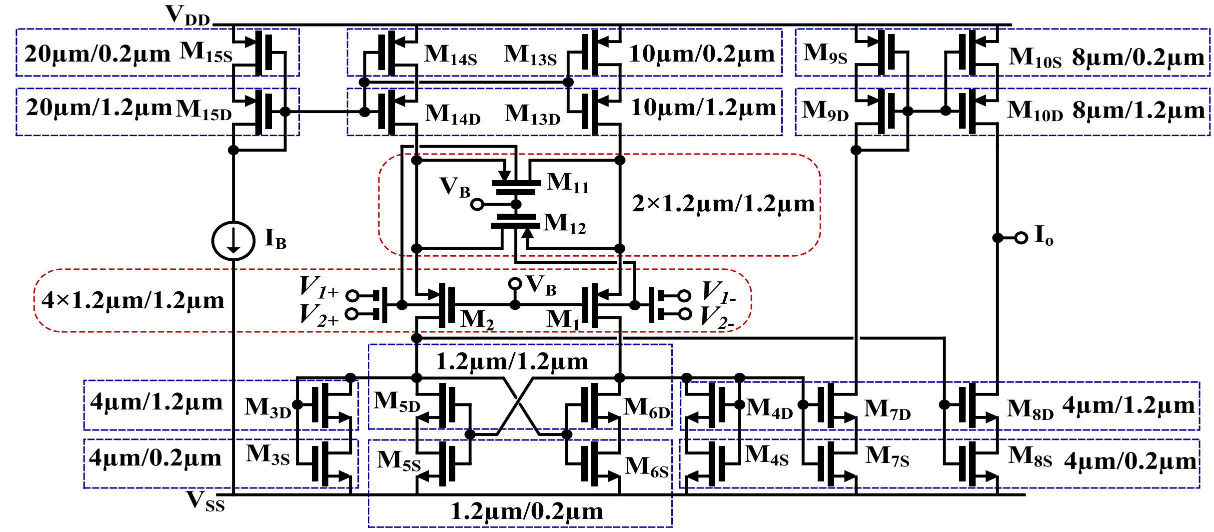

FIGURE 1. The proposed CMOS structure of the MI-OTA.

DC gain of the OTA is reduced. In general the concept of multiple-input active devices attracted attention of the circuit designers since it offers the advantage of arbitrary summing or subtracting the voltage signals at the inputs allowing topology simplification and reducing the number of used components [30], [31], [40], [41]. Another way to increase the OTA's linearity is the source degeneration technique; however, the total DC gain is also reduced [1].

This paper presents low-voltage supply low-power consumption OTA operating in subthreshold region and using the bulk-driven MI-MOST as differential pairs, the differential stage includes the source degeneration transistors. All these techniques improve the linearity significantly but reduce the DC gain of the OTA. Therefore, in order to boost the DC gain, the OTA employs two techniques suitable for low-voltage operation, the self-cascode transistor (SC) [32]–[33] and the partial positive feedback [34]. These techniques increase the output resistance of the transistors and hence the total DC gain of the OTA. The paper is organized as follows: in Sec. II the CMOS structure of the MI-OTA is presented and analyzed, Sec. III presents application of 3rd-order Butterworth band-pass filter for ECG signal processing, Sec. IV presents the simulation results and finally Sec. V concludes the paper.

II. THE PROPOSED OTA

Fig. 1. shows the proposed CMOS structure of the MI-OTA. The circuit can be seen as a current mirror OTA, with a bulk-driven (BD) source degenerative differential input pair $M_{1,2}$ and $M_{11,12}$. The multiple input transistors M_1 and M_2 were realized using parallel connections of capacitors and resistors. The symbol and schematic of the MI transistor applied in this design is shown in Fig. 2. The resistance R_{MOS} is used to provide proper DC biasing of the bulk terminals of M_1 and M_2. The resistance should be large with minimum occupied chip area; therefore, it is realized with two minimum-size

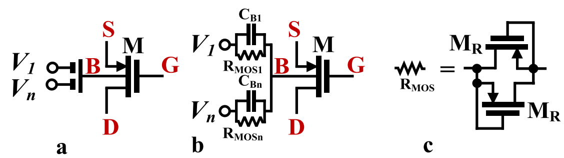

FIGURE 2. The MI-MOS transistor: a) symbol, b) realization, c) realization of R_{MOS}.

PMOS transistors operating in a cut-off region, as shown in Fig. 2(c).

For AC signals, the resistors R_{MOS} are shunted with capacitances C_B, that create an analog voltage divider/voltage summing circuit. For frequencies $f \gg 1/2\pi R_B C_B$, the AC voltage at the bulk terminal of an MI transistor (V_b) can be expressed as:

$$V_b = \sum_{i=1}^{n} \beta_i V_i \tag{1}$$

where n is the number of inputs of the MI transistor and β_i is the voltage gain of the capacitive divider from i-th input. Neglecting the input capacitance of the BD MOS, the voltage gain β_i can be expressed as:

$$\beta_i = \frac{C_{Bi}}{\sum_{i=1}^{n} C_{Bi}} \tag{2}$$

Note, that with identical capacitors C_{Bi}, all coefficients β_i are equal as well and equal to 1/n.

The input pair $M_{1,2}/M_{11,12}$ is biased by a current sources based on the self-cascode transistors $M_{13S,D}$ and $M_{14S,D}$. It is worth noting, that all transistors in this design, excluding the input differential pair, are realized using self-cascode connections that allows increasing the output resistances of such a complex device, while not limiting the minimum voltage drops across this element significantly. The output resistance of the SC M_{SD} transistors can be expressed as:

$$R_{oMSD} = r_{oMS} + r_{oMD} + g_{mMD} r_{oMS} r_{oMD} \approx g_{mMD} r_{oMS} r_{oMD} \tag{3}$$

Thanks to the increased output resistance, the SC transistors allows increasing the overall DC voltage gain of the OTA, with only minor limitation of the output voltage swing.

The basic topology of the input differential stage $M_{1,2}/M_{11,12}$ is derived from [35]. The I/V DC transfer characteristic of the input differential pair M_1 and M_2 is linearized with transistors M_{11} and M_{12} operating in a triode region. Since the gates and the bulks of $M_{1,2}$ and $M_{11,12}$ are tied together, then both the V_{GS} as well as the V_{BS} voltages of the four transistors are equal to each other, provided that, the voltages at the bulk terminals of M_1 and M_2 are equal as well. This means, that the linearization principle is insensitive to the input common-mode variations, which is an advantage of this topology.

In the original design, the transistors $M_{1,2}$, $M_{11,12}$ were controlled with their gate terminals. In this design, we propose to use the bulk terminal of the devices as a signal input, while biasing their gates with a constant potential V_B. Such modification allows increasing the linear range of the OTA.

Assuming the following model of a p-channel MOS transistor operating in subthreshold:

$$I_D = I_T\left(\frac{W}{L}\right) exp\left(\frac{V_{SG}+V_{TH}}{n_p U_T}\right)\left[1 - exp\left(-\frac{V_{SD}}{U_T}\right)\right] \quad (4)$$

where I_T is the technology current, W and L are the transistor channel width and length respectively, V_{TH} is the threshold voltage, n_p is the subthreshold slope factor and U_T is the thermal potential, the differential output current of the input pair I_{D1}-I_{D2}, where M_1 and M_2 are biased with the current of $I_B/2$ each, and the inputs are controlled with fully-differential signals, can be expressed as:

$$I_{D1} - I_{D2} = I_B tanh\left(\eta\frac{V_{bdiff}}{2n_p U_T} - tanh^{-1}\left[\frac{1}{4m+1} tanh\left(\eta\frac{V_{bdiff}}{2n_p U_T}\right)\right]\right) \quad (5)$$

where $\eta = g_{mb1,2}/g_{m1,2}$ is the ratio of the bulk to gate transconductance of the input transistors M_1 and M_2 at the operating point respectively, V_{bdiff} is the voltage difference between the bulk terminals of M_1 and M_2, which with respect to the inputs of the OTA can be expressed as:

$$V_{bdiff} = \sum\nolimits_{i=1}^{n} \beta_i\left(V_{i+} - V_{i-}\right) \quad (6)$$

In (5) $m = (W_{11}/L_{11})/(W_1/L_1)$ is the relative aspect ratio of the two matched transistor pairs $M_{11,12}$ and $M_{1,2}$, which affects the circuit linearity (the shape of the transconductance function). For optimum linearity $m = 0.5$. This result is independent of the biasing current I_B. Note, that equation (5) is nearly identical with the one derived in [36] for a gate driven (GD) pair. The equation for a bulk-driven pair contains an additional coefficient η. Thus, the BD transconductor can be considered as a GD one, with an input signal attenuated $1/\eta$ times.

Assuming a 1% variation of the first derivative of (5), with respect to V_{bdiff} (i.e. the small signal transconductance), with $n_p U_T = 35$mV, we find a linear range of 55.7mV/η. With a typical value of $\eta = 0.33$ for the used technology in subthreshold region, this range is extended to 167mV. Thus, the linear range of the BD version of the source-degenerative OTA is significantly increased, as compared to its gate driven counterpart.

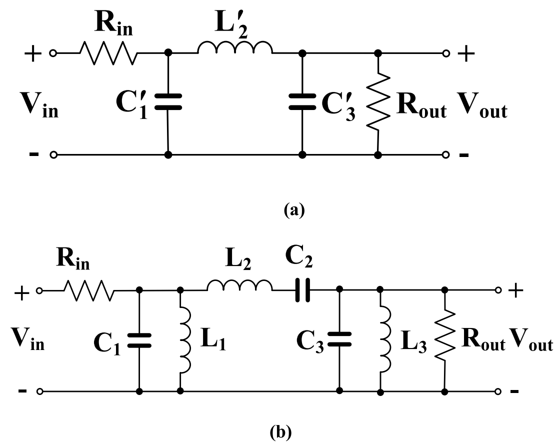

FIGURE 3. The 3rd -order LPF RLC prototype (a) and the 3rd-order BPF RLC prototype (b).

Due to the additional capacitive divider at the input, this linear range is further increased. For instance, assuming that only one differential input is controlled and the other ones are grounded for AC signals, with all capacitors C_{Bi} equal to each other, the voltage gain from i-th differential input to the bulk terminals of the internal pair is equal to $\beta_i = 1/n$. With 2-input OTA, as in Fig. 1, the linear range is thus increased to 334mV.

The combination of three techniques; source degeneration, driving with bulk terminals and application of an additional capacitive voltage divider allows increasing the linear range of a subthreshold transconductor, but leads to degradation of the input transconductance and consequently the DC voltage gain. In order to overcome this issue, two other techniques have been used. Firstly, all current mirrors were realized with SC transistors. Secondly, a partial positive feedback has been introduced with a cross-coupled pair M_{SD5} and M_{SD6}. The cross coupled pair generates negative conductances $-g_{mSD5} = -g_{mSD6}$ at its input ports, that decrease the total conductances loading the differential output of the input pair to $g_{load} = g_{mSD3,4} - g_{mSD5,6}$.

It should be pointed out that the minimum value of the load conductance g_{load} is first of all limited by the maximum voltage gain from inputs of the OTA to the drain terminals of M_1 and M_2. In order to avoid additional nonlinear distortion, introduced by this load, the value of this voltage gain should be low enough to provide operation of all transistors M_{3D}-M_{6D} in saturation, for the whole linear range of the OTA, which limits the maximum voltage swing at these points. If this condition is satisfied, then it can be assumed, that the load of the input pair will not introduce additional nonlinear distortion.

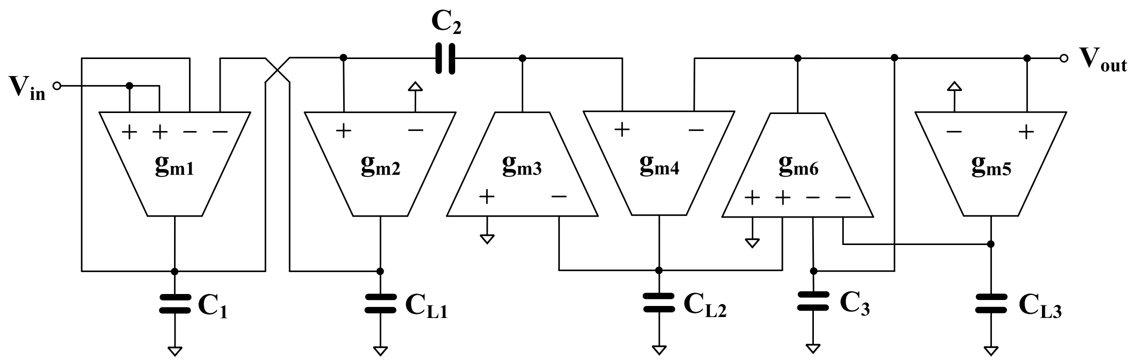

FIGURE 4. The 3rd-order Butterworth BPF using MI-OTA.

Assuming that $M_{SD4} = M_{SD7} = M_{SD8}$ and $M_{SD9} = M_{SD10}$, the small signal transconductance of an n-input OTA, from one differential input, can be expressed as:

$$G_m = \frac{1}{n} \cdot \frac{g_{mb1,2}}{1 + g_{m1,2}(r_{ds11}||r_{ds12})/2} \cdot \frac{g_{mSD7}}{g_{mSD3,4} - g_{mSD5,6}} \quad (7)$$

where $r_{ds11,12}$ is the r_{ds} resistance of M_{11} and M_{12} operating in a triode region. For the circuit considered in this work n = 2.

The DC voltage gain of the OTA is:

$$A_{VO} = G_m[(g_{mD10}r_{dsD10}r_{dsS10}) \,||\, (g_{mD8}r_{dsD8}r_{dsS8})] \quad (8)$$

Thus both, G_m as well as A_{vo} will be a function of a difference of transconductances of the SC transistors $M_{SD3,4}$ and $M_{SD5,6}$, and increase with decreasing this difference. However, in such a case, both, the amplitude of the voltage swing at the load of the differential pair, and the circuit sensitivity to transistor mismatch is increasing. Therefore, there is a tradeoff between the DC voltage gain, circuit sensitivity to mismatch and nonlinear distortion. If the load of the differential pair operates as linear circuit, then the large-signal transfer characteristic of the OTA from one differential input can be expressed as:

$$I_o = \frac{I_B}{n} tanh\left(\eta\frac{V_{1+} - V_{1-}}{2nU_T} - tanh^{-1}\left[\frac{1}{4m+1} tanh \times \left(\eta\frac{V_{1+} - V_{1-}}{2nU_T}\right)\right]\right) \cdot \frac{g_{mSD7}}{g_{mSD3,4} - g_{mSD5,6}} \quad (9)$$

and, neglecting second order effects, its linear range is the same as for an input differential pair.

III. THIRD-ORDER BUTTERWORTH BPF

We will start the design of the third-order BPF with an appropriate RLC prototype. The RLC prototype is transformed from a third-order low-pass filter (LPF) as shown Fig. 3(a) and the corresponding third-order BPF is shown in Fig. 3(b). The capacitor $C_1^{'}$ is transformed to a parallel connection of capacitor C_1 and inductor L_1, the capacitor $C_3^{'}$ is transformed to a parallel connection of capacitor C_3 and inductor L_3 whereas inductor $L_2^{'}$ is transformed to a series connection of inductor L_2 and capacitor C_2 [37].

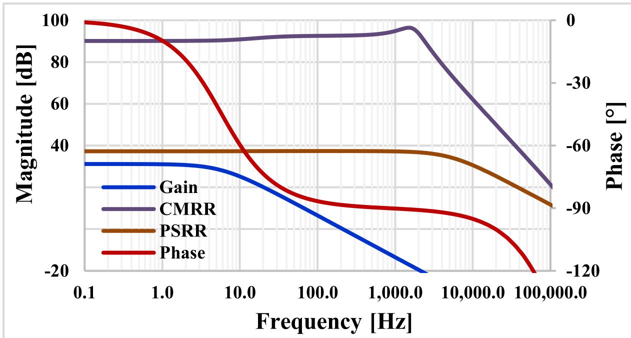

FIGURE 5. The gain, phase, CMRR and PSRR characteristics of the integrator for I_B = 10 nA.

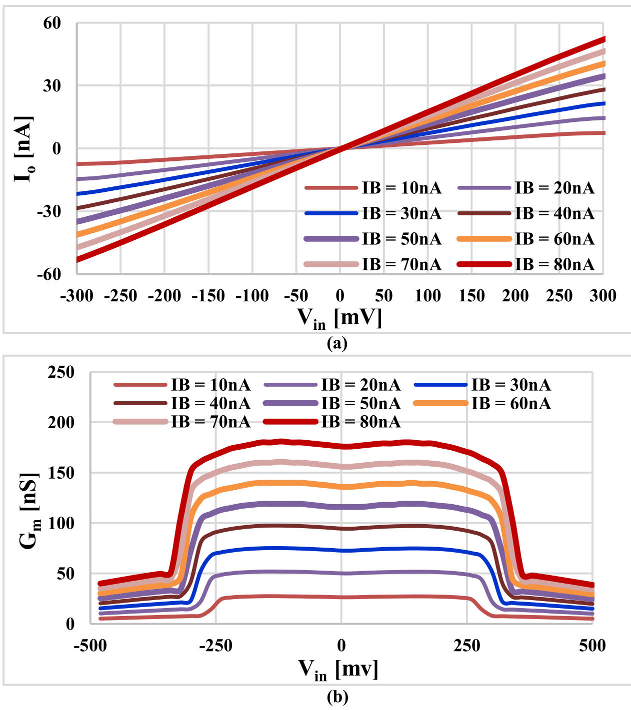

FIGURE 6. The output current (a) and the transconductance (b) versus the input voltage for various I_B.

Letting $R_{in} = R_{out} = R$, denoting the quality factor of the BPF as Q, and its center frequency as ω_o, the passive values

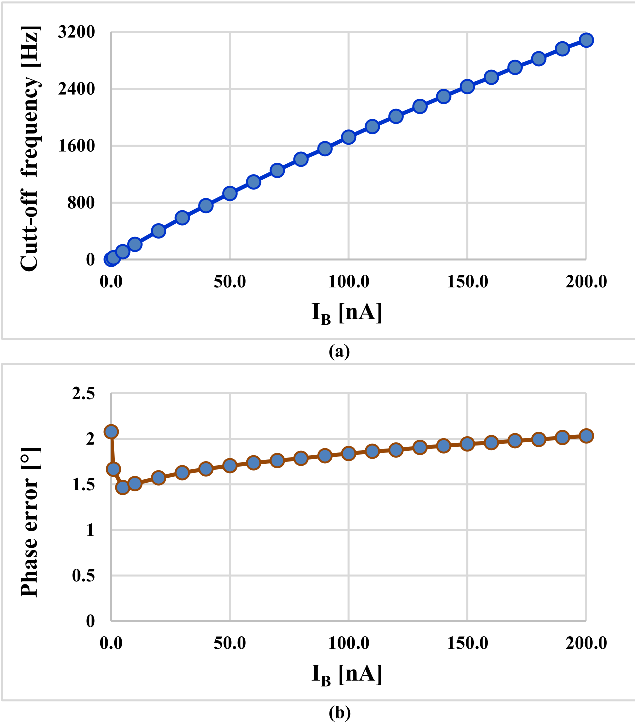

FIGURE 7. The cut-off frequency (a) and the phase error (b) of the integrator for various I_B.

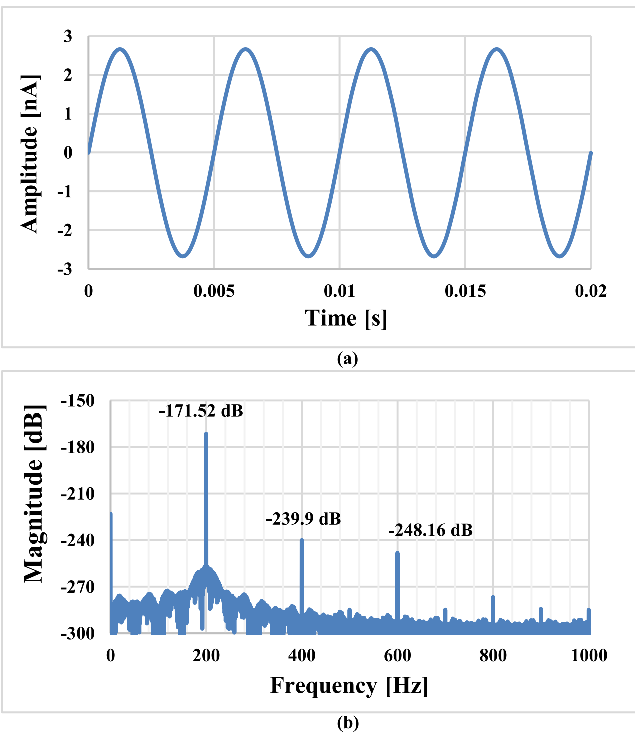

FIGURE 8. The transient analysis of the output signal (a) and the signal spectrum (b) for $I_B = 10$ nA.

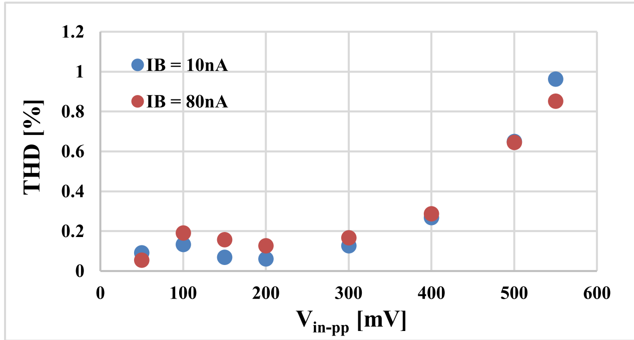

FIGURE 9. The THD versus input signal $V_{in\text{-}pp}$.

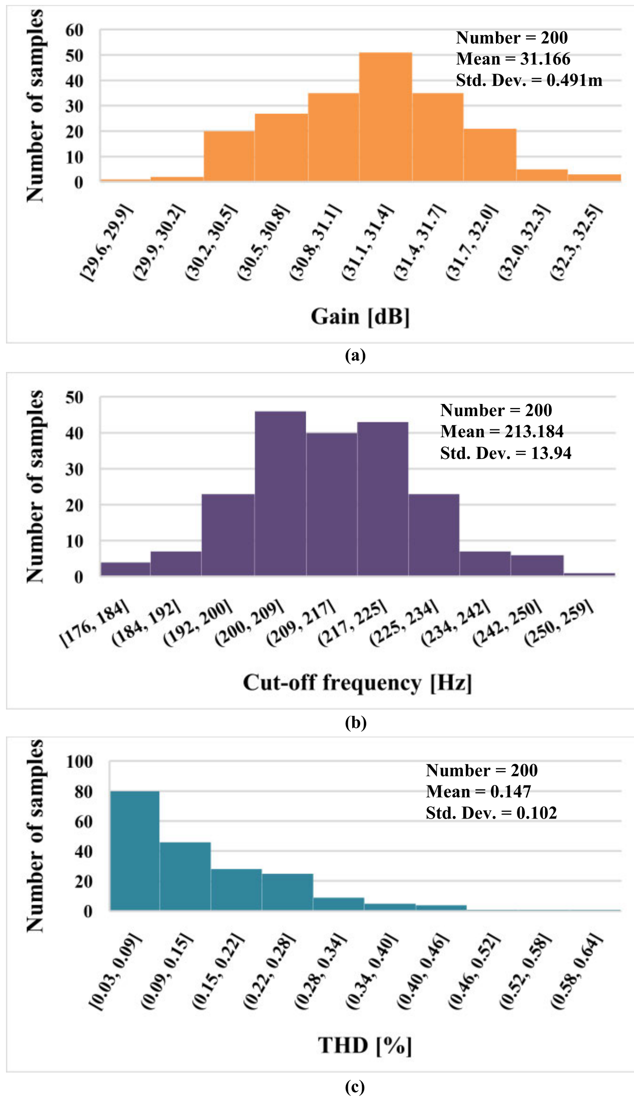

FIGURE 10. The histogram of the gain, cut-off frequency, phase error and THD with 200 runs MC analysis.

in Fig. 3(b) can be given using Fig. 3(a) as [37]:

$$C_1 = QC_1^{`}\left(\frac{1}{R\omega_o}\right) \tag{10}$$

$$L_1 = \frac{1}{QC_1^{`}} \times \frac{R}{\omega_o} \tag{11}$$

$$C_2 = \frac{1}{QL_1^{`}} \times \frac{1}{R\omega_o} \tag{12}$$

TABLE 1. The performance of the integrator with 200 runs MC analysis.

	Min.	Mean	Max.	Std. Dev.
Gain [dB]	29.4	31.17	32.45	0.491
Phase error [°]	1.245	1.5	1.89	0.127
Cut-off frequency [Hz]	175.5	213.2	254.8	13.95
CMRR [dB]	32.47	47.91	81.79	9.3
PSRR [dB]	33.01	36.75	41.33	1.39
THD [%]	0.0327	0.147	0.607	0.102

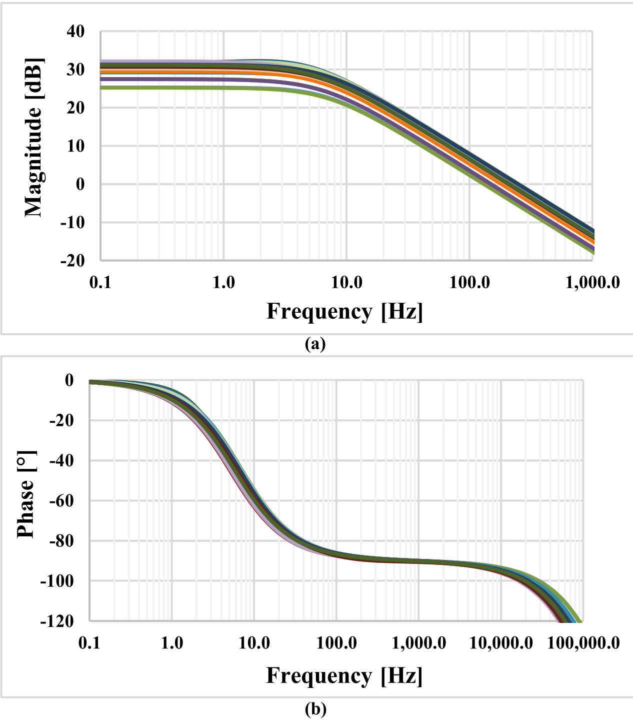

FIGURE 11. The PVT corner simulation gain (a) and phase characteristic (b).

$$L_2 = QL_2^{'}\left(\frac{R}{\omega_o}\right) \tag{13}$$

$$C_3 = QC_3^{'}\left(\frac{1}{R\omega_o}\right) \tag{14}$$

$$L_3 = \frac{1}{QC_3^{'}} \times \frac{R}{\omega_o} \tag{15}$$

To obtain a third-order Butterworth LPF, the normalized LPF values in Fig. 3(a) can be given as $C_1^{'} = 1$ F, $L_2^{'} = 2$ H, $C_3^{'} = 1$ F, $R = 1\Omega$ where $\omega = 1$ rad/s: thus third-order Butterworth BPF values can be obtained using (10)-(15).

Fig. 4 shows the third-order Butterworth BPF using MI-OTA. Thank to MI-OTA, the number of active components can be reduced compared with previous work [7]. The inductor can be implemented using OTA-based gyrator. Assume that all OTAs are identical, inductance value can be given as $L_i = g_m^2 C_{Li} (i = 1, 2, 3)$.

TABLE 2. The performance of the integrator with 200 runs PVT corners analysis.

	Min.	Nom.	Max.
Gain [dB]	25.2	31.17	34.53
Phase error [°]	0.566	1.5	3.08
Cut-off frequency [Hz]	131.5	212.4	250.3
CMRR [dB]	37.2	90.05	89.9
PSRR [dB]	28.5	37.26	44.96
THD [%]	0.061	0.066	0.143

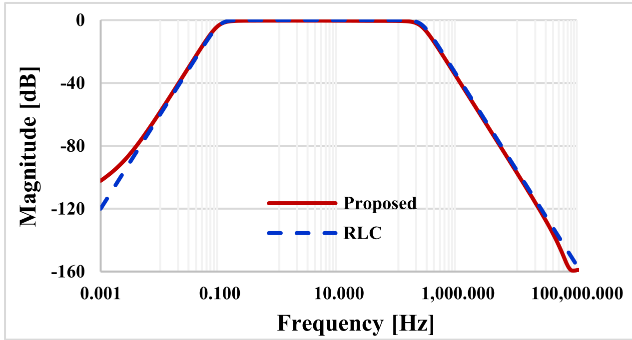

FIGURE 12. The frequency characteristic of the RLC and the proposed filter for $I_B = 20$nA.

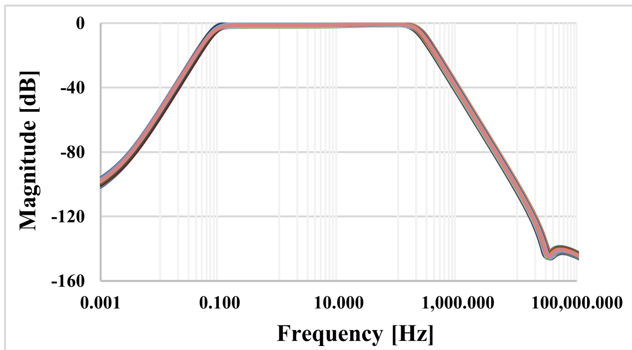

FIGURE 13. The frequency characteristic of the proposed filter for $I_B = 20$nA with 200 runs MC analysis.

IV. SIMULATION RESULTS

The proposed circuit was designed and simulated using the Cadence Spectre simulator using 0.18 μm CMOS technology from Taiwan Semiconductor Manufacturing Company (TSMC). The transistors aspect ratios are shown in Fig. 1. The multiple-input resistor M_R-transistor has 4μm/5μm and the input capacitor C_B is created by the highly linear metal-insulator-metal (MIM) capacitor available in TSMC technology, each $C_B = 0.5$pF. The voltage supply is 0.5V ($V_{DD} = -V_{SS} = 0.25$V) and the bias voltage $V_B = -160$mV. The estimated chip area of the MI-OTA is 0.0088 mm^2.

The OTA-C integrator based on the proposed MI-OTA was loaded with 20pF capacitance. Fig. 5 shows the gain, phase, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) frequency characteristics for the

TABLE 3. Performance comparison between proposed integrator and others.

Parameter	Units	This work	[8]	[9]	[10]
		Multiple-input Bulk-driven	Bulk-driven	Bulk-driven	Bulk-driven
		Single ended	Fully differential	Single ended	Single ended
CMOS technology	µm	0.18	0.18	0.13	0.35
Threshold voltage (V_{TH})	V	0.5	0.5	0.22	0.58
Voltage supply (V_{DD})	V	0.5	0.3	0.25	0.8
Power consumption	nW	0.139–267.5	13 – 97	100	40
Bias current (I_B)	nA	0.1–200	2.5–20	10	-
DC transconductance (g_m)	nS	0.34–383	68–460	22	66
DC voltage gain (A_{vo})	dB	31.17	33.3	-	61
Bandwidth	Hz	2.67–3080	50–334	175	210
CMRR	dB	90.05	54.5	–	–
PSRR	dB	37.26	50.2	–	–
Input offset (V_{OS})	mV	0.224	1	±10.82	±3
Maximum input swing (V_{pp}) for THD ≤ 0.5 %	mV	480	300	100	600
THD at input mV_{pp}	%	0.5 @ 480	0.15 @ 100	0.53 @ 100	0.39 @ 600
Phase error	°	2	0.5–1	–	7
V_{DD}/V_{TH}	-	1	0.6	1.14	1.37
Noise bandwidth	Hz	0.1–200	–	0.2–200	0.2–200
Input referred noise	µVrms	174	–	100	80
Linear input range [HD3 1%](V_{pp})	V	0.55	0.3	0.1	0.1
DR (for HD3 ≤ 1 %)	dB	66.98	–	56.98	58.92
Chip area	mm^2	0.0088	0.035	0.053	0.04
Obtained results	–	Sim.	Exp.	Exp.	Exp.

proposed MI-OTA-C integrator for $I_B = 10$ nA. The low frequency value was 31.17 dB for gain, 90.07 dB for CMRR and 37.26 dB for PSRR. The cut-off frequency (f_c) was 212.4 Hz while the phase shift was 88.5°.

The output current I_o and the transconductance value G_m versus one differential input voltage V_{in} (while other inputs were grounded) for different bias current I_B in range from 10nA to 80nA are shown in Fig. 6(a) and (b), respectively. It is evident the high linear range and the wide tuning capability of the integrator. Note, that in practice I_B can be set by a digitally controlled current source.

Fig. 7(a) and (b) shows the relation of the cut-off frequency and the phase error of the integrator, respectively, for various I_B in range from 0.1nA till 200nA. The cut-off frequency is tunable in frequency range from 2.6 Hz to 3.08 kHz that cover most of biological signal spectrum. The phase error for all bias currents was below 2.2°.

The transient response of the MI-OTA (with $I_B = 10$ nA) for a sine wave signal with $200mV_{pp}$@ 200Hz applied to the input while the output is grounded is shown in Fig. 8(a). The output signal spectrum in Fig. 8 (b) shows that the second harmonic HD2 = −239.9 dB and the third harmonic HD3 = −248.16 dB that indicate very low distortion of the integrator.

The total harmonic distortion (THD) of the integrator for different V_{in-pp}@ 200 Hz and for $I_B = 10$nA and 80nA are shown in Fig. 9. The THD is below 1% for V_{in-pp} below 550mV.

To test the performance characteristics of the integrator the Monte Carlo analysis with mismatch and process variation is used. The histograms of the gain, cut-off frequency, phase error and THD with 200 runs MC analysis are shown in Fig. 10. (a), (b), (c) and (d), respectively. The performance is summarized in Table 1 showing acceptable variation.

The PVT corners simulations have been performed for temperature variations –10–60 °C, for power supply voltage variations V_{DD}±5% and for process corners for MOS transistor: ss, sf, fs, ff, and for the MIM capacitor: ss and ff. The results of the gain and phase characteristics are shown in Fig. 11 (a) and (b), respectively while the results are summarized in Table 2. It is evident that the design is robust to PVT variations.

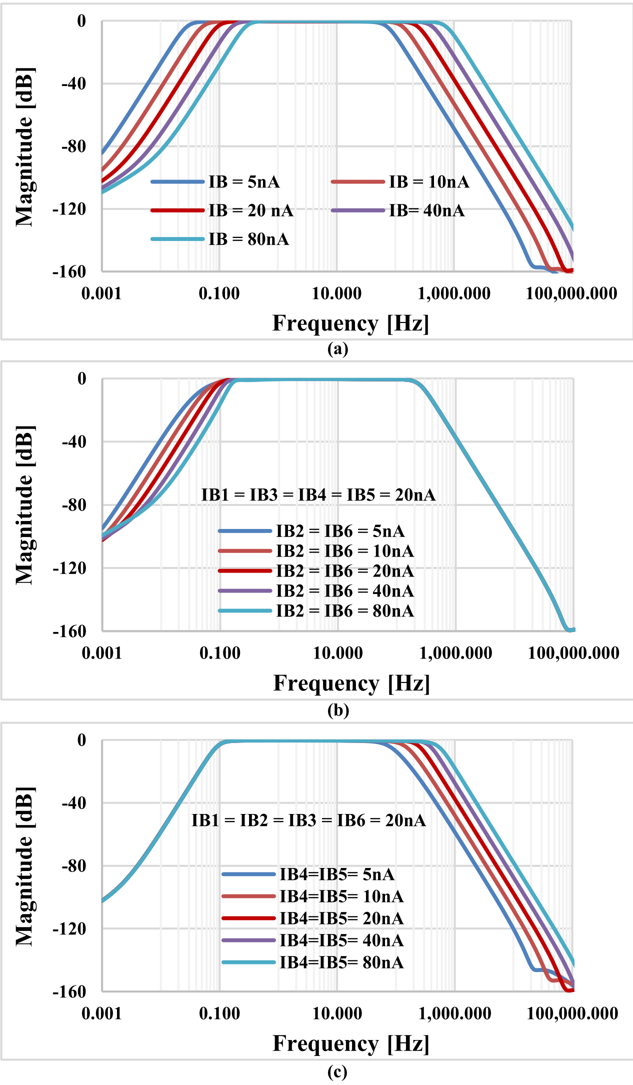

FIGURE 14. The frequency characteristic of the proposed filter for different I_B.

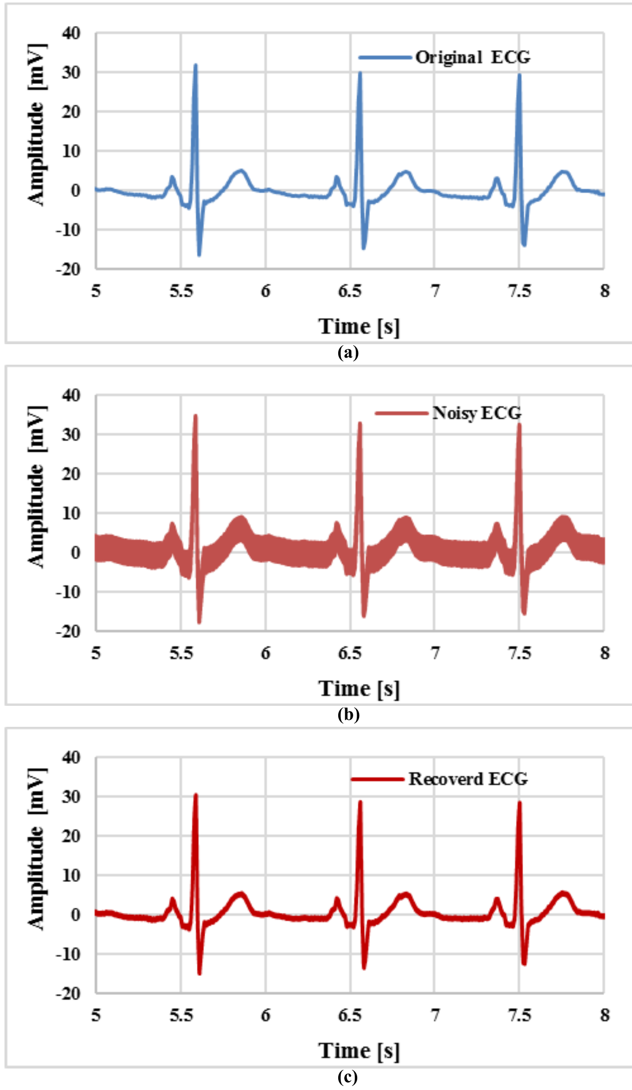

FIGURE 15. The original ECG signal (a), noisy ECG signal (b) and recovered ECG signal (c).

A performance comparison between this work and others sub-volts bulk-driven OTAs is shown in Tab. 3. It is evident that the proposed MI-OTA integrator offers a high dynamic range and wide tunability compared with other circuits.

The RLC BPF filter was designed for bandwidth (BW) = 0.1-250Hz, $\omega o = 2\pi\sqrt{\mathbf{0.1} \times \mathbf{250}} = 2\pi 5$ rad/s, $Q = 5/250 = 0.02$, R = 16.7MΩ, from above, the passive elements values of 3rd-order RLC filter are: $C_1 = 38.12$pF, $L_1 = 26.578$MH, $C_2 = 47.65$nF, $L_2 = 21.26$kH, $C_3 = 38.12$pF, $L_3 = 26.578$MH. The off-chip capacitors value of the3rd-order Butterworth filter based on MI-OTA are: $C_1 = C_3 = 38.12$pF, $C_{L1} = C_{L3} = 95.68$nF, $C_2 = 47.65$nF, $C_{L2} = 76.53$pF where $G_m = 60$ nS is given.

Note that the input voltage in Fig. 4 is applied to two positive inputs of first OTA, doubling its amplitude and achieving a passband voltage gain of 0 dB. The double amplitude of the input voltage is applied to the RLC filter in Fig. 3 (b) For the purpose of comparison.

Fig. 12 shows the frequency characteristic of the RLC and the proposed filter for $I_B = 20$nA. Both characteristics are in good agreement. The lower cut-off frequency of the proposed filter is 0.1 Hz while for upper cut-off frequency is 250 Hz. The impact of mismatch and process variation on the filter's frequency response is negligible as it is shown in Fig. 13.

The tuning capability of the filter BW for I_B from 5 nA till 80 nA is shown in Fig. 14. (a), while in (b) shows the capability of tuning the lower cut-off frequency and (c) the upper cut-off frequency. For Fig. 14 (a) the tuning range of the lower cut-off frequency is in range of 0.025 – 0.3 Hz while for upper cut-off frequency is in range of 57 – 670 Hz.

The performance of the filter was tested for ECG signal, where the original/clear ECG signal shown in Fig. 15(a), was mixed with low noise Motion Artifact (3mV @ 0.01Hz) and random noise at higher-frequency (3mV @ 500Hz), the result of the noisy ECG signal is shown in Fig. 15(b). This noisy ECG signal was applied to the input of the 3rd-order BPF

TABLE 4. Performance comparison between proposed filter and others.

Parameter	This work	2007 [7]	2018 [38]	2020 [39]
V_{DD}[V]	0.5	1	1	0.5
Vth [V]	0.5	0.7	0.5	0.5
Tech. [µm]	0.18	0.35	0.18	0.18
Order	3rd BP	3rd BP	5th LP	4th LP
Method	ladder	ladder	ladder	cascade of two biquad
Topology	single-end MI-OTA-C	single-end OTA-C	fully OTA-C	fully FSF
No. of device	6-OTA	8-OTA	6-OTA	–
f_c/BW [Hz]	250	670	50	200
DC gain [dB]	0	0	-6	-5.6
Input referred noise [µVrms]	198	50	100	91.9
DR [dB]	55.6	49	49.9	48.5
Power [nW]	160.8	68*	350	3.69
Low voltage capability V_{TH}/V_{DD} (100%)	100	70	50	100
Area (mm^2)	0.0528** (off chip cap.)	0.234	0.06 (off chip cap.)	0.074

* without bias circuits.
** Estimated.

(with AC characteristic shown in Fig. 12 (I_B = 20nA)), the recovered ECG signal is shown in Fig. 15(c).

In Table 4 the filter performance is compared with the 3rd-order BPF in [7], 5th order LPF in [38] and 4th order LPF based on flipped source follower (FSF) in [39]. It is evident that for 3rd-order BPF the device number of the proposed filter is 6-MI-OTAs whereas 8-OTAs are needed for [7]. The proposed filter also offers the best DR compared with BPF and LPF in [7], [38], [39]. Another advantage is the capability of fine-tuning of the lower, higher cut-off frequencies and the bandwidth of the filter.

V. CONCLUSION

This work presents a 0.5V multiple-input operational transconductance amplifier with high linearity performance and increased input voltage swing. Several design techniques to improve the linearity and the DC gain of the MI-OTA has been successful used. A 3rd-order Butterworth band-pass filter for ECG signal with 6-MIOTAs and 55.6 dB DR is presented. The attractive features of the MI-OTA and the filter have been confirmed by intensive simulation using the Cadence environment.

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FABIAN KHATEB received the M.Sc. and Ph.D. degrees in electrical engineering and communication from the Brno University of Technology, Czech Republic, in 2002 and 2005, respectively, and the M.Sc. and Ph.D. degrees in business and management from the Brno University of Technology, in 2003 and 2007, respectively. He is currently a Professor with the Department of Microelectronics, Faculty of Electrical Engineering and Communication, Brno University of Technology, and also with the Department of Information and Communication Technology in Medicine, Faculty of Biomedical Engineering, Czech Technical University in Prague. He holds five patents. He has authored or coauthored over 100 publications in journals and proceedings of international conferences. He has expertise in new principles of designing low-voltage low-power analog circuits, particularly biomedical applications. He is a member of the Editorial Board of *Microelectronics Journal*, *Sensors*, *Electronics*, and *Journal of Low Power Electronics and Applications*. He is an Associate Editor of IEEE Access, *Circuits, Systems and Signal Processing*, *IET Circuits, Devices & Systems*, and the *International Journal of Electronics*. He was a Lead Guest Editor for the Special Issues on Low Voltage Integrated Circuits and Systems on *Circuits, Systems, and Signal Processing* (2017), *IET Circuits, Devices & Systems* (2018), and *Microelectronics Journal* (2019). He was also a Guest Editor for the Special Issue on Current-Mode Circuits and Systems; Recent Advances, Design and Applications on *AEU—International Journal of Electronics and Communications* (2017).

TOMASZ KULEJ received the M.Sc. and Ph.D. degrees from the Gda sk University of Technology, Gda sk, Poland, in 1990 and 1996, respectively. He was a Senior Design Analysis Engineer at Chipworks Inc., Polish Branch, Ottawa, Canada. He is currently an Associate Professor with the Department of Electrical Engineering, Cz stochowa University of Technology, Poland, where he conducts lectures on electronics fundamentals, analog circuits, and computer-aided design. He has authored or coauthored over 80 publications in peer-reviewed journals and conferences. He holds three patents. His recent research interests include analog integrated circuits in CMOS technology, with emphasis to low voltage and low power solutions. He serves as an Associate Editor for the *Circuits, Systems, and Signal Processing* and *IET Circuits, Devices & Systems*. He was also a Guest Editor of the Special Issues on Low-Voltage Integrated Circuits and Systems on *Circuits, Systems, and Signal Processing* (2017), *IET Circuits, Devices & Systems* (2018), and *Microelectronics Journal* (2019).

MEYSAM AKBARI was born in Kermanshah, Iran, in 1988. He received the B.S. degree in electrical engineering from Islamic Azad University, Kermanshah, Iran, in 2010, the M.Sc. and Ph.D. degrees in electrical engineering from Shahid Beheshti University, Tehran, Iran, in 2014 and 2019, respectively. In September 2017, he joined the ICE-LAB, Aarhus University, Denmark, for a period of one year, as a Visiting Ph.D. Candidate to carry out part of his research study. He has been chosen as an Elite Student and Top Researcher by the Iran's National Elite Foundation for three consecutive years, from 2016 to 2019. Since November 2019, he has been a Postdoctoral Research Scholar with the Neuromorphic and Biomedical Engineering (NBME)-Lab, National Tsing Hua University, Hsinchu, Taiwan, where he is engaged in research on analog spiking neuromorphic circuits and systems. He has authored or coauthored over 40 publications in peer-reviewed journals and conferences. His research interests include analog integrated circuits and systems, data converters, neuromorphic circuits, and ultralow-power circuitry blocks for biomedical applications.

MONTREE KUMNGERN received the B.S.Ind.Ed. degree in electrical engineering from the King Mongkut's University of Technology Thonburi, Thailand, in 1998, the M.Eng. and D.Eng. degrees in electrical engineering from the King Mongkut's Institute of Technology Ladkrabang, Thailand, in 2002 and 2006, respectively. In 2007, he served as a Lecturer for the Department of Telecommunications Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, where he served as an Assistant Professor, from 2010 to 2017, and he is currently an Associate Professor. He has authored or coauthored over 200 publications in journals and proceedings of international conferences. His research interests include analog and digital integrated circuits, discrete-time analog filters, non-linear circuits, data converters, and ultra-low voltage building blocks for biomedical applications.