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0.8-V Supply Voltage Deep-Submicrometer Inversion-Mode $In_{0.75}Ga_{0.25}As$ MOSFET

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***Abstract*—We report the experimental demonstration of deep-submicrometer inversion-mode $In_{0.75}Ga_{0.25}As$ MOSFETs with ALD high-k Al_2O_3 as gate dielectric. In this letter, n-channel MOSFETs with 100–200-nm-long gates have been fabricated. At a supply voltage of 0.8 V, the fabricated devices with 200–130-nm-long gates exhibit drain currents of 232–440 $\mu A/\mu m$ and transconductances of 538–705 $\mu S/\mu m$. The 100-nm device has a drain current of 801 $\mu A/\mu m$ and a transconductance of 940 $\mu S/\mu m$. However, the device cannot be pinched off due to severe short-channel effect. Important scaling metrics, such as on/off current ratio, subthreshold swing, and drain-induced barrier lowering, are presented, and their relations to the short-channel effect are discussed.**

***Index Terms*—Atomic layer deposition, high-k, InGaAs, MOSFET.**

I. Introduction

THE CONTINUOUS device scaling and performance improvements required by the International Technology Roadmap for Semiconductors are faced with a grand challenge as conventional Si CMOS scaling comes to its fundamental physical limits. As several new technologies, such as high-k metal gate integration, nonplanar Si transistors, and strained-channel materials, have been developed to maintain Moore's law, tremendous efforts have been spent to look into those alternative channel materials "beyond Si," such as germanium and III–V compound semiconductors. Benefiting from their high electron mobility and velocity, III–V high-electron-mobility transistors or quantum-well transistors with In-rich InGaAs, InAs, or InSb channels have been demonstrated with superior device metrics such as transconductance, cutoff frequency, and gate delay [1]–[3]. However, the gate leakage of these transistors limits their applications in large-scale integrated circuits.

In the quest for perfect dielectrics for III–V semiconductors, significant progress has recently been made on inversion-type enhancement-mode InGaAs NMOSFETs, operating under the same mechanism as Si MOSFETs, using high-k gate dielectrics. The promising dielectric options include ALD Al_2O_3 [4]–[7], HfO_2 [7]–[9], HfAlO [7], [10], [11], ZrO_2 [12] and *in situ* molecular beam epitaxy (MBE) $Ga_2O_3(Gd_2O_3)$ [13]–[15]. Most recently, a record-high inversion current above 1 A/mm has been achieved for long-channel Al_2O_3/InGaAs MOSFETs [5]. In this letter, we present the experimental results of $In_{0.75}Ga_{0.25}As$ MOSFETs with gate lengths down to 100 nm and a supply voltage as low as 0.8 V. The on/off current ratio, subthreshold swing (SS), and drain-induced barrier lowering (DIBL) are affected by the short-channel effect.

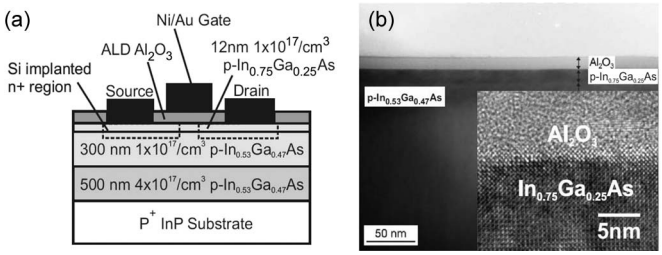

Fig. 1. (a) Cross section of an inversion-type enhancement-mode $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET. (b) TEM image of a similarly fabricated device with 10-nm Al_2O_3 after 750 °C RTA activation. (Inset) High-resolution TEM shows sharp $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface remaining after full device fabrication, including 750 °C RTA activation process.

II. Device Structure and Fabrication

Fig. 1(a) shows the cross section of an ALD $Al_2O_3/In_{0.75}Ga_{0.25}As$ MOSFET. A 500-nm p-type $4\times10^{17}/cm^3$ buffer layer, a 300-nm p-type $1\times10^{17}/cm^3$ $In_{0.53}Ga_{0.47}As$ layer, and a 12-nm strained p-type $1\times10^{17}/cm^3In_{0.75}Ga_{0.25}As$ channel were sequentially grown by MBE on a 2-in p^+-InP wafer. After surface cleaning and ammonia passivation, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30-nm-thick Al_2O_3 encapsulation layer was deposited at a substrate temperature of 300 °C. All patterns were defined by a Vistec VB-6 UHR electron-beam lithography (EBL) system. The source and drain regions of the MOSFETs were formed by selective implantation of 3×10^{13} cm^{-2} at 40-keV Si with the designed range of 43 nm and annealed at 650 °C or 750 °C for 10 s in N_2 for activation. Compared with the values in [5], relatively low implantation energy and dose were chosen here to avoid the penetration of implanted Si ions through the 280-nm-thick electron-beam resist used to protect the channel regions. After $(NH_4)_2S$ treatment for 10 min, another 5-nm Al_2O_3 was also grown by ALD after stripping away the encapsulation oxide layer. The ohmic source

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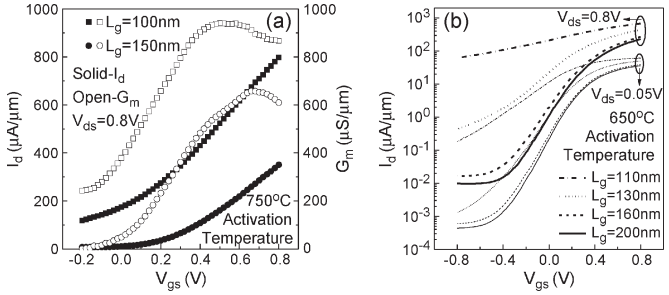

Fig. 2. (a) Transfer characteristics of $In_{0.75}Ga_{0.25}As$ MOSFETs with gate lengths of 100 and 150 nm. These devices are after 750 °C RTA activation. (b) Subthreshold characteristics of $In_{0.75}Ga_{0.25}As$ MOSFETs at $V_{ds} = 0.05$ and 0.8 V with gate lengths of 110, 130, 160, and 200 nm, respectively. The junction leakage current is significantly reduced by reducing the activation temperature from 750 °C to 650 °C.

TABLE I
MAJOR DEVICE PARAMETERS OF $In_{0.75}Ga_{0.25}As$ MOSFETs

L_g (nm)	I_{on} (μA/μm) (V_{ds}=0.8V)	G_m (μS/μm) (V_{ds}=0.8V)	SS (V_{ds}=0.05V) (mV/dec)	SS (V_{ds}=0.8V) (mV/dec)	DIBL (mV/V)	I_{on}/I_{off} (V_{ds}=0.8V)
110	685	700	430	1500		
120	568	704	273	653	956	
130	440	705	168	297	457	60
140	332	680	165	226	279	605
150	304	632	160	194	225	1.2 x 10^3
160	270	580	150	170	187	1.6 x 10^3
170	250	566	150	165	181	1.8 x 10^3
180	246	544	149	162	160	2.2 x 10^3
200	232	538	144	154	137	2.7 x 10^3

and drain contacts were made by electron-beam evaporation of AuGe/Ni/Au and annealing at 400 °C for 30 s in N_2. The gate electrode was made by electron-beam evaporation of Ni/Au. The fabricated MOSFETs have nominal gate lengths L_g's of 100, 110, 120, 130, 140, 150, 160, 170, 180, and 200 nm defined by the source–drain implant separation. The metal gates were designed to be 200 nm longer than the L_g with 100-nm extension on each side. The 100-nm extension guarantees the device structure shown in Fig. 1(a) since the EBL realignment accuracy is better than 50 nm. The device process is not self-aligned. Fig. 1(b) shows the transmission electron microscopy (TEM) images of the cross section of Al_2O_3/$In_{0.75}Ga_{0.25}As$/$In_{0.53}Ga_{0.47}As$ on a similarly finished device. The sheet resistance and contact resistance of the implanted source and drain regions are determined to be ∼300 Ω/square and ∼500 Ω · μm, respectively, by the transfer length method.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the transfer characteristics of 100- and 150-nm-gate-length $In_{0.75}Ga_{0.25}As$ MOSFETs. The maximum supply voltage V_{DD} is 0.8 V. At the gate–source voltage $V_{gs} = V_{ds} = 0.8$ V, the measured on-currents (I_{on}'s) are 801 and 354 $\mu A/\mu m$ for 100- and 150-nm devices. The 100-nm device cannot be turned off at any gate bias with drain current of 170 $\mu A/\mu m$ at $V_{ds} = 0.8$ V and $V_{gs} = 0$ V, suggesting that the p-doped channel region is punched through by the implanted n^+ source and drain and/or that the source/drain is excessively deep implanted. The punchthrough effect becomes less severe for devices with gate lengths of 130 nm or longer because their L_g's are more than twice the depletion width in the p-doped channel region from the n^+ source and drain. Their L_g's are also exactly three times or more than the designed source/drain implantation range of 43 nm. The 130–200-nm devices are operated in enhancement mode with the threshold voltage V_T of 0.14–0.2 V, measured from the transfer characteristics in the linear region at drain–source voltage $V_{ds} = 0.05$ V. The maximum extrinsic transconductances G_m's are 940 $\mu S/\mu m$ for a 100-nm device and 660 $\mu S/\mu m$ for a 150-nm device. To the best of the authors' knowledge, these values are among the highest G_m's ever reported for surface-channel III–V MOSFETs [5], [15]. The intrinsic G_m for a 100-nm device is estimated to be 1.77 $mS/\mu m$ since the measured contact resistance is approximately 500 Ω · μm. Compared with that in [5], G_m is increased to 660 from 350 $\mu S/\mu m$ by reducing the Al_2O_3 thickness from 10 to 5 nm and shrinking the gate length from 0.4 μm to 150 nm. The observed linear scaling of G_m and I_{on} versus L_g between 0.4 and 40 μm does not sustain any longer in the deep-submicrometer region. To maintain the ON-state device performance at low-power operation, more aggressive reduction of the effective oxide thickness is needed.

Fig. 2(b) shows the subthreshold characteristics of drain current, I_d versus V_{gs}, for four representative devices with 110-, 130-, 160-, and 200-nm gate lengths at $V_{ds} = 0.8$ and 0.05 V. The devices with 130-nm or shorter gate length show severe short-channel effect, as discussed previously. Strictly speaking, at $V_{ds} = 0.8$ V and $V_{gs} = 0$, only the 200-nm device is really turned off if the 1 $\mu A/\mu m$ metric is used. Shallow junctions or more sophisticated halo implantations are needed to fabricate sub-200-nm-surface-channel $In_{0.75}Ga_{0.25}As$ MOSFETs with acceptable OFF-state performance. The saturation of the decrease of I_d at $V_{gs} < 0$ is due to the substrate leakage current induced from the reversely biased drain junction [16]. The junction leakage is significantly reduced by reducing the implantation activation temperature from 750 °C to 650 °C. The similar effect was also reported in [17]. Meanwhile, ON-state performance is only slightly degraded by reducing the activation temperature from 750 °C to 650 °C. The typical gate leakage current for these devices is below 1 $pA/\mu m$ at -0.8 V $< V_{gs} < 0.8$ V and $V_{ds} = 0.8$ V, which is about eight orders of magnitude lower than the drain current. The 5-nm Al_2O_3 leakage current density is $< 10^{-4}$ A/cm^2 at the device operation biases.

Table I summarizes the I_{on}, G_m, and the scaling metrics of SS, DIBL, and I_{on}/I_{off} as functions of L_g obtained from I_d. All these devices were activated at 650 °C. I_{on}/I_{off} is chosen as $I_{on}(V_{ds} = 0.8\ V, V_{gs} = V_T + 2/3V_{DD})/I_{off}(V_{ds} = 0.8\ V, V_{gs} = V_T - 1/3V_{DD})$ with 1 $\mu A/\mu m$ metric for V_T and 0.8V for V_{DD} [2], [18]. It can be seen that SS and DIBL increase and I_{on}/I_{off} decreases with decreasing L_g. The values start to fall apart dramatically at $L_g = 130$ nm or shorter, indicating that severe short-channel effect occurs. These scaling metrics could be further improved by nonplanar geometry, junction engineering, and better interface quality. With minimum

short-channel effects at $L_g = 200$ nm, SS ~ 100 mV/decade is obtained from I_s. It is smaller than the value obtained from I_d. The SS from I_s is more intrinsic without the junction leakage degradation. Without considering the SS degradation by short-channel effects, the upper limit of the interface trap density $D_{\rm it}$ is estimated to be $4 \times 10^{12}/{\rm cm}^2 \cdot {\rm eV}$ for the present devices from the m factor, defined as 60 mV/decade $\cdot (1 + C_{\rm it}/C_{\rm ox})$. Here, $C_{\rm it} = qD_{\rm it}$ is the interface trap capacitance, and $C_{\rm ox}$ is the oxide capacitance.

IV. Conclusion

Inversion-mode $In_{0.75}Ga_{0.25}As$ MOSFETs with gate lengths of 100–200 nm were demonstrated experimentally. At a supply voltage of 0.8 V, the fabricated devices with 200–130-nm-long gates exhibited drain currents of 232–440 μA/μm and transconductances of 538–705 μS/μm, respectively. The 100-nm device has a transconductance as high as 940 μS/μm, although the device cannot be pinched off due to severe short-channel effect. With better demonstrated ON-state performance of inversion-mode MOSFETs on In-rich InGaAs channels, more work is needed to study the fundamental limitations of the narrow energy gap of In-rich InGaAs and the OFF-state performance related with interface trap densities.

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