Nanoscale Research Letters

NANO EXPRESS

Open Access

1.3 kV Vertical GaN-Based Trench MOSFETs on 4-Inch Free Standing GaN Wafer

Wei He[1], Jian Li[1], Zeliang Liao[1], Feng Lin[1], Junye Wu[1], Bing Wang[1], Maojun Wang[2], Nan Liu[3], Hsien-Chin Chiu[4], Hao-Chung Kuo[5], Xinnan Lin[6], Jingbo Li[7] and Xinke Liu[1*]

Abstract

In this work, a vertical gallium nitride (GaN)-based trench MOSFET on 4-inch free-standing GaN substrate is presented with threshold voltage of 3.15 V, specific on-resistance of 1.93 mΩ·cm^2, breakdown voltage of 1306 V, and figure of merit of 0.88 GW/cm^2. High-quality and stable MOS interface is obtained through two-step process, including simple acid cleaning and a following $(NH_4)_2S$ passivation. Based on the calibration with experiment, the simulation results of physical model are consistent well with the experiment data in transfer, output, and breakdown characteristic curves, which demonstrate the validity of the simulation data obtained by Silvaco technology computer aided design (Silvaco TCAD). The mechanisms of on-state and breakdown are thoroughly studied using Silvaco TCAD physical model. The device parameters, including n$^-$-GaN drift layer, p-GaN channel layer and gate dielectric layer, are systematically designed for optimization. This comprehensive analysis and optimization on the vertical GaN-based trench MOSFETs provide significant guide for vertical GaN-based high power applications.

Keywords: Free standing gallium nitride (GaN), Trench MOSFET, GaN MOSFET, Breakdown, TCAD

Introduction

Wide-bandgap GaN-based power devices have been regarded as the great potential candidates for the next generation efficient power electronics and compact power systems, owing to the superior material properties such as high electron mobility, large breakdown field strength and high thermal stability [1–5]. Compared with high electron mobility transistors (HEMTs) [6–11] and current aperture vertical electron transistors (CAVETs) [12–15], GaN-based trench metal oxide semiconductor field effect transistors (MOSFETs) [16–18] are more competitive to realize intrinsically normally-off operation with higher current density, lower specific on-resistance ($R_{on,sp}$) and lower current collapse. Moreover, GaN-based trench MOSFETs possess relatively simple manufacturing process and do not need the regrowth of AlGaN/GaN layers [19, 20].

The development of lateral GaN-based MOSFETs has approximately come to saturation, due to the breakdown voltage (V_{BR}) limited by the length of lateral drift region. Although the growth of length can increase V_{BR}, the size of device enlarges, leading to reduction of the effective current density per unit chip area. In contrast, vertical GaN-based devices have been fully advanced. Under the same required V_{BR} and amperage rating, smaller size and less cost can be realized on vertical GaN-based MOSFETs when make a contrast with lateral GaN MOSFETs [21]. In comparison with Si, Sapphire, SiC and Diamond substrate, the MOSFETs on free-standing GaN substrate can greatly reduce the probability of the high-density trap states and non-linearity contributed by lattice mismatch while operating at high power [22].

More studies have made great progress in V_{BR}, $R_{on,sp}$ and device reliability for GaN vertical MOSFETs in recent years. Floating P-body had been introduced in the N$^-$-GaN drift region to form "P-body/N-drift" junction

*Correspondence: xkliu@szu.edu.cn
[1] College of Materials Science and Engineering, College of Electronics and Information Engineering, College of Physics and Optoelectronic Engineering, Institute of Microelectronics (IME), Shenzhen University, Shenzhen 518060, China
Full list of author information is available at the end of the article

via TCAD simulation for the improvement of V_{BR} of the enhancement-mode vertical GaN MOSFET [23]. Vertical GaN interlayer-based trench MOSFET (OG-FET) on a large-area in-situ oxide performed threshold voltage (V_{th}) of 2.5 V, $R_{on,sp}$ of 0.98 mΩ·cm^2 and V_{BR} of 700 V with regrown 10-nm unintentional-doped-GaN interlayer as the channel and 50-nm in-situ Al_2O_3 as the gate dielectric [24]. Vertical GaN trench-MOSFETs with MBE regrown UID-GaN channel were investigated, which avoided the need to reactivate the buried body p-GaN and promised the same benefit on channel mobility compared to the MOCVD regrowth [25]. The device characteristics had been improved for vertical GaN trench MOSFETs by using Silvaco ATLAS 2-D simulation in order to get the best trade-off between V_{BR} and $R_{on,sp}$ [26].

In this work, we present vertical GaN-based trench gate MOSFETs (GaN TG-MOSFETs) on 4-inch free-standing GaN substrate exhibiting normally off operation for high power applications. We use Silvaco TCAD to simulate the structure and performance of GaN TG-MOSFETs based on semiconductor physics and advanced process. The simulation results obtained by Silvaco ATLAS simulation are consistent well with experiment data on the characteristic curves of transfer, output, and breakdown voltage, respectively. The device parameters are researched comprehensively by using TCAD for providing guide in actual fabrication and optimization. The design of the parameters includes the thickness of n$^-$-GaN drift body layer (L_{drift}), n$^-$-GaN drift trench region (L_{trench}), p-GaN channel layer ($L_{channel}$) and gate dielectric layer ($L_{dielectric}$). The doping density of p-GaN channel layer (N_a) and n$^-$-GaN Drift layer (N_d) are included.

Experiment and Simulation Approach

High-quality, large-size and less-expensive GaN substrates are crucial for the progress of vertical GaN power devices. More techniques were proposed to optimize the growth of bulk GaN crystals, such as halide vapor phase epitaxy (HVPE), high nitrogen pressure solution (HNPS), basic and acidic ammonothermal, Na-flux method and near atmospheric pressure solution growth [27, 28]. HVPE is the main method for mass fabrication of GaN crystals, due to its high grow rate, high purity, high process repeatability and easy doping. The transparent 4-inch freestanding GaN wafer grown by HVPE with 13 points position for test is shown in Fig. 1a. We utilized a 420-μm-thick free-standing n$^+$-GaN substrate in the device fabrication with the average mobility of 614 cm^2·V^{-1}·s^{-1} and the average dislocation density of 1.94×10^6 cm^{-2} at the top surface, as determined by contactless Hall measurement and cathodoluminescence (CL). The test result and CL image of the epitaxial layer are presented in Fig. 1b, c, respectively.

The fabrication process of the GaN TG-MOSFETs discussed in this work is shown in Fig. 1d. The epitaxial growth began with 12-μm lightly doped 8.0×10^{15} cm^{-3} n$^-$-GaN as the drift region. A 1.0-μm heavily doped p-GaN with a doping density of 1.0×10^{18} cm^{-3} was deposited as the channel region. Thereafter, a 0.2-μm-thick heavily doped n$^+$-GaN with a doping density of 3×10^{18} cm^{-3} was grown as the source contact layer. The device fabrication process started with the formation of 0.2-μm-deep vertical trench and 1.7-μm-deep vertical mesa for p-body and gate contacts by using Cl_2-based gases in reactive ion etching (RIE) at 15 W power, respectively. A 16-nm-thick Al_2O_3 film was deposited by atomic layer deposition (ALD) as gate dielectric. High-quality and stable MOS interface with low-density trap states is essential for GaN TG-MOSFETs. A two-step process, including simple acid cleaning and a following $(NH_4)_2S$ passivation, was required to drastically reduce the interface states and border traps [29]. The source and drain electrodes with Ti/Al were annealed at 550 °C for 5 min in N_2 ambient for ohmic contacts. The gate and p-body electrodes were composed of Ti/Au and Palladium, respectively. A 400-nm-thick SiO_2 film was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivated isolation mesa. Finally, field plate termination was employed to impair the peak electric field crowded at the edge of PN junction around the isolation mesa. The Al-based field plate was connected to the source electrode.

The schematic of energy band lined-up at the Al_2O_3/GaN heterointerface in Fig. 1e. The forbidden band of GaN was exactly contained in that of Al_2O_3, where the deviations of the conduction band and valence band were 3.38 eV and 0.22 eV, respectively. It revealed that Al_2O_3 could maintain excellent insulation with GaN for electrons, which greatly reduced gate leakage current and improved device performance. The 3D drawing structure and parameters needed for optimization are shown in Fig. 1f. Figure 1g shows the micrograph of the device. The hexagonal crystal structure contained the outward vertical C axis, three horizontal axes a_1, a_2 and a_3, and crystal planes in various directions.

The physical simulation models concerned for simulation were the parallel electric field-dependent mobility model, concentration-dependent mobility model, low field mobility model, Shockley–Read–Hall recombination model, Auger recombination model, impact ionization model, energy bandgap narrowing model and trap model [26, 29–31]. The main physical models and parameter values for simulation are shown in Table 1.

For GaN simulation, Si donors and Mg acceptors were not completely ionized at room temperature since their high activation energies, especially for Mg-doped

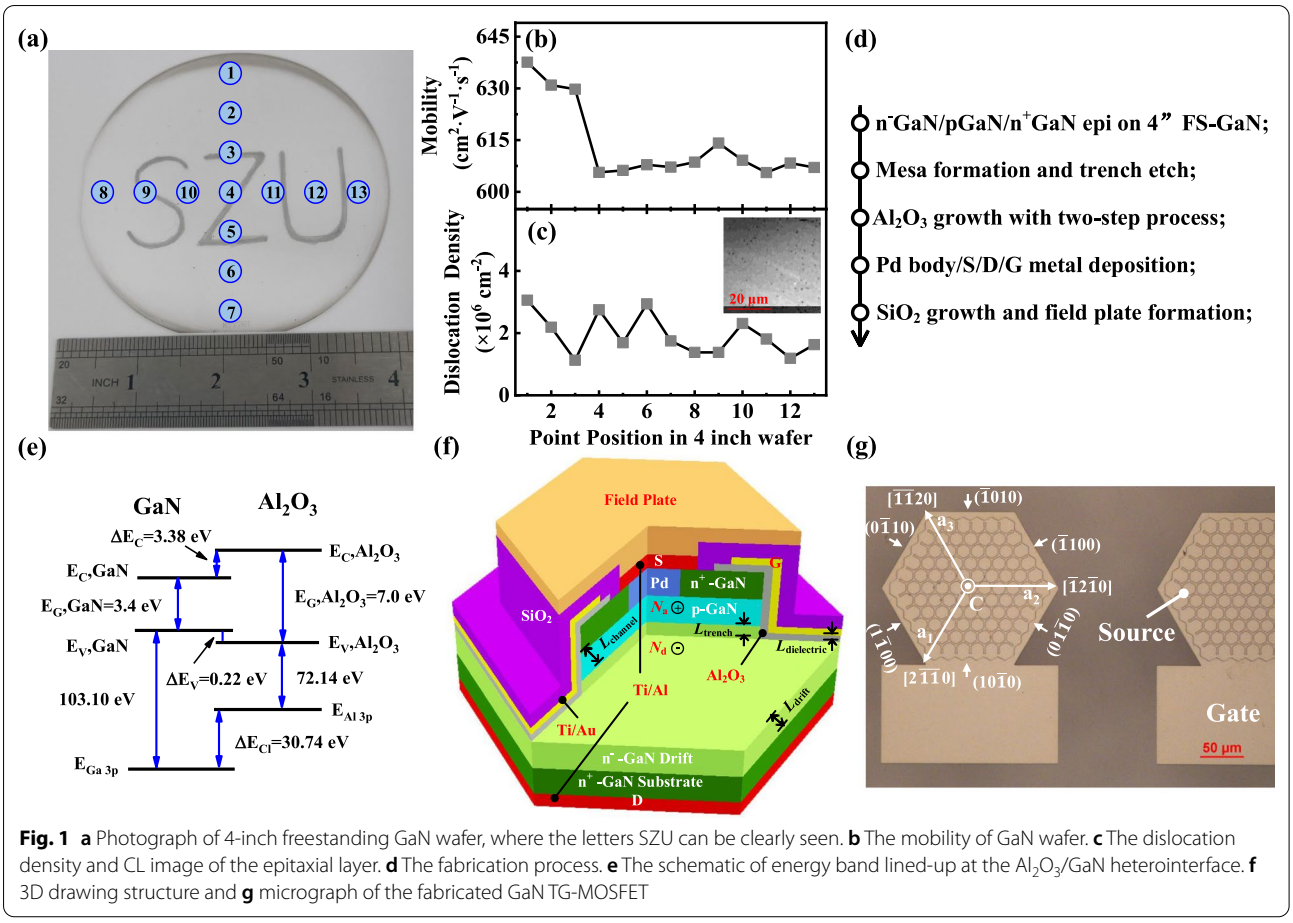

Fig. 1 **a** Photograph of 4-inch freestanding GaN wafer, where the letters SZU can be clearly seen. **b** The mobility of GaN wafer. **c** The dislocation density and CL image of the epitaxial layer. **d** The fabrication process. **e** The schematic of energy band lined-up at the Al_2O_3/GaN heterointerface. **f** 3D drawing structure and **g** micrograph of the fabricated GaN TG-MOSFET

p-type GaN [32–34]. Thus, according to Fermi–Dirac distribution, the incomplete ionization model was incorporated in the simulation for accurately reproducing the breakdown voltage. The ionized donors and acceptors impurity concentrations were given as follows

$$N_D^+ = \frac{N_D}{1 + g_D \cdot \exp\left(\frac{\varepsilon_{Fn} + E_{D,0} - \theta_n \cdot \sqrt[3]{N_D} - E_C}{KT}\right)} \quad (1)$$

$$N_A^- = \frac{N_A}{1 + g_A \cdot \exp\left(\frac{E_V + E_{A,0} - \theta_p \cdot \sqrt[3]{N_A} - \varepsilon_{Fp}}{KT}\right)} \quad (2)$$

Here, g_D and g_A are the appropriate degeneracy factors for conduction and valence bands. $E_{D,0}$ and $E_{A,0}$ are the donor and acceptor ionization energy at very low doping levels. θ_n and θ_p are constants accounting for geometrical factors as well as for the properties of the material. Low field mobility model is the result of fitting Caughey Thomas like model to Monte Carlo data [26, 32]. It can be defined as

$$\mu_{(n/p)}(T,N) = \mu_{1(n/p)} \cdot (T/300)^{\beta_{1(n/p)}} + \frac{(\mu_{2(n/p)} - \mu_{1(n/p)}) \cdot (T/300)^{\beta_{2(n/p)}}}{1 + \left[\frac{N}{N_{ref\,(n/p)} \cdot (T/300)^{\beta_{3(n/p)}}}\right]^{\rho_{(n/p)} \cdot (T/300)^{\beta_{4(n/p)}}}} \quad (3)$$

where μ_1, μ_2 are the minimum and maximum mobility, ρ, β_1, β_2, β_3, β_4, are all temperature dependent fitting parameters, N_{ref} is the reference doping level and N is the donor concentration.

The Poisson's equations and Current continuity equation were essential for the analysis of simulation [35]. As in semiconductor PN junction, avalanche breakdown occurred when the impact ionization integral reached unity

$$I_n = \int \alpha_n \exp\left(\int^w \alpha_p - \alpha_n \mathrm{d}v\right) \mathrm{d}w = 1 \quad (4)$$

where I_n is the impact ionization integral of electrons. The utilized ionization rate model of electrons and holes

Table 1 The main model and parameter values for TCAD simulation

Model	Parameter	Value	Unit
Incomplete ionization	g_D	2	–
	$E_{D,0}$	0.017	eV
	θ_n	3.4×10^{-9}	eV·cm
	g_A	2	–
	$E_{A,0}$	0.16	eV
	θ_p	3.14×10^{-8}	eV·cm
Low field mobility	μ_{1n}	250	$cm^2/V{\cdot}s$
	μ_{2n}	1150	$cm^2/V{\cdot}s$
	N_{refn}	2×10^{17}	cm^{-3}
	ρ_n	1.0	–
	μ_{1p}	10	$cm^2/V{\cdot}s$
	μ_{2p}	170	$cm^2/V{\cdot}s$
	N_{refp}	3×10^{17}	cm^{-3}
	ρ_p	2.0	–
Impact ionization	*AN*	2.1×10^9	cm^{-1}
	BN	3.4×10^7	cm^{-1}
	AP	5.4×10^6	V/cm
	BP	1.8×10^7	V/cm
	BETAN	1.0	–
	BETAP	1.0	–

are variation of the classical Chynoweth model [36], which based upon the following expressions,

$$\alpha_n = AN \cdot \exp\left[-\left(\frac{BN}{E}\right)^{BETAN}\right] \tag{5}$$

$$\alpha_p = AP \cdot \exp\left[-\left(\frac{BP}{E}\right)^{BETAP}\right] \tag{6}$$

Here, E is the electric field in the direction of current flow at the p-GaN channel layer in the structure. Various group has reported impact ionization coefficients to accurately predict the breakdown of GaN power devices in recent years [37–41]. The coefficients *AN*, *AP*, *BN*, *BP*, *BETAN* and *BETAP* of the impact ionization model in this work were determined by referring to the experiments above.

In this study, the work was mainly carried out by TCAD. The data obtained by simulation had been calibrated with the result of experiment on GaN TG-MOSFET shown in the third part. The comprehensive analysis and optimization design on L_{drift}, L_{trench}, $L_{dielectric}$, $L_{channel}$, N_a and N_d of devices were demonstrated in the fourth part, respectively.

Results and Discussion

The initial device parameters of simulation model were set as follows: $N_d = 8.0 \times 10^{15}$ cm^{-3}, $N_a = 1.0 \times 10^{18}$ cm^{-3}, $L_{drift} = 12$ μm, $L_{trench} = 0.5$ μm, $L_{channel} = 1.0$ μm, and $L_{dielectric} = 16$ nm. The interface state could capture the free electrons in the channel and formed the negative interface charge, leading to the decrease of the number of free electrons and the increase of $R_{on,sp}$. A low density of interface state was beneficial to reduce $R_{on,sp}$ and switch loss. The interface state in the simulation was defined as 10^{11} $cm^{-2}{\cdot}eV^{-1}$ by referring to the previous work [25]. The characteristic curves of transfer, output, and breakdown of GaN TG-MOSFET via experiment (Exp) and simulation (Sim) are shown in Fig. 2, respectively. This simulation results were consistent well with the data of experiment, which could verify the validity of the results obtained by simulation and calibrate the simulation model.

Figure 2a shows the I_D–V_G characteristics at $V_{DS} = 0.5$ V. Several extraction methods were used to determine the value of V_{th} from the measured I_D–V_G characteristics [42]. Normally-off operation with V_{th} (defined at $I_{DS} = 1$ μA/mm) of 3.15 V was observed. Figure 3a shows the current could not be conducted between the source and drain, since the channel was not yet formed a conduction path. In Fig. 3b, the inversion layer of electron was effectively generated in the channel only when $V_{GS} > V_{th}$, hence generating the drain-to-source current. The distributions of energy band along line A and line B during off-state and on-state are shown in Fig. 3c and Fig. 3d, respectively. From off-state to on-state, the energy of conduction band (CB) obviously reduced until closing to the Quasi-Fermi level (QFL). Therefore, electrons could easily jump to CB and generate conduction current. Figure 2b exhibits the output I–V characteristics at $V_{GS} = 0$ V, 5 V, 10 V, 15 V and 20 V, respectively. The $R_{on,sp}$ estimated from the linear region was 1.93 $m\Omega{\cdot}cm^2$ at $V_{DS} = 0.5$ V and $V_{GS} = 20$ V.

Figure 2c demonstrates the off-state I–V characteristics measured at $V_{GS} = 0$ V. This work achieved the hard breakdown V_{BR} of 1306 V when $I_{DS} > 50$ mA/cm^2 from experiment, while the V_{BR} of simulation reached 2278 V. The insufficient activation of the Mg dopant existing in the p-GaN was considered as the reason for making the discrepancy in V_{BR} between experiment and simulation. Finally, the corresponding figure of merit (FOM) obtained were 0.88 GW/cm^2 and 1.68 GW/cm^2 by experiment and simulation, respectively.

Two breakdown mechanisms, namely punch-through breakdown and avalanche breakdown, existed in the device, which were dominated by the product of $L_{channel}$ and N_a ($L_{channel} \cdot N_a$) of p-GaN. Taking the

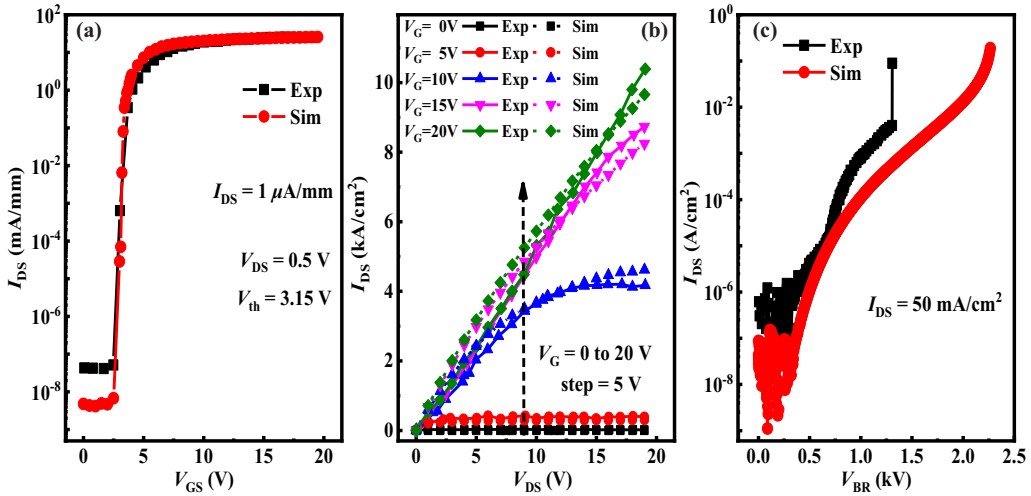

Fig. 2 **a** Transfer *I–V* characteristics (I_D–V_G) at V_{DS} = 0.5 V. **b** Output *I–V* characteristics (I_D–V_D) at V_{GS} = 0 V, 5 V, 10 V, 15 V and 20 V, respectively. **c** Off-state *I–V* characteristics measured at V_G = 0 V for fabricated GaN TG-MOSFET

$N_a = 2.0 \times 10^{17}$ cm^{-3} and various $L_{channel}$ for example by simulation as shown in Fig. 4a. Punch-through breakdown would occur when $L_{channel} \cdot N_a$ was lower than a certain value, such as $L_{channel} = 0.6$ μm and $N_a = 2.0 \times 10^{17}$ cm^{-3} in Fig. 4a. However, it would be changed to avalanche breakdown when $L_{channel} \cdot N_a$ was high enough, such as $L_{channel} = 0.8$ μm and $N_a = 2.0 \times 10^{17}$ cm^{-3}. Moreover, the breakdown mechansims were studied in detail from the expansion of depletion region (DR), distributions of electric field and impact gen rate (IGR). Figure 4b shows the schematic of the device. Figures 4c–f and 5a–f show the expansion of DR of device with $L_{channel} = 0.4$ μm and $L_{channel} = 1.2$ μm, respectively. As drain voltage enlarged, the DR extended continually and was oriented toward the drain, which offered strong current blocking capability and suppressed the permature breakdown.

Punch-through breakdown occured in the device with $N_a = 2.0 \times 10^{17}$ cm^{-3} and $L_{channel} = 0.4$ μm when $V_{DS} > 1000$ V for $L_{channel} \cdot N_a$ was low. The EF along line A is shown in Fig. 4g. The peak EF was ~ 2.3 MV/cm and did not reach the critical electric field strength value of GaN. A high potential barrier prevents current flow. The barrier between source and drain significantly reduced for the expansion of DR when V_{DS} increased. Since the current was an exponential function of barrier height, the current increased rapidly once the punch-through condition was satisfied. The number of electrons injected from source region into channel had greatly increased through EF. Large current flowed from drain directly to source as shown in Fig. 6a. In Fig. 6b, the peak IGR was located at the reverse biased PN junction between p-GaN and n$^-$-GaN drift region as shown in the red circle.

Avalanche breakdown happened in the device with $N_a = 2.0 \times 10^{17}$ cm^{-3} and $L_{channel} = 1.2$ μm when $V_{DS} > 2000$ V for the $L_{channel} \cdot N_a$ was high. The EF along line B is shown in Fig. 5g. The peak EF was ~ 3.45 MV/cm and closed to the critical electric field of 3.3 MV/cm of GaN. The energy of electrons and holes was enhanced by EF when they pass through the space charge region. Since they collided with electrons of atoms in DR, large numbers of new electron–hole pairs were generated, causing the avalanche effect. Large electron and hole current were produced as shown in Fig. 6c. The electron current mainly flowed to drain, while hole current flowed to the source along p-GaN region. In the red circle of Fig. 6d, the peak IGR was located at the gate corner. It implied that the breakdown characteristic was similar to that of PN junction diode as long as punch-through did not occur. The simulation showed that device could achieve avalanche and avoid punch-through breakdown with enough value of $L_{channel} \cdot N_a$. The effect of various N_a on the breakdown mechanism was similar to that of $L_{channel}$.

Analysis and Performance Evaluation

This simulation focused on studying the effects of various device parameters and obtaining the scheme of optimization design. Firstly, the thickness and doping density of n$^-$-GaN drift layer were researched with different initial values. Then, we analysed the thickness and doping density of p-GaN channel layer based on the optimal parameters of n$^-$-GaN drift layer. Finally, the impact of the thickness of gate dielectric was thoroughly studied.

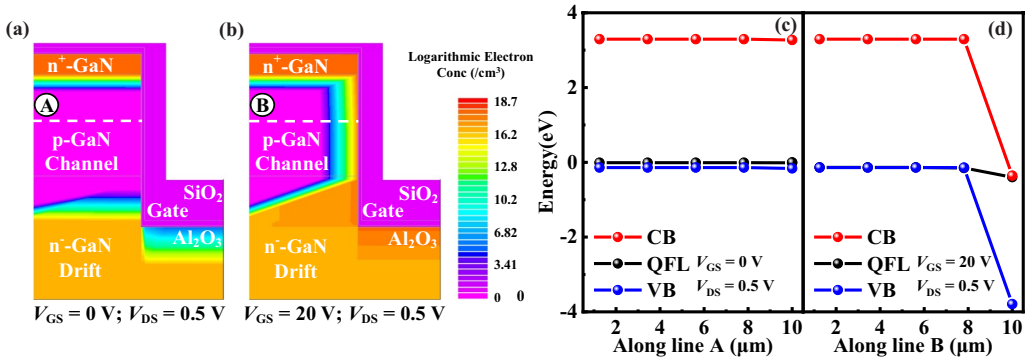

Fig. 3 Electron concentration distributed at **a** $V_{GS}=0$ V, $V_{DS}=0.5$ V (off-state) and **b** $V_{GS}=20$ V, $V_{DS}=0.5$ V (on-state). The energy band distributed during **c** off-state and **d** on-state

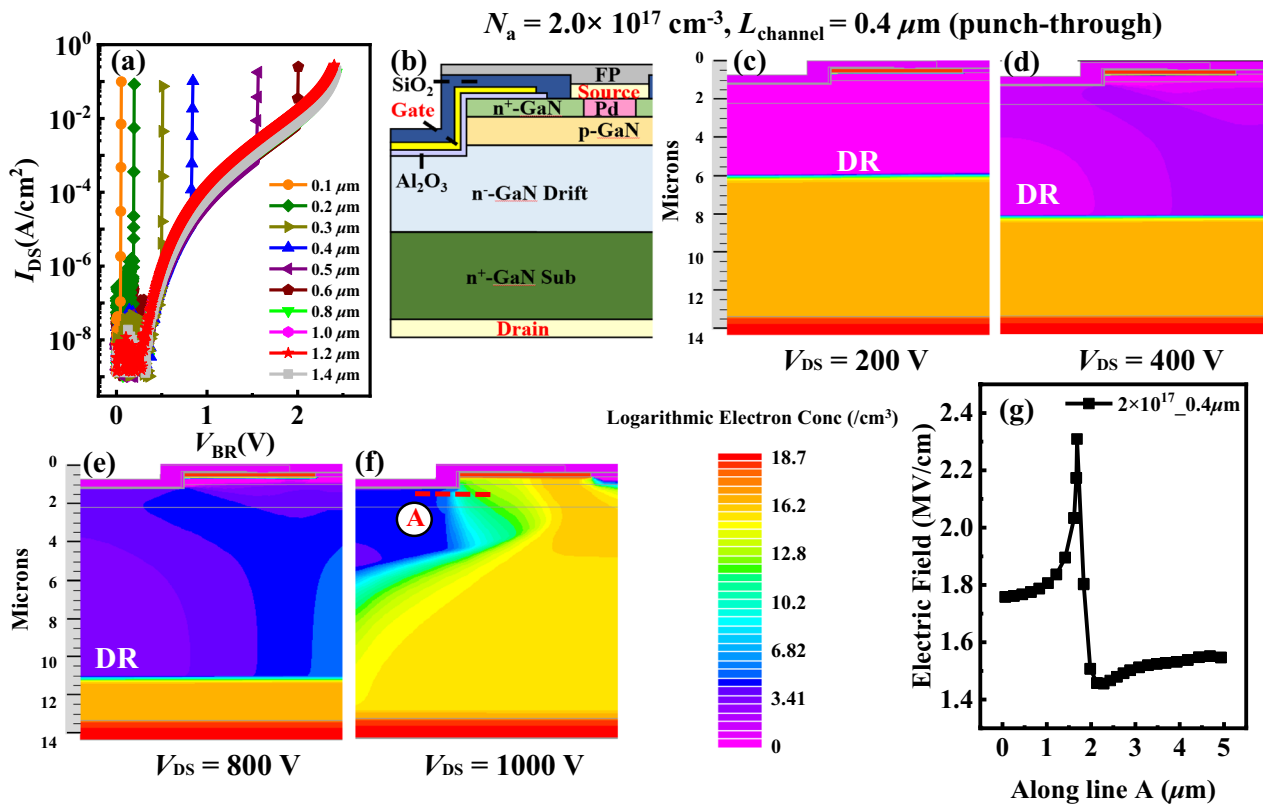

Fig. 4 **a** Breakdown curves under $N_a=2.0\times10^{17}$ cm^{-3} and various $L_{channel}$. **b** Schematic of GaN TG-MOSFET. **c**–**f** Depletion region at different reverse bias under $N_a=2.0\times10^{17}$ cm^{-3} and $L_{channel}=0.4$ μm, including $V_{DS}=200$ V, 400 V, 800 V and 1000 V. **g** Electric Field distributed along line A at $V_{DS}=1000$ V

All the changes of the above parameters were discussed within a reasonable range. The power figure of merit $FOM=V_{BR}{}^2/R_{on,sp}$ and V_{th} could be used as a criterion for optimization.

Analysis the Influence of n⁻-GaN Drift Layer

As shown in Fig. 7a, V_{BR} increased and saturated at a certain value as L_{drift} increased with different initial conditions. The phenomenon that DR extended and saturated with the growth of L_{drift} caused the V_{BR} increased and saturated. Conversely, V_{BR} decreased with the growth of N_d. The situation was equivalent to the effect of the doping

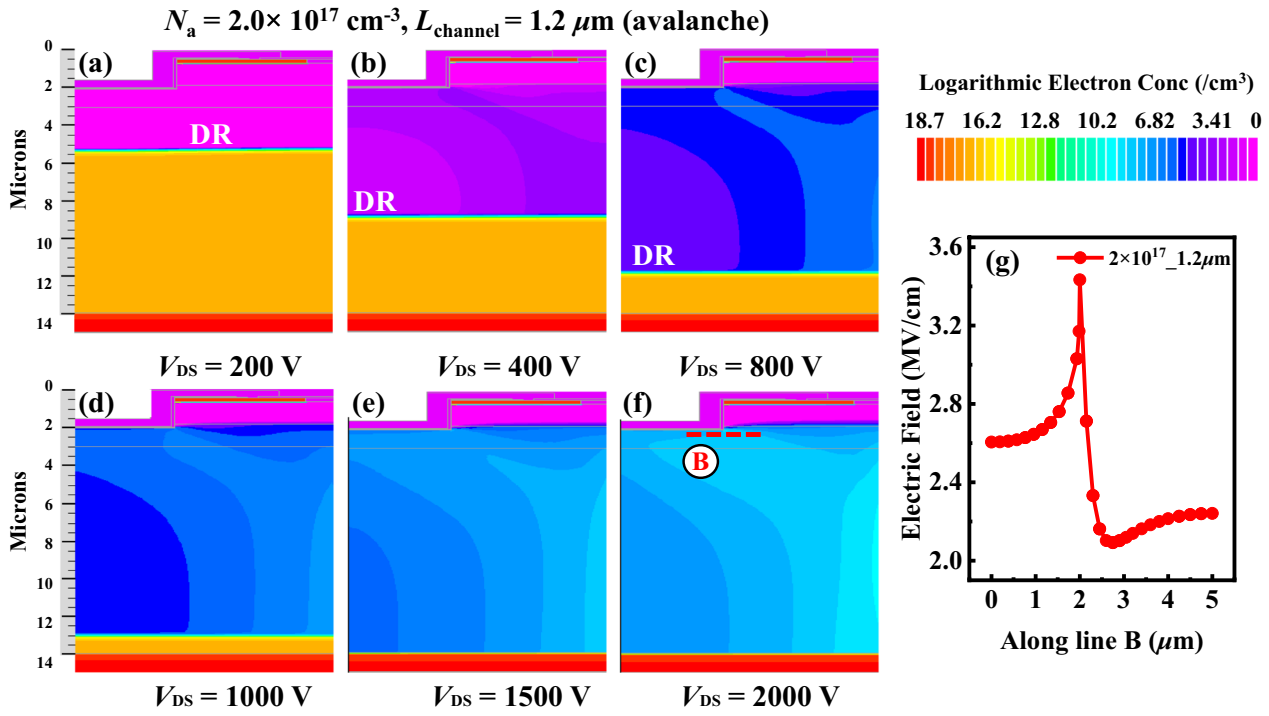

Fig. 5 **a**–**f** Depletion region at different reverse bias under $N_a = 2.0 \times 10^{17}$ cm^{-3} and $L_{channel} = 1.2$ μm, including $V_{DS} = 200$ V, 400 V, 800 V, 1000 V, 1500 V and 2000 V. **g** Electric Field distributed along line B at $V_{DS} = 2000$ V

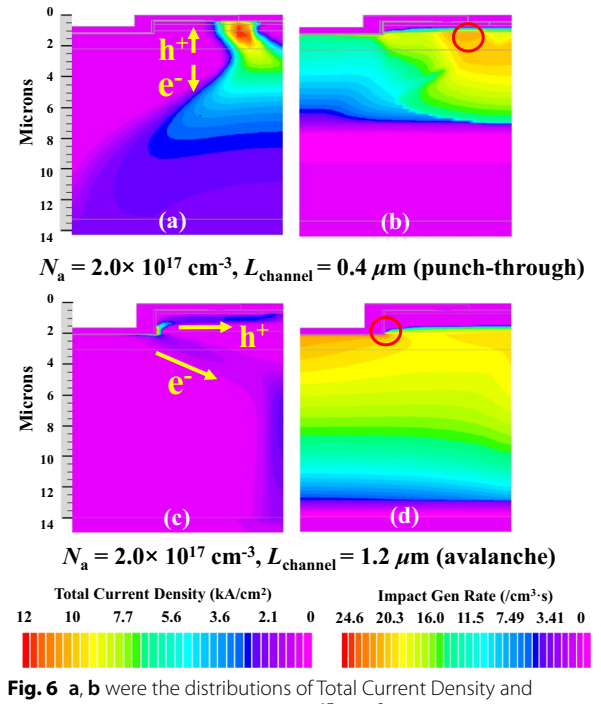

Fig. 6 **a**, **b** were the distributions of Total Current Density and Impact Gen Rate under $N_a = 2.0 \times 10^{17}$ cm^{-3} and $L_{channel} = 0.4$ μm, respectively. **c**, **d** were the distributions of Total Current Density and Impact Gen Rate under $N_a = 2.0 \times 10^{17}$ cm^{-3} and $L_{channel} = 1.2$ μm, respectively

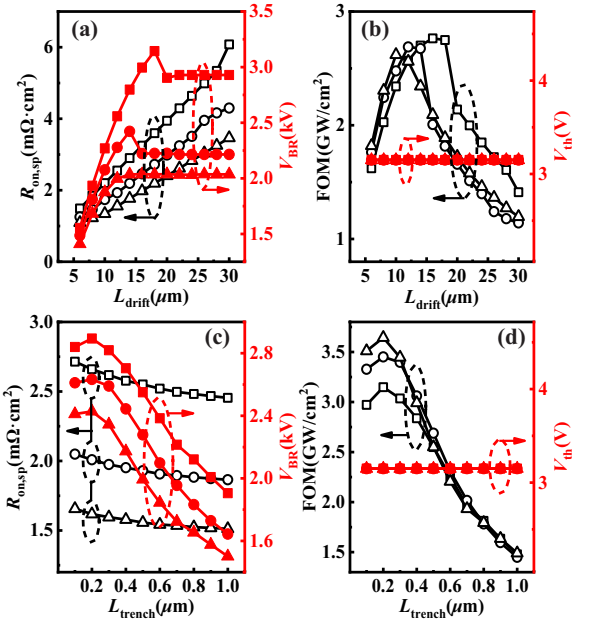

Fig. 7 **a** Simulated $R_{on,sp}$ and V_{BR} of the device versus L_{drift} and N_d. **b** V_{th} and FOM as a function of L_{drift} and N_d. **c** Simulated $R_{on,sp}$ and V_{BR} of the device versus L_{trench} and N_d. **d** V_{th} and FOM as a function of L_{trench} and N_d. In (**a**)–(**d**), the square, circle and triangle curves were simulated under $N_d = 6.0 \times 10^{15}$ cm^{-3}, $N_d = 8.0 \times 10^{15}$ cm^{-3} and $N_d = 1.0 \times 10^{16}$ cm^{-3}, respectively

concentration in the low-doped side of the PN single junction diode on the V_{BR}, which demonstrated that the value of N_d was inversely proportional to V_{BR}. It implied that V_{BR} prematurely saturated at thin L_{drift} with high N_d. Low N_d had larger DR than high N_d due to the IGR of electron was low. Large DR could withstand high voltage and prevent electron absorbing electric field energy to reach breakdown. The change of $R_{on,sp}$ was mainly caused by the variation of R_{drift} ($R_{on,sp}$ of n^--GaN drift layer). The $R_{on,sp}$ decreased with the increase of N_d and decrease of L_{drift}, respectively. $R_{on,sp}$ decreased from 2.55 mΩ·cm^2 to 1.56 mΩ·cm^2 and V_{BR} reduced from 2558 to 1997 V as N_d increased from 8.0×10^{15} cm^{-3} to 1.0×10^{16} cm^{-3} under $L_{drift}=12$ μm. In Fig. 7b, the obtained peak FOM were 2.76 GW/cm^2, 2.69 GW/cm^2 and 2.62 GW/cm^2 under $L_{drift}=16$ μm, $L_{drift}=12$ μm, and $L_{drift}=10$ μm with the growth of N_d, respectively. It demonstrated that the optimal FOM could be obtained under the low N_d and thick L_{drift}. In contrast, the change of N_d and L_{drift} had no effect on V_{th}, and it remained at 3.15 V. The impact on $R_{on,sp}$ and V_{BR} were obvious by the change of N_d and L_{drift}, while hardly influenced V_{th}.

With the increase of L_{trench} from 0.1 to 1.0 μm in Fig. 7c, d, $R_{on,sp}$ continuously decreased. In contrast, V_{BR} and FOM first increased and then decreased as the advance of L_{trench}, finally reaching peak value at $L_{trench}=0.2$ μm. The obtained peak FOM were 3.15 GW/cm^2, 3.45 GW/cm^2 and 3.64 GW/cm^2 under $N_d=6.0\times10^{15}$ cm^{-3}, $N_d=8.0\times10^{15}$ cm^{-3}, and $N_d=1.0\times10^{16}$ cm^{-3}, respectively. The impact of L_{trench} on FOM was apparent when it was thin. The variety of N_d and L_{trench} also made little difference on V_{th}. V_{th} showed independence for the change of N_d, L_{drift} and L_{trench}, due to the p-type channel region.

Analysis the Impact of p-GaN Channal and Dielectric

The effects of the $L_{channel}$ and N_a of p-GaN channel layer were investigated based on $L_{drift}=12$ μm and $L_{trench}=0.2$ μm of n^--GaN drift layer. The change of $R_{on,sp}$ was mainly caused by the variation of $R_{channel}$ ($R_{on,sp}$ of p-GaN channel layer). The curves of $R_{on,sp}$ showed continuous rising trend with the enhancement of $L_{channel}$ as shown in Fig. 8a. As N_a increased from 2.0×10^{17} cm^{-3} to 3.0×10^{18} cm^{-3} under $L_{channel}=1.0$ μm, $R_{on,sp}$ showed increasing trends from 1.94 mΩ·cm^2 to 1.96 mΩ·cm^2. The effect on the $R_{on,sp}$ brought by the variety of $L_{channel}$ was little. The growth of N_a could enlarge the V_{BR} from 65 to 2632 V under 0.1 um. V_{BR} increased and saturated at $L_{channel}=0.8$ μm under $N_a=2.0\times10^{17}$ cm^{-3}. In contrast, V_{BR} increased and saturated at $L_{channel}=0.2$ μm

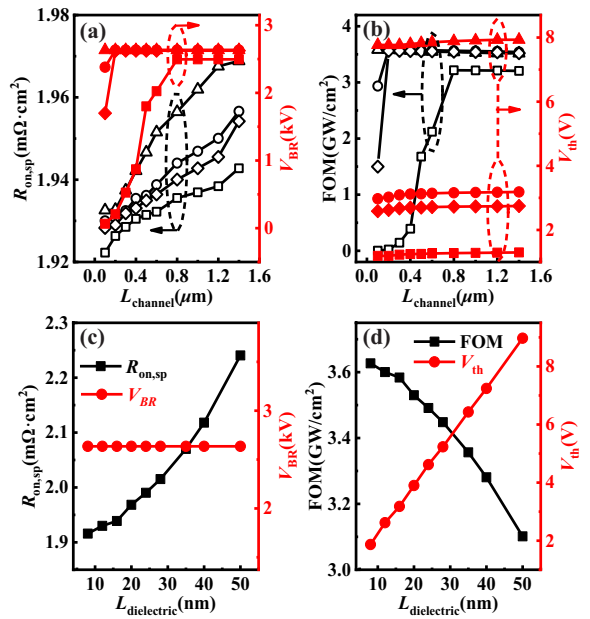

Fig. 8 **a** Simulated $R_{on,sp}$ and V_{BR} of the device versus $L_{channel}$ and N_a. **b** V_{th} and FOM as a function of $L_{channel}$ and N_a. In (**a**) and (**b**), the square, rhombus, circle and triangle curves were simulated under $N_a=2.0\times10^{17}$ cm^{-3}, $N_a=8.0\times10^{17}$ cm^{-3}, $N_a=1.0\times10^{18}$ cm^{-3} and $N_a=3.0\times10^{18}$ cm^{-3}, respectively. **c** Simulated $R_{on,sp}$ and V_{BR} of the device versus $L_{dielectric}$. **d** V_{th} and FOM as a function of $L_{dielectric}$

under $N_a=8.0\times10^{17}$ cm^{-3} and $N_a=1.0\times10^{18}$ cm^{-3}, respectively. Moreover, V_{BR} kept saturated from 0.1 μm to 1.0 μm of $L_{channel}$ under $N_a=3.0\times10^{18}$ cm^{-3}. The high enough value of $L_{channel}\cdot N_a$ could achieve avalanche breakdown, which could be seen from the saturated V_{BR}. On the contrary, the unsaturated V_{BR} was known as punch-through breakdown. Similarly, the variation trend of FOM was the same as V_{BR}. The peak FOM obtained was 3.59 GW/cm^2. V_{th} grew from 1.19 V to 7.93 V under $L_{channel}=1.0$ μm with the increase of N_a as shown in Fig. 8b. The change of N_a had a marked effect on V_{th}, whereas the impact brought by the variety of $L_{channel}$ on V_{th} was negligible.

The impact of the $L_{dielectric}$ was researched based on $L_{channel}=1.0$ μm. The growth of $L_{dielectric}$ would reduce C_{ox} and electron concentration of channel layer under on-state condition, resulting in larger $R_{on,sp}$ and V_{th}. $R_{on,sp}$ increased from 1.92 mΩ·cm^2 to 2.24 mΩ·cm^2 and V_{th} enhanced from 1.87 V to 8.97 V for $L_{dielectric}$ increasing from 8 to 50 nm as shown in Fig. 8c, d. $L_{dielectric}$ had no effect on V_{BR}, leading to the reduction of FOM from 3.63 GW/cm^2 to 3.10 GW/cm^2.

Conclusion

In this work, we analysed the performance of the fabricated GaN TG-MOSFET on 4-inch free-standing GaN substrate by Silvaco TCAD. The mechanisms of on-state and breakdown have been well studied. The key device parameters have been thoroughly researched considering the trade-off between $R_{on,sp}$ and V_{BR}. The normally off operation and high breakdown voltage show enormous potential to provide a bright future application for vertical GaN-based high power electronics.

Acknowledgements
We thank the reviewers for their valuable comments.

Authors' contributions
XL and WH conceived the idea. ZL and JL did the experiment part of this work. JL and FL did the simulation part of this work. JW collected and sorted out the literatures. BW, MW, NL, H-CC, and H-CK took place in analysis and discussion. Jian Li drafted the manuscript. Xinnan Lin and Jingbo Li provided professional assistance in the revised manuscript. All authors read and approved the final manuscript.

Funding
This work was supported by National Natural Science Foundation of China (61974144, 62004127), Key-Area Research and Development Program of Guangdong Province 2020B010169001, Guangdong Science Foundation for Distinguished Young Scholars, and Science and Technology Foundation of Shenzhen JSGG20191129114216474.

Availability of data and materials
All data generated or analyzed during this study are included within the article.

Declarations

Competing interests
The authors declare that they have no competing interests.

Author details
[1]College of Materials Science and Engineering, College of Electronics and Information Engineering, College of Physics and Optoelectronic Engineering, Institute of Microelectronics (IME), Shenzhen University, Shenzhen 518060, China. [2]Institute of Microelectronics, Peking University, Beijing 100871, China. [3]Shaanxi Reactor Microelectronics Co., Ltd., Xi'an 710075, China. [4]Department of Electronic Engineering, Chang Gung University, Taoyuan 333, Taiwan. [5]Department of Photonic and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan. [6]The Shenzhen Key Lab of Advanced Electron Device and Integration, ECE, Peking University Shenzhen Graduate School, Shenzhen 518055, China. [7]Institute of Semiconductors, South China Normal University, Guangzhou 510631, Guangdong, China.

Received: 9 November 2021 Accepted: 4 January 2022
Published online: 15 January 2022

References

1. Boutros KS, Chu R, Hughes B (2012) GaN power electronics for automotive application. IEEE Energytech 1–4
2. Ueda T (2014) Recent advances and future prospects on GaN-based power devices. In: 2014 international power electronics conference (IPEC-Hiroshima 2014-ECCE ASIA):2075–2078
3. Li H, Yao C, Fu L, Zhang X, Wang J (2016) Evaluations and applications of GaN HEMTs for power electronics. In: 2016 IEEE 8th international power electronics and motion control conference (IPEMC-ECCE Asia), pp 563–569
4. Flack TJ, Pushpakaran BN, Bayne SB (2016) GaN technology for power electronic applications: a review. J Electron Mater 45(6):2673–2682
5. Sun R, Lai J, Chen W, Zhang B (2020) GaN power integration for high frequency and high efficiency power applications: a review. IEEE Access 8:15529–15542
6. Liu X, Kim Fong Low E, Pan J, Liu W, Leong Teo K, Tan LS, Yeo YC (2011) Impact of In situ vacuum anneal and SiH_4 treatment on electrical characteristics of AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistors. Appl Phys Lett 99(9):093504
7. Liu X, Zhan C, Chan KW, Owen MHS, Liu W, Chi DZ, Tan LS, Chen KJ, Yeo YC (2013) AlGaN/GaN metal–oxide–semiconductor high-electron-mobility transistors with a high breakdown voltage of 1400 V and a complementary metal–oxide–semiconductor compatible gold-free process. Jpn J Appl Phys 52(4S):04CF06
8. Huang S, Liu X, Wang X, Kang X, Zhang J, Bao Q, Wei K, Zheng Y, Zhao C, Gao H (2016) High uniformity normally-OFF GaN MIS-HEMTs fabricated on ultra-thin-barrier AlGaN/GaN heterostructure. IEEE Electron Device Lett 37(12):1617–1620
9. Liu S, Wang M, Tao M, Yin R, Gao J, Sun H, Lin W, Wen CP, Wang J, Wu W (2017) Gate-recessed normally-OFF GaN MOSHEMT with improved channel mobility and dynamic performance using AlN/Si_3N_4 as passivation and post gate-recess channel protection layers. IEEE Electron Device Lett 38(8):1075–1078
10. Han PC, Yan ZZ, Wu CH, Chang EY, Ho YH (2019) Recess-Free Normally-off GaN MIS-HEMT Fabricated on Ultra-Thin-Barrier AlGaN/GaN Heterostructure. In: 2019 31st international symposium on power semiconductor devices and ICs (ISPSD), pp 427–430
11. Liu X, Chiu HC, Liu CH, Kao HL, Chiu CW, Wang HC, Ben J, He W, Huang CR (2020) Normally-off p-GaN gated AlGaN/GaN HEMTs using plasma oxidation technique in access region. IEEE J Electron Devices Soc 8:229–234
12. Nie H, Diduck Q, Alvarez B, Edwards AP, Kayes BM, Zhang M, Ye G, Prunty T, Bour D, Kizilyalli IC (2014) 1.5-kV and 2.2-mΩ-cm^2 Vertical GaN Transistors on Bulk-GaN Substrates. IEEE Electron Device Lett 35(9):939–941
13. Ji D, Laurent MA, Agarwal A, Li W, Mandal S, Keller S, Chowdhury S (2016) Normally OFF trench CAVET with active Mg-doped GaN as current blocking layer. IEEE Trans Electron Devices 64(3):805–808
14. Shibata D, Kajitani R, Ogawa M, Tanaka K, Tamura S, Hatsuda T, Ishida M, Ueda T (2016) 1.7 kV/1.0 mΩ·cm^2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure. In: 2016 IEEE international electron devices meeting (IEDM).
15. Ji D, Agarwal A, Li H, Li W, Keller S, Chowdhury S (2018) 880 V/2.7 mΩ·cm^2 MIS Gate Trench CAVET on Bulk GaN Substrates. IEEE Electron Device Lett 39(6):863–865
16. Oka T, Ueno Y, Ina T, Hasegawa K (2014) Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV. Appl Phys Express 7(2):21002–21002
17. Oka T, Ina T, Ueno Y, Nishii J (2015) 1.8 mΩ·cm^2 vertical GaN-based trench metal-oxide-semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation. Appl Physics Express 8(5):54101–54101
18. Li R, Cao Y, Chen M, Chu R (2016) 600 V/1.7 Ω normally-Off GaN vertical trench metal-oxide-semiconductor field-effect transistor. IEEE Electron Device Lett 37(11):1466–1469
19. Williams RK, Darwish MN, Blanchard RA, Siemieniec R, Rutter P, Kawaguchi Y (2017) The trench power MOSFET: Part I-History, technology, and prospects. IEEE Trans Electron Devices 64(3):674–691
20. Williams RK, Darwish MN, Blanchard RA, Siemieniec R, Rutter P, Kawaguchi Y (2017) The trench power MOSFET-part II: application specific VDMOS, LDMOS, packaging, and reliability. IEEE Trans Electron Devices 64(3):692–712
21. Guo Z, Hitchcock C, Chow TSP (2019) Comparative performance evaluation of lateral and vertical GaN high-voltage power field-effect transistors. Jpn J Appl Phys 58(SC):9
22. Liu X, Gu H, Li K, Guo L, Zhu D, Lu Y, Wang J, Kuo HC, Liu Z, Liu W (2017) AlGaN/GaN high electron mobility transistors with a low sub-threshold swing on free-standing GaN wafer. AIP Adv 7(9):95305–95305
23. Zhou Q, Wei D, Peng X, Zhu R, Dong C, Huang P, Wei P, Xiong W, Ma X, Dong Z (2018) A novel enhancement-mode GaN vertical MOSFET with double hetero-junction for threshold voltage modulation. Superlattices Microstruct 123:297–305

24. Ji D, Gupta C, Agarwal A, Chan SH, Lund C, Li W, Keller S, Mishra UK, Chowdhury S (2018) Large-area in-situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET). IEEE Electron Device Lett 39(5):711–714
25. Li W, Nomoto K, Lee K, Islam S, Hu Z, Zhu M, Gao X, Pilla M, Jena D, Xing HG (2018) Development of GaN vertical trench-MOSFET with MBE regrown channel. IEEE Trans Electron Devices 65(6):2558–2564
26. Liu S, Song X, Zhang J, Zhao S, Luo J, Zhang H, Zhang Y, Zhang W, Zhou H, Liu Z (2020) Comprehensive Design of Device Parameters for GaN Vertical Trench MOSFETs. IEEE Access 8:57126–57135
27. Kucharski R, Sochacki T, Lucznik B, Bockowski M (2020) Growth of bulk GaN crystals. J Appl Phys 128(5):050902
28. Mikawa Y, Ishinabe T, Kagamitani Y, Mochizuki T, Ikeda H, Iso K, Takahashi T, Kubota K, Enatsu Y, Tsukada Y, Izumisawa S (2020) Recent progress of large size and low dislocation bulk GaN growth//Gallium Nitride Materials and Devices XV. Int Soc Opt Photon 11280:1128002
29. Ren B, Sumiya M, Liao M, Koide Y, Liu X, Shen Y, Sang L (2018) Interface trap characterization of Al_2O_3/GaN vertical-type MOS capacitors on GaN substrate with surface treatments. J Alloys Compd 767:600–605
30. Park J, Lee JH (2016) A 650 V super-junction MOSFET with novel hexagonal structure for superior static performance and high BV resilience to charge imbalance: A TCAD simulation study. IEEE Electron Device Lett 38(1):111–114
31. Huang H, Li F, Sun Z, Sun N, Zhang F, Cao Y, Zhang H, Tao P (2019) Gallium nitride normally-off vertical field-effect transistor featuring an additional back current blocking layer structure. Electronics 8(2):241–241
32. Sabui G, Parbrook PJ, Arredondo-Arechavala M, Shen Z (2016) Modeling and simulation of bulk gallium nitride power semiconductor devices. AIP Adv 6(5):55006–55006
33. Donato N, Udrea F (2018) Static and dynamic effects of the incomplete ionization in superjunction devices. IEEE Trans Electron Devices 65(10):4469–4475
34. Mukherjee K, Santi CD, Buffolo M, Borga M, You S, Geens K, Bakeroot B, Decoutere S, Gerosa A, Meneghesso G (2021) Understanding the leakage mechanisms and breakdown limits of vertical GaN-on-Si p^+n^-n diodes: the road to reliable vertical MOSFETs. Micromachines 12(4):445
35. Tripathi PM, Soni H, Chaujar R, Kumar A (2020) Numerical simulation and parametric assessment of GaN buffered trench gate MOSFET for low power applications. IET Circuits Devices Syst 14:915–922
36. Manual AU (2010) Silvaco. Santa Clara, CA.
37. Oğuzman IH, Bellotti E, Brennan KF, Kolník J, Wang R, Ruden PP (1997) Theory of hole initiated impact ionization in bulk zincblende and wurtzite GaN. J Appl Phys 81(12):7827–7834
38. Cao L, Wang J, Harden G, Ye H, Stillwell R, Hoffman AJ, Fay P (2018) Experimental characterization of impact ionization coefficients for electrons and holes in GaN grown on bulk GaN substrates. Appl Phys Lett 112(26):262103–262103
39. Ji D, Ercan B, Chowdhury S (2019) Experimental determination of impact ionization coefficients of electrons and holes in gallium nitride using homojunction structures. Appl Phys Lett 115(7):73503
40. Maeda T, Narita T, Yamada S, Kachi T, Kimoto T, Horita M, Suda J (2019) Impact ionization coefficients in GaN measured by above-and sub-Eg illuminations for p^-/n^+ junction. In: 2019 IEEE international electron devices meeting (IEDM)
41. Cooper JA, Morisette DT (2020) Performance limits of vertical unipolar power devices in GaN and 4H-SiC. IEEE Electron Device Lett 41(6):892–895
42. Ortiz-Conde A, Sánchez FG, Liou JJ, Cerdeira A, Estrada M, Yue Y (2002) A review of recent MOSFET threshold voltage extraction methods. Microelectron Reliab 42:583–596

Publisher's Note