1.6 nm Oxide Equivalent Gate Dielectrics Using Nitride/Oxide (N/O) Composites Prepared by RPECVD/Oxidation Process

Yider Wu, Yi-Mu Lee, and Gerald Lucovsky, *Member, IEEE*

***Abstract*—Ultrathin nitride/oxide (∼1.5/0.7 nm) dual layer gate dielectrics have been formed using remote plasma enhanced CVD of nitride onto plasma-grown oxide interface layers. High accumulation capacitance (1.72 μF/cm^2) is measured and the equivalent oxide thickness is 1.6 nm after quantum effect corrections. Compared to 1.6 nm oxides, a tunneling current reduction of more than 100 fold is found for devices with 1.6 nm N/O dielectrics due to increased film thickness and interface nitridation. Hole channel mobility decreases by about 5%, yielding very good P-MOSFET current drive. Excellent dielectric reliability and interface robustness are also demonstrated for P-MOSFET's with N/O dielectrics.**

***Index Terms*—Gate dielectric, MOSFET, nitride, oxide, tunneling current.**

I. Introduction

As THE AGGRESSIVE scaling of CMOS technology continues, tunneling leakage limits the scaling of SiO_2 to approximately 1.6–1.7 nm. Nitride/oxide dual layer gate dielectrics have emerged as promising alternatives to silicon dioxide in dual gate CMOS devices [1]. The advantages include a higher dielectric constant ($\varepsilon_{\rm nitride} \sim 7.8$), excellent thermal stability, and a barrier for impurity/dopant diffusion. It has been shown that 0.8 nm of nitride suppresses boron transport out of p$^+$ polysilicon gates during high thermal budget dopant activation anneals [2]. Therefore, with a diffusion barrier at polysilicon/dielectric interface, the N/O dual layer dielectrics prevent boron incorporation in the oxide bulk and show improved reliability [3]. In addition, because silicon nitride has almost twice the dielectric constant of silicon dioxide, lower tunneling has been obtained for N/O films compared to oxides with the same oxide-equivalent thickness [4]. Whereas pure nitride gate dielectric may be preferable for tunneling current reductions, its poor interface with Si severely degrades MOSFET performance, so that ultrathin buffer oxide interfacial layer are required in MOSFET devices [5].

Manuscript received July 15, 1999; revised November 8, 1999. This work was supported in part by the NSF, SRC, and ONR. The review of this paper was arranged by Editor D. J. Dumin.

Y. Wu is with Advanced Micro Devices, Sunnyvale, CA 94088 USA (e-mail: yider.wu@amd.com).

Y.-M. Lee is with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-8202 USA.

G. Lucovsky is with the Department of Electrical and Computer Engineering, the Department of Material Science and Engineering, and the Department of Physics, North Carolina State University, Raleigh, NC 27695-8202 USA (e-mail: gerry_lucovsky@ncsu.edu).

Publisher Item Identifier S 0741-3106(00)02116-9.

In this work, we have investigated the electrical properties of p$^+$-poly gate P-MOSFET's with 1.6 nm N/O dual layer gate dielectrics in which the nitride layer was prepared by remote plasma enhanced chemical vapor deposition (RPECVD) and the oxide layer by remote plasma oxidation. This paper focuses on PMOS because, due to boron penetration, PMOS has more severe reliability problem compared to NMOS while oxide is scaled down to sub-2.0 nm region. That is a major limit for oxide scaling down, but N/O dielectrics can take advantage of nitride's low boron diffusivity to improve it. An interface nitridation process was used to incorporate one monolayer nitrogen at the Si-dielectric interface; this modifies the interfacial suboxide bonding and also reduces direct tunneling [6]. We find that 1.6 nm N/O dielectrics reduce direct tunneling by more than 100 compared to single layer oxide with the same capacitance. Very good hole channel mobility and MOSFET characteristics are demonstrated. Finally, excellent dielectric reliability and immunity against hot carrier stressing were observed for PMOSFETS with the aggressively-scaled N/O dielectrics.

II. Experimental

P-MOSFET's with p$^+$-poly gates were fabricated on 0.02–0.05 Ω-cm n-type Si ⟨100⟩ substrates. The bottom oxide layer is formed using remote N_2O plasma oxidation. This low temperature process provides an excellent thickness control of oxide growth down to 0.4–0.7 nm, which is not readily achieved by the furnace oxidation processes [7]. Following the oxidation, a remote plasma nitridation step is used to incorporate a monolayer nitrogen at the interface; this modifies the interface sub-oxide bonding and reduces tunneling current [6]. A 1.5 nm RPECVD nitride is then deposited using SiH_4 and N_2 as source gases to form the N/O structure [1], [7]. The oxide thickness is estimated by on-line Auger electron spectroscopy [8], and nitride thickness is determined from the deposition rate. Post-deposition annealing of the N/O films was performed in He at 900 °C for 30 s for chemical and structural relaxation [9]. Polysilicon ∼290 nm was then deposited, patterned, and implanted with BF_2 (30 keV, 5×10^{15}/cm^2), and activated at 1000 °C for 40 s. The equivalent oxide electrical thickness (T_{ox-eq}) of 1.6 nm was obtained from analysis of high-frequency capacitance–voltage (C–V) data including quantum effect correction [10]. 1.6–2.6 nm oxides were grown in the dry oxygen for control devices.

0741-3106/00$10.00 © 2000 IEEE

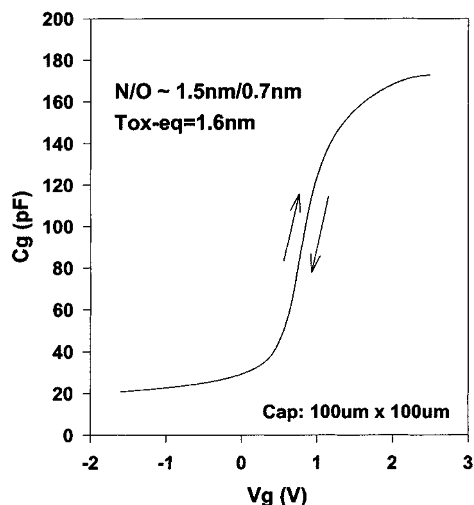


Fig. 1. Hysteresis for N/O∼1.5/0.7 nm dielectrics, with 1.6 nm equivalent oxide thickness. It is clear that no measurable hysteresis can be found in the C–V curves.

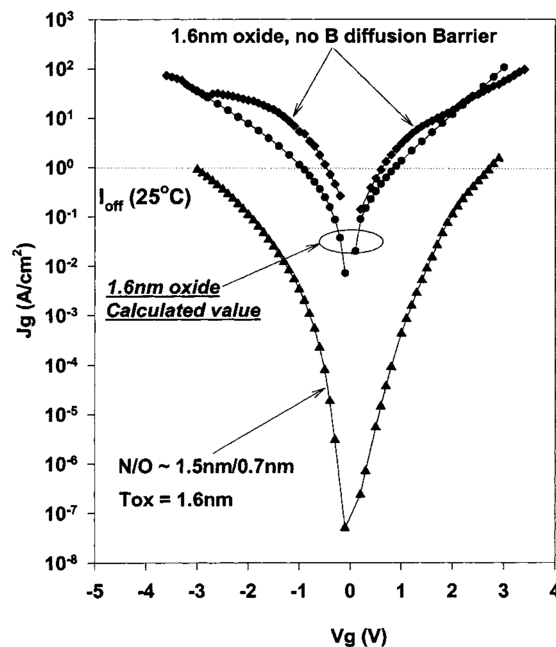


Fig. 2. Tunneling currents for 1.6 nm oxide, 1.6 nm N/O films, and calculated value for 1.6 nm oxide. Compared to the calculated tunneling current of 1.6 nm oxide, the N/O device shows a reduced tunneling current of more than 100. The oxide device shows higher current due to boron penetration to the Si–SiO_2 interface.

III. Results and Dissusion

Fig. 1 shows the C–V trace for a P-MOSFET with a N/O∼1.5/0.7 nm. The 1.6 nm equivalent oxide thickness is obtained by the accumulation capacitance (∼1.72 μF/cm^2) with quantum effect correction [10]. The trace/retrace indicated by the arrows indicates no measurable hysteresis in the C–V curves. Finally, based on the agreement between the measured and calculated flatband voltages, there is no measurable boron transport to the Si-dielectric interface. The effect of tunneling current reduction is shown in Fig. 2. Compared to the calculated tunneling current of 1.6 nm oxide, the N/O device shows a reduced tunneling current of more than 100 for both substrate and gate injection. If the off state gate leakage current limitation is taken as 1 Amp/cm^2 [11], these N/O dual layer gate dielectrics should not reach this level of tunneling current until the effective thickness is scaled to about 1.3 nm, thereby providing about 30% more capacitance than a 1.7 nm oxide. The reduction of tunneling current comes from two independent effects: 1) the increased physical film thickness associated with the increased dielectric constant of the nitride layer [4] and 2) an interface restructuring due to monolayer nitrogen incorporation [6]. Additionally, the device with the oxide dielectric in Fig. 2 shows an increased tunneling current with respect to calculated value due to boron degradation to the oxide bulk and Si-dielectric interface.

Fig. 3 shows the PMOS mobility for 1.6 nm N/O dual layer and 2.6 nm oxide gate dielectrics and Id–Vg characteristics with 0.7 μm channel length. The effective mobility of N/O dual layer and oxide devices were extracted from large transistors ($W/L = 10/10$ μm) to avoid the uncertainties in effective channel length and the effects of the source/drain series resistance [12]. Because the PMOS device with 1.6 nm oxide did not function due to the large gate tunneling, no mobility data could be extracted for comparison. Therefore, a device with a 2.6 nm oxide was used for the mobility comparison. As shown in Fig. 3, the 1.6 nm N/O device shows only ∼5% mobility degradation compared to the 2.6 nm oxide device, which meets acceptable targets for device scaling. The inset of Fig. 3 shows the Id–Vg characteristics for a 0.7 μm P-MOSFET with 1.6 nm N/O film. A good on-off characteristic is shown with a subthreshold slope at 78 mV/dec. The N/O dielectric reliability is shown in Fig. 4. Two aggressive stress conditions, $Vg = -3$ V and −3.6 V, are applied as shown in Fig. 4(a), which correspond to Jg∼2.4 and 17 Amp/cm^2, respectively. No breakdown or SILC was found for −3 V stress after 80 000 s. There was a 3.3% transconductance (gm) degradation and 7% threshold voltage shift after a

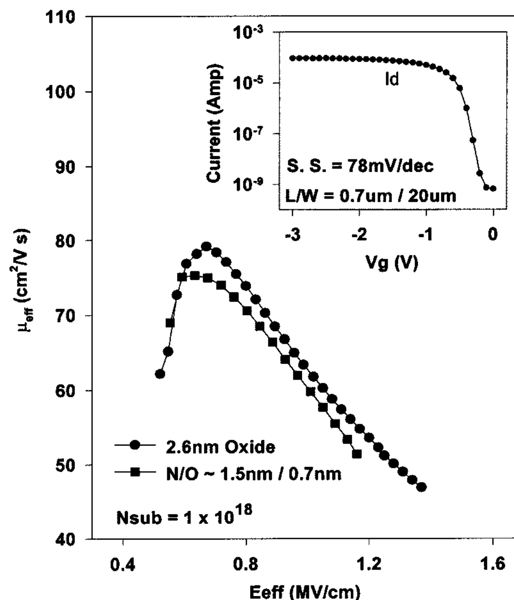
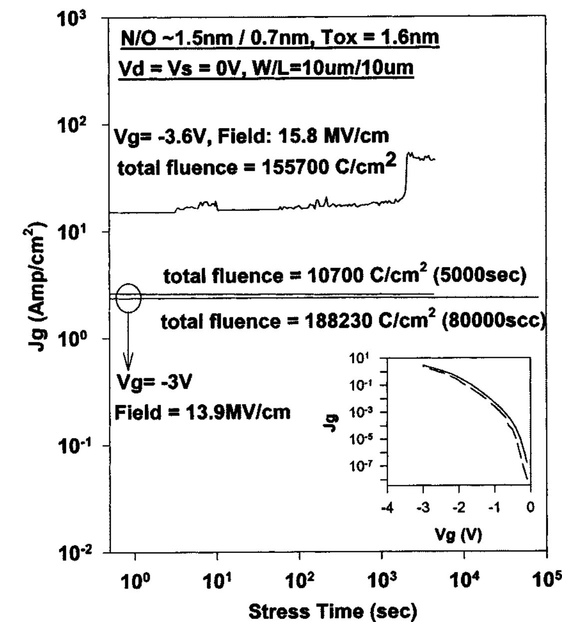


Fig. 3. PMOS mobility for 1.6 nm N/O dual layer and 2.6 nm oxide gate dielectrics, and Id–Vg characteristics for 0.7 μm channel length P-MOSFET.



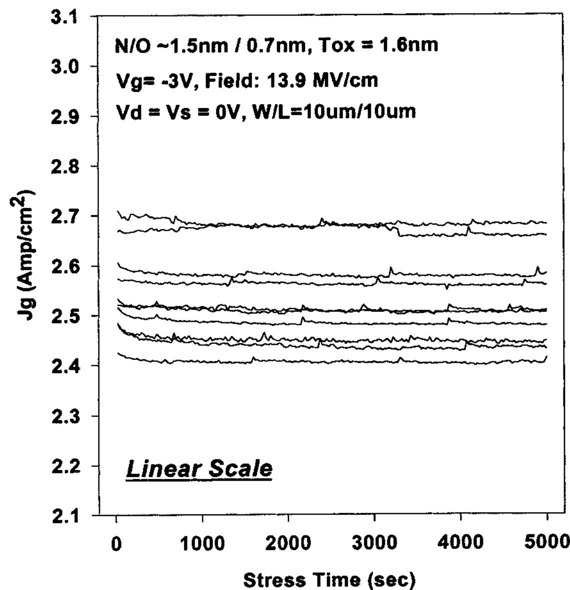


Fig. 4. Constant voltage stressing for N/O films. (a) Two aggressive stress conditions, $Vg = -3$ V and −3.6 V, are plotted in log scale, which correspond, respectively, to Jg∼2.6 and 17 Amp/cm^2. No breakdown or SILC was found for −3 V stress after 5000 s. The inset shows the *I–V* curves before and after −3 V, 5000 s stress. The dash line is before stress and the solid line is after stress. (b) Stressing of 10 N/O devices at $Vg = -3$ V plotted in linear scale.

188 230 C/cm^2 carrier injection at this stress voltage. For the −3.6 V stress, which corresponds to Eox-eq∼15.8 MV/cm, the gate leakage was increased by about three after 5000 s stress due to multiple soft breakdowns. However, no hard breakdown was found even after a 155 700 C/cm^2 gate current injection, and the MOSFET is still functioning but with 10% gm degradation and 15% threshold voltage shift. Although this is not adequate here to express the reliability of gate dielectrics because the appearance of soft breakdowns in the early stage should also be avoided, the magnitude of injected charge and wearout phenomena for the N/O devices reveal a clear improvement if compared to the conventional oxide devices. Furthermore, the inset compared current–voltage (I–V) characteristics for N/O dielectrics before and after stress. The SILC is still negligible after 10 700 C/cm^2 charge injection. Fig. 4(b) shows the $I - t$ characteristics of ten N/O devices with $Vg = -3$ V stress in the linear scale. All the $I - t$ curves show almost no SILC after 10^4 C/cm^2 charge injection. This possibly indicates that N/O dielectrics is with a low defect generation rate.

IV. Conclusion

Nitride/oxide dual layer gate dielectrics prepared by a RPECVD/oxidation process with 1.6 nm equivalent oxide thickness have been fabricated for p$^+$-poly P-MOSFET's. The devices with the 1.6 nm N/O layers and with a post-oxidation plasma-assisted interface nitridation show more than 100 times lower tunneling current compared to devices with 1.6 nm oxides. Combined with the good interface properties, an effective impurity diffusion barrier, and improved film reliability as demonstrated in this paper, the N/O dual layer gate dielectrics show good promise for sub-.25 μm dual-gate CMOS technology; with the expectation of tunneling leakage currents remaining below 1 Amp/cm^2 for Tox-eq∼1.3 nm.

References

[1] Y. Wu and G. Lucovsky, "Ultrathin nitride/oxide (N/O) gate dielectrics for p+-poly gated PMOSFET's prepared by a combined remote plasma enhanced CVD/thermal oxidation process," *IEEE Electron Device Lett.*, vol. 19, p. 367, 1998.

[2] ——, "Improvement of gate dielectric reliability for p+ poly MOS devices using remote PECVD top nitride deposition on thin gate oxides," in *IEEE Int.Reliability Physics Symp.*, 1998, p. 70.

[3] ——, "Improvement of gate dielectric reliability for p+ poly MOS devices using remote PECVD top nitride deposition on ultra-thin (2.4–6 nm) gate oxides," *Microelectron. Reliab.*, vol. 39, p. 365, 1999.

[4] C. Parker, G. Lucovsky, and J. Hauser, "Ultrathin oxide-nitride gate dielectric MOSFET's," *IEEE Electron Device Lett.*, vol. 19, p. 106, 1998.

[5] G. Lucovsky *et al.*, "Bonding constraint and defect formation at interfaces between crystalline silicon and advanced single layer and composite gate dielectrics," *Appl. Phys. Lett.*, vol. 74, p. 2005, 1999.

[6] H. Niimi, H. Yang, and G. Lucovsky, "A new low thermal budget approach to interface nitridation for ultra-thin silicon dioxide gate dielectrics by combined plasma-assisted and rapid thermal processing," in *Proc. Int. Conf. Characterization and Metrology for ULSI Technology*, 1998, p. 273.

[7] S. Hattangady, H. Niimi, and G. Lucovsky, "Controlled nitrogen incorporation at the gate oxide surface," *Appl. Phys. Lett.*, vol. 66, p. 3495, 1995.

[8] C. Chang, "General formalism for quantitative Auger analysis," *Surf. Sci.*, vol. 48, p. 9, 1975.

[9] Y. Ma, T. Yasuda, and G. Lucovsky, "Ultrathin device quality oxide-nitride-oxide heretostructure formed by remote plasma enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 64, p. 2226, 1994.

[10] W. Henson *et al.*, "Estimating oxide thickness of tunnel oxides down to 1.4 nm using conventional capacitance-voltage measurements on MOS capacitors," *IEEE Electron Device Lett.*, vol. 20, p. 179, 1999.

[11] S. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Lett.*, vol. 18, p. 209, 1997.

[12] J. Hauser, "Extraction of experimental mobility data for MOS devices," *IEEE Trans. Electron Devices*, vol. 43, p. 1981, 1996.