1-Bit Full Adder in Perpendicular Nanomagnetic Logic using a Novel 5-Input Majority Gate

Stephan Breitkreutz[1,a], Irina Eichwald[1], Josef Kiermaier[1], Adam Papp[2], György Csaba[2], Michael Niemier[2], Wolfgang Porod[2], Doris Schmitt-Landsiedel[1], and Markus Becherer[1]

[1]Lehrstuhl für Technische Elektronik, Technische Universität München, 80333 Munich, Germany
[2]Center for Nano Science and Technology, University of Notre Dame, Notre Dame, IN 46556, USA

Abstract. In this paper, we show that perpendicular Nanomagnetic Logic (pNML) is particularly suitable to realize threshold logic gate (TLG)-based circuits. Exemplarily, a 1-bit full adder circuit using a novel 5-input majority gate based on TLGs is experimentally demonstrated. The theory of pNML and its extension by TLGs is introduced, illustrating the great benefit of pNML. Majority gates based on coupling field superposition enable weighting each input by its geometry and distance to the output. Only 5 magnets, combined in two logic gates with a footprint of $1.95\,\mu m^2$ and powered by a perpendicular clocking field, are required for operation. MFM and magneto-optical measurements demonstrate the functionality of the fabricated structure. Experimental results substantiate the feasibility and the benefits of the combination of threshold logic with pNML.

1 Introduction

Nanomagnetic Logic (NML) is an emerging information processing technology using the interaction of bistable magnets to perfom logic operations [1, 2]. Low-power switching and high density integration of interconnect-free, non-volatile magnets facilitate energy-efficient and area-saving integration of combined logic and memory devices in pure NML or hybrid CMOS/NML circuitry [3, 4].

Perpendicular NML (pNML) uses CoPt or CoNi nanomagnets with perpendicular magnetic anisotropy (PMA). It benefits from flexible geometries and shape independent anisotropy, which is tuned by focused ion beam (FIB) irradiation [5]. Therefore, so-called artificial nucleation centers (ANCs) are fabricated by partial FIB irradiation at user-defined positions and provide directed signal flow in chains [6–8] and gates [9] of field-coupled nanomagnets.

Fig. 1 shows the vision of a fully-integrated pNML system. Information is processed by complex circuits providing non-volatile logic operation using majority gates and inverters connected by wires [10]. Crossing of magnetic signals is achieved by detouring through additional functional layers [11] and logic gates can be programed during runtime [12]. Current wires [13] and spin transfer torque (STT) devices [14] are envisioned as I/O elements for electrical circuitry integration. An integrated on-chip coil generates perpendicular magnetic fields which operate as both power supply and clock generator [15].

Furthermore, perpendicular NML is highly suitable to realize threshold logic gate (TLG)-based architectures [16]. The working principle of majority gates based on fringing field superposition offers the possibility to weight
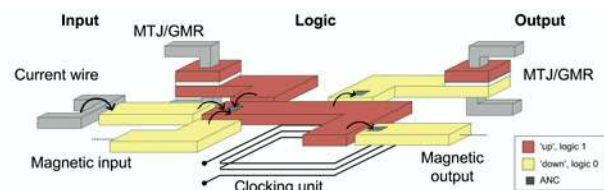

Figure 1. Vision of a perpendicular NML system using field-coupled magnets for logic computation, electrical I/O elements for CMOS integration and an on-chip coil as power supply.

each input by its size and distance to the ANC. In this paper, we exemplary demonstrate a TLG-based full adder circuit using a novel 5-input majority gate by experiment.

2 Theory of perpendicular NML

To realize logic operations, the switching process of an output magnet needs to be controlled by the coupling fields of its surrounding input magnets. The reversal process of each nanomagnet with PMA is governed by domain wall (DW) nucleation and propagation [17]. In pNML devices, the DW nucleation at the ANC of the output is supported or constrained by the input coupling fields [9].

Fig. 2 shows the basic principle of pNML. The central magnet with magnetization M_z is partially irradiated on the left side and its switching field is reduced to H_c. Due to the location of the ANC, only the short ranged coupling field C of the left neighbor M_1 influences the switching process of the central magnet. The antiferromagnetic coupling field superposes with the applied, perpendicular field
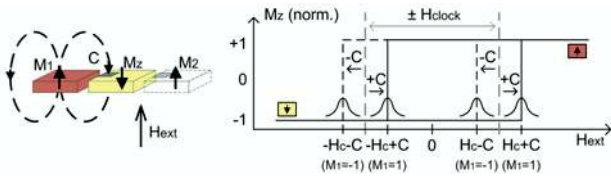
---

[a]e-mail: stephan.breitkreutz@tum.de

Figure 2. Theory of pNML. The ANC of the central magnet is only sensitive to the short ranged coupling field C of the left neighbor. A clocking field with adequate amplitude H_{clock} enforces antiparallel ordering from left to right.

H_{ext} and therefore shifts the hysteresis of the central magnet to left or right depending on the magnetization state M_1, but independent of M_2 [6].

An alternating clocking field with adequate amplitude $H_{clock} = H_c$ will force the central magnet to switch to the antiparallel state of M_1. Similarly, M_2 will be ordered antiparallel to M_z. The stepwise antiparallel ordering enables directed signal flow in a chain of magnets and constitutes the basis for logic operations in pNML circuitry [7, 8].

Due to switching field distributions (SFDs) caused by the influence of thermal noise and fabrication variations of the ANC from dot to dot, the residual clocking window for complex NML circuits is noticeably reduced [15, 18–20]. Hence, it is fundamental to precisely control the location and the strength of the ANC by size and dose of the partial FIB irradiation [5, 9].

3 TLG-based pNML

In general, threshold logic gates weight each single, binary input and compare the weighted sum to a threshold to define the binary output [21]. In adaption to pNML, where magnets can only have the binary (magnetization) states up ($+1 \hat{=}$ logic '1') or down ($-1 \hat{=}$ logic '0'), the definition of the function F of a threshold gate is given by

$$F(x_1 \ldots x_n) = 1 \text{ if } \sum_{i=1}^{n} w_i x_i \geq 0 \qquad (1)$$

$$F(x_1 \ldots x_n) = -1 \text{ if } \sum_{i=1}^{n} w_i x_i < 0 \qquad (2)$$

with w_i as weight and $x_i \in \{-1, 1\}$ as binary state of the input i [16]. In a majority gate, the superposed coupling fields of all input magnets on the ANC of the output decide about its switching. The coupling field C of a magnet approximately scales by

$$C \propto \frac{A^{n_1}}{d^{n_2}} \qquad (3)$$

with the input size A and the distance d to the magnet. n_1 and n_2 are geometry-dependend exponents in the range of $0 < n_1 \leq 1$ and $1 < n_2 \leq 3$. Thus, pNML majority gates offer the possibility to weight each input by its geometry and distance to the output ANC. According to [16], the magnetization m_{out} of an output magnet after clocking is

$$m_{out} = -\text{sgn} \sum_i C_i \cdot m_i \qquad (4)$$
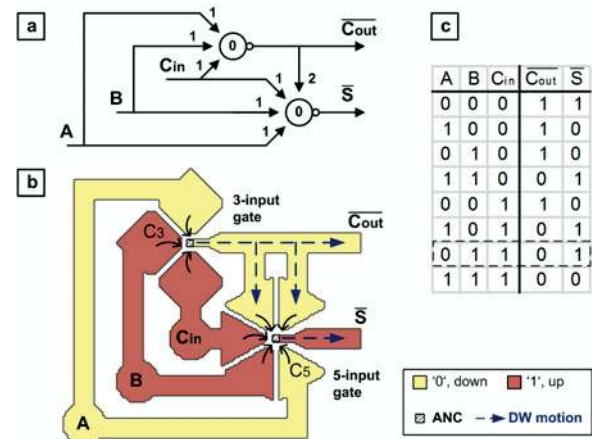

Figure 3. a) Schematic of a full adder based on threshold logic gates. b) Full adder layout using a 3-input gate to set the inverted carry-out $\overline{C_{out}}$ and a novel 5-input gate with a double weighted input for the inverted sum $\overline{S}$. c) Corresponding truth table.

with $m_i \in \{-1, 1\}$ as normalized magnetization state M_z/M_s and C_i as effective coupling field of the input i.

Fig. 3a shows the schematic of a TLG-based full adder circuit as proposed by [21] and adapted for pNML by [16]. The inverted carry-out $\overline{C_{out}}$ is defined by a 3-input majority gate with equal weights. The inverted sum $\overline{S}$ is given by a 4-input TLG with the input $\overline{C_{out}}$ double-weighted compared to A, B and C_{in}. However, in semiconductor technology, it is more common to fabricate structures with equal sizes and distances. Consequently, $\overline{S}$ can be computed by a 5-input majority gate where two inputs are set by $\overline{C_{out}}$ and the other three by A, B and C_{in}, respectively.

Fig. 3b shows the layout of the TLG-based full adder structure using a 3-input and a 5-input gate to compute the outputs $\overline{C_{out}}$ and $\overline{S}$. The size and the distance (and therefore the weight) of each input structure is equal within each gate, but $\overline{C_{out}}$ defines two inputs in the 5-input gate. During clocking, $\overline{C_{out}}$ is set antiparallel to the majority of the input magnets A, B and C_{in} by the first clocking pulse in the 3-input gate, according to the truth table (Fig. 3c). Once $\overline{C_{out}}$ is set, $\overline{S}$ is defined (switched or not) in the 5-input gate by the second clocking pulse.

The input magnets B and C_{in} can be contacted by crossing elements [11] or MTJ/GMR structures. Remarkably, the whole circuit consists of only 5 magnets, which is the minimum possible number to realize a structure with 3 inputs and 2 outputs.

4 Experiment

The $Ta_{1nm}Pt_{3nm}[Co_{0.8nm}Pt_{1nm}]_{x4}Pt_{3nm}$ multilayer stack is magnetron sputtered on a thermally oxidized Si $\langle 100 \rangle$ wafer. The Pt seed layer enforces the PMA of the Co, the toplayer prevents the Co from oxidation. The multilayer film is structured by FIB lithography and ion beam etching using an evaporated 5 nm-Ti hard mask. Subsequently, the output magnets $\overline{C_{out}}$ and $\overline{S}$ are partially irradiated on
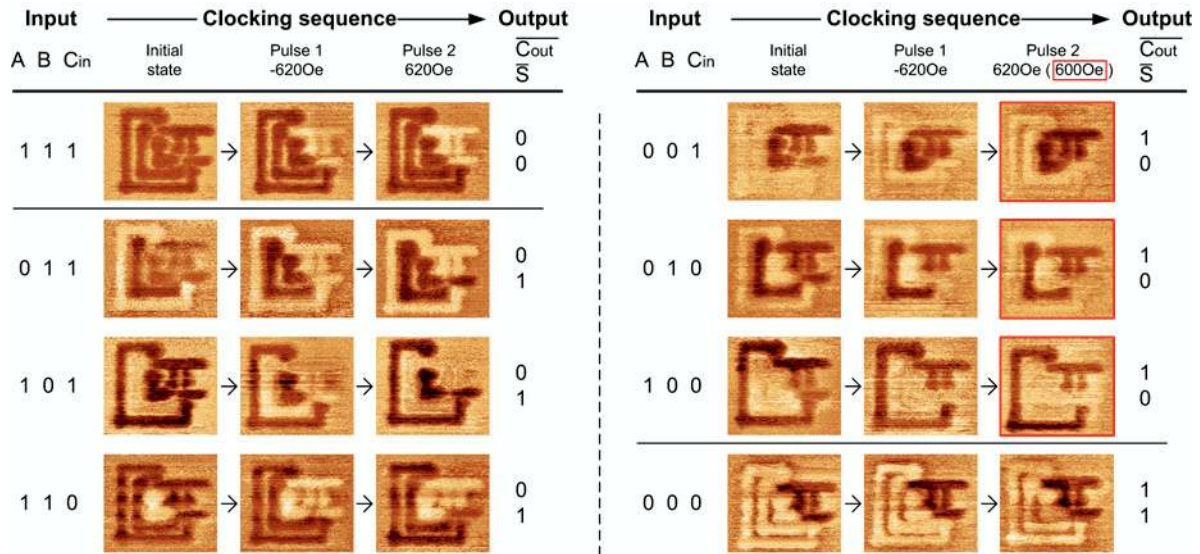
Figure 6. MFM images of the full adder structure during the clocking sequence for all possible input configurations. Out of the initial state, $\overline{C_{out}}$ and $\overline{S}$ are sequentially ordered in the correct state by two subsequent clocking pulses with $H_{clock} = \mp620$ Oe.
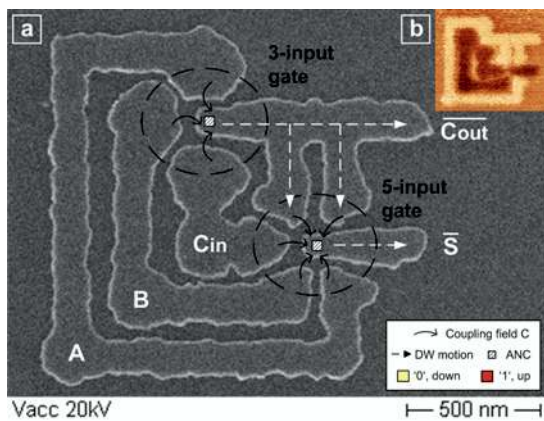

Figure 4. a) SEM image of the fabricated structure with inputs A, B and C_{in} and the outputs $\overline{C_{out}}$ and $\overline{S}$. The estimated position of the ANCs is marked by shaded areas. b) Corresponding MFM image of the '011' input configuration after clocking.

Figure 5. Experimental procedure: In the initial state the input magnets A, B and C_{in} are set to the desired configuration, the outputs $\overline{C_{out}}$ and $\overline{S}$ are set to the up state by a 1 kOe pulse. Afterwards $\overline{C_{out}}$ and $\overline{S}$ are sequentially ordered by two alternating clocking pulses with the amplitude $H_{clock} = \mp620$ Oe.

an area of $20\,\text{nm} \cdot 20\,\text{nm}$ with a dose of $2 \cdot 10^{13}\,\frac{\text{ions}}{\text{cm}^2}$ using a 50 kV Ga$^+$ FIB system. Fig. 4a shows a SEM image of the fabricated full adder. Its size is $1.5 \cdot 1.3\,\mu\text{m}^2$, the width of the magnets is 100 nm and the gap between inputs and outputs is $\approx 20 - 30$ nm. Fig. 4b shows the corresponding MFM phase image for the '011' input configuration (A, B, C_{in}) after clocking.

Due to the lowered anisotropy at the ANC, the partial irradiated magnets $\overline{C_{out}}$ and $\overline{S}$ have a mean switching field of ≈ 620 Oe, which is also the amplitude B_{clock} for the clocking field. The input magnets A, B and C_{in} are not irradiated and therefore not affected by the clocking pulses. Hence, each input configuration can be set by external fields prior to the clocking phase of the experiment. Certainly, in an operating circuit, the inputs would be set by prior gates or input structures.
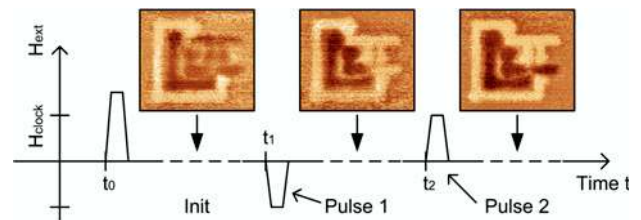
Fig. 5 shows the clocking scheme utilized in the experiment. The input configuration A, B, C_{in} is set by external fields and the outputs $\overline{C_{out}}$ and $\overline{S}$ are set upwards by an initial field pulse with 1 kOe amplitude (Init, time t_0). Afterwards the outputs are computed by two opposing clocking pulses with $H_{clock} = \mp620$ Oe. The first pulse (Pulse 1, t_1), sets $\overline{C_{out}}$ to the designated state. The second pulse (Pulse 2, t_2) switches $\overline{S}$ back to the correct state.

Fig. 6 shows the measurement results for all possible input configurations of A, B and C_{in}. The outputs $\overline{C_{out}}$ and $\overline{S}$ are subsequentially ordered by the clocking pulses. Note, that depending on the input configuration, $\overline{C_{out}}$ and/or $\overline{S}$ may be already set correctly by the init pulse. Then the structure is earlier in its final state, but does not change by any further pulses. However, correct ordering of the outputs is only guaranteed after one complete clocking cycle.

In some cases, the amplitude of the second pulse had to be reduced to 600 Oe to avoid undesired switching of $\overline{S}$. Due to the influence of thermal noise, a magnet has a given probability to switch during an applied field pulse depending on its amplitude and length. The statistical switch-
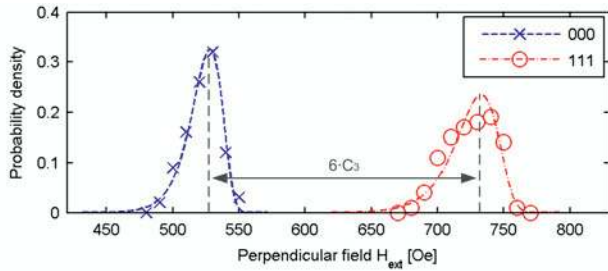
Figure 7. Measured probability densities of $\overline{\mathrm{C_{out}}}$ for the ′000′ (inputs down) and the ′111′ input configuration (inputs up), separated by 6 times of $\mathrm{C_3}$ (input coupling of the 3-input gate).

ing behavior is described by a probability density function (PDF) [15, 18]. As described in section 2, the coupling fields of the input magnets superpose with the field pulse and therefore shift the PDF up or down. Certainly, for reliable computation those shifted PDFs have to be separated to clearly determine the magnets switching [7].

Fig. 7 shows the measured PDFs of $\overline{\mathrm{C_{out}}}$ for the ′000′ and the ′111′ input configuration. The means of those two PDFs are separated by 210 Oe, which is 6 times the coupling of each input of the 3-input gate: $\mathrm{C_3 = 35\,Oe}$. Accordingly, we measured a coupling field of $\mathrm{C_5 = 27\,Oe}$ for each input of the 5-input gate, which is obviously not sufficient to separate the different PDFs. Additionally, the mean switching fields of both output magnets $\mathrm{H_{c,\overline{C_{out}}} = 630\,Oe}$ and $\mathrm{H_{c,\overline{S}} = 620\,Oe}$ are slightly different, which further decreases the clocking window.

Therefore, great effort should be made in increasing the coupling and decreasing the SFDs, as they can be engineered by enhancing the material system and improving the fabrication technology. Both components exhibit great potential to increase the reliability of pNML circuitry. For instance, the coupling field can be dramatically increased by enhancing the total magnetic moment or reducing the distance between the inputs and the ANC according to eq.3. Simulations using compact modeling [20] show, that the coupling of each input has to be increased to $\mathrm{C_x = 60\,Oe}$ to reduce the error rate to $\mathrm{e} < 10^{-3}$. Consequently, distances between inputs and ANCs have to be reduced to $\mathrm{d} < 20\,\mathrm{nm}$ to provide definite and reliable computation using TLG-based pNML.

5 Conclusion

Perpendicular NML is highly suitable to implement threshold logic based circuits. Majority gates offer the possibility to weight each input by its coupling field, which is defined by the inputs geometry and distance to the ANC. Hence, a very straight and efficient way to realize TLG-based circuits is combined with advantages of pNML, e.g. non-volatility and low-power computing.

In this paper, we experimentally demonstrate a TLG-based 1-bit full adder circuit using a novel 5-input majority gate. Here, the geometry and the distance of each input in the gate is kept constant, but one input signal is connected to two physical input arms to double its influence.

Compared to former implementations of a full adder [10], the device footprint is reduced by 88.5 % (from $17\,\mu\mathrm{m}^2$ to $1.95\,\mu\mathrm{m}^2$) and the maximum device speed is increased by 200 % (smaller magnets and less clocking cycles).

Acknowledgements

References

1. The International Technology Roadmap for Semiconductors (ITRS): Emerging Research Devices (ERD), http://www.itrs.net (2013)
2. G. Csaba et al., IEEE Transactions on Nanotechnology **1**, 209-213 (2002)
3. M. Becherer et al., Digest Technical Papers IEEE International Solid-State Circuits Conference (ISSCC), 474-475 (2009)
4. M. Niemier et al., Proceedings of the 13th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA), 59-64 (2012)
5. S. Breitkreutz et al., Journal of Applied Physics **111**, 07A715 (2012)
6. S. Breitkreutz et al., Proceedings of the 41st IEEE European Solid-State Device Research Conference (ESSDERC), 323-326 (2011)
7. I. Eichwald et al., IEEE Transactions on Magnetics **48**, 4332-4335 (2012)
8. J. Kiermaier et al., Journal of Applied Physics **113**, 17B902 (2013)
9. S. Breitkreutz et al., IEEE Transactions on Magnetics **48**, 4336-4339 (2012)
10. S. Breitkreutz et al., IEEE Transactions on Magnetics **49**, 4464-4467 (2013)
11. I. Eichwald et al., IEEE Transactions on Magnetics **49**, 4468-4471 (2013)
12. J. Kiermaier et al., EPJ Web of Conferences **40**, 16007 (2013)
13. J. Kiermaier et al., Journal of Applied Physics **111**, 07E341 (2012)
14. S. Mangin et al., Nature Materials **5**, 210-215 (2006)
15. M. Becherer et al., Proceedings of the 43rd IEEE European Solid-State Device Research Conference (ESSDERC), 276-279 (2013)
16. A. Papp et al., "Threshold gate based circuits from Nanomagnetic Logic", submitted to IEEE Transactions on Nanotechnology, (2013).
17. J. H. Franken et al., Journal of Physics: Condensed Matter **24**, 024216 (2012)
18. J. Engelen et al., Nanotechnology **21**, 035703 (2010)
19. G. Csaba et al., Proceedings of the 14th International Workshop on Computational Electronics (IWCE), (2010)
20. S. Breitkreutz et al., Journal of Computational Electronics **10**, 352-359, (2011)
21. D. Hampel et al., IEEE Spectrum **8**, 32-39 (1971)