

# $1/f$ Noise in Drain and Gate Current of MOSFETs With High- $k$ Gate Stacks

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**Abstract**—In this paper, we investigate the quality of MOSFET gate stacks where high- $k$  materials are implemented as gate dielectrics. We evaluate both drain- and gate-current noises in order to obtain information about the defect content of the gate stack. We analyze how the overall quality of the gate stack depends on the kind of high- $k$  material, on the interfacial layer thickness, on the kind of gate electrode material, on the strain engineering, and on the substrate type. This comprehensive study allows us to understand which issues need to be addressed in order to achieve improved quality of the gate stack from a  $1/f$  noise point of view.

**Index Terms**—Drain noise, gate noise, high- $k$  dielectric, MOSFET,  $1/f$  noise.

## I. INTRODUCTION

THE RELENTLESS push for more and faster devices on a chip in CMOS technology is driving the demand for shrinking geometries. The accompanying gate dielectric thickness decrease leads to a large gate-current leakage due to quantum mechanical tunneling of carriers through the thin gate oxide [1], [2] and, therefore, to higher static power dissipation. That problem is alleviated in novel gate stacks by introducing high- $k$  materials in order to achieve the same gate dielectric capacitance of conventional SiO<sub>2</sub> with a thicker dielectric layer. It should be noted that, for decades, the quality of the silicon/silicon dioxide interface was a strong point of the silicon technology and a lot of effort has been put in order to replace the silicon dioxide with high- $k$  dielectrics. Difficulties arise in order to address typical issues like threshold voltage shift, mobility reduction, bias temperature instability, and stress-induced leakage current, which are common in high- $k$  materials [3], [4]. On the other hand, several studies have shown that low-

frequency drain-current noise measurements represent one of the most powerful tools to investigate the material defectiveness [5]–[14]; therefore, noise analysis is very useful to validate the quality of the gate stack when new materials are introduced. Furthermore, a new model has been recently proposed in [15], where it is shown that low-frequency gate-current  $1/f$  noise can also be used as a source of information for assessing the quality of the gate stack in MOS structures. This investigation technique is very suitable in the case of large gate-current leakage, where the accuracy of most traditional techniques (combination of high-frequency and quasi-static  $C$ - $V$  [16], charge pumping [17], [18], and drain noise measurements) could be corrupted. The idea behind this model [15] is that the charging/discharging of defects in the dielectric can block/unblock effective portions of the gate area, thus causing a fluctuation in the gate current. With this in mind, the gate noise is proportional to the total amount of traps that can be charged/discharged in the dielectric.

In this paper, both drain- and gate-current noise measurements are used to check the quality of high- $k$  gate stacks in MOSFETs. In order to better localize the sources of gate-stack quality degradation, the impact on noise of several parameters is exploited: high- $k$  material, interfacial layer (IL) thickness, gate electrode material, strain engineering and substrate material.

The remainder of this paper is organized as follows. In Section II, the details about the typical high- $k$  dielectrics investigated and about the measurement system are given. In Section III, the methodology utilized for data elaboration and interpretation is described. In Section IV, the experimental results are shown, and in Section V, the main conclusions are summarized.

## II. EXPERIMENTAL

In this paper, we examined Hf-based dielectrics as replacement materials of conventional SiO<sub>2</sub> or SiON. In particular, two types of high- $k$  dielectrics were used in the gate stacks investigated: HfO<sub>2</sub> or HfSiON with different percentage of hafnium. These materials were deposited by means of atomic layer deposition (ALD) or metallo-organic chemical vapor deposition (MOCVD) [2]. Furthermore, a SiO<sub>2</sub> or SiON stratum was comprised between the substrate and the high- $k$  dielectric as an IL.

Noise measurements were done on MOSFETs by means of a specially designed instrumentation setup [19]. Drain-current noise measurements were carried out in linear region with

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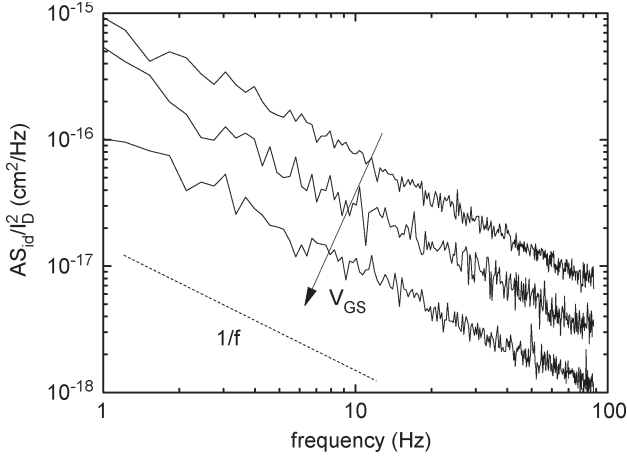


Fig. 1. Drain-current noise spectra normalized with respect to the device area and the dc drain-current square. Typical  $1/f$  spectra are observed for different  $V_{GS}$  values.

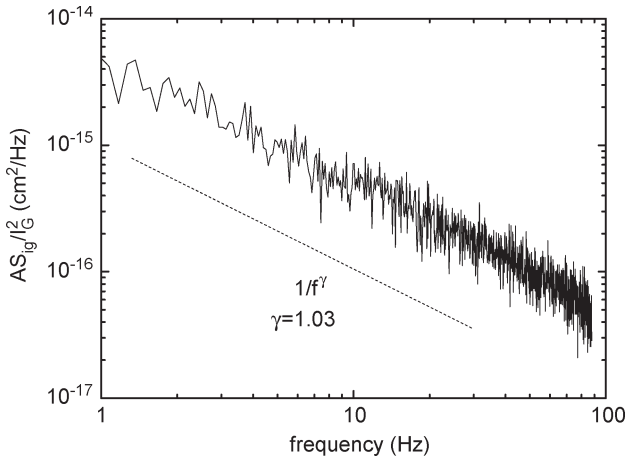


Fig. 2. Gate-current noise spectrum normalized with respect to the device area and the dc gate-current square. By fitting the spectrum with a  $1/f^\gamma$  law, the coefficient  $\gamma$  is found to be very close to one ( $\gamma = 1.03$ ).

the drain-to-source voltage  $V_{DS} \leq 50$  mV, while for the gate-current noise measurements,  $V_{DS} = 0$  V was applied. Static characterization was performed with a 4200-SCS Keithley parameter analyzer in order to measure  $I_D$ - $V_{GS}$  and  $I_G$ - $V_{GS}$  curves and then to extract typical parameters such as transconductance  $g_m$  and threshold voltage  $V_T$ .

### III. DATA ANALYSIS METHODOLOGY

In this paper, the spectra were measured for both drain- and gate-current noises. The typically observed spectra are shown in Figs. 1 and 2 for the drain and gate currents, respectively. In both cases, a  $1/f$ -like noise is found. The obtained power spectral densities are then fitted with a law  $1/f^\gamma$  in a frequency range of 1 decade, and the coefficients  $\gamma$ 's are extracted. It can be easily checked that in Figs. 1 and 2,  $\gamma$  is close to one. Moreover, the dc drain and gate currents are measured at the same time.

All the data reported in this paper are extracted in samples exhibiting  $1/f$  noise. In the following, we will show how these measurements are treated, in order to obtain a figure of merit for the MOSFETs investigated.

#### A. Drain Current

The drain-current power spectral density  $S_{id}$  normalized with respect to the square of the dc drain current  $I_D$  and with respect to the channel area  $A = WL$  is measured in the frequency range of 1–100 Hz and evaluated at a fixed frequency ( $f = 25$  Hz) as a function of the gate voltage overdrive. In order to understand which mechanism dominates the drain flicker noise, a common method consists in checking the normalized  $S_{id}$  dependence on the gate voltage overdrive ( $V_{OV} = V_{GS} - V_T$ ) with the MOSFET biased in the linear region. When  $A \cdot S_{id}/I_D^2 \propto (1/N)^2 \propto 1/(V_{GS} - V_T)^2$ , where  $N$  is the number of electrons in the channel, the noise is attributed to the fluctuation of charge carriers which are trapped and detrapped by oxide traps [7], [20], [21]. Otherwise, if  $A \cdot S_{id}/I_D^2 \propto 1/N \propto 1/(V_{GS} - V_T)$ , the noise is attributed to the fluctuation of the mobility in the inversion layer [5]. Moreover, correlated carrier number/mobility fluctuation is also possible in the middle case [6], [21]. Based on the dominant source of noise, a different figure of merit can be computed.

If carrier number fluctuation dominates, then the trap density in the dielectric per unit energy and unit volume can be extracted as [7]

$$N_t = \frac{S_{id} C_{EOT}^2 W L f (V_{GS} - V_T)^2 \gamma}{q^2 k T I_D^2} \quad (1)$$

where  $q$  is the elementary electron charge,  $kT$  is the thermal energy,  $\gamma$  is the attenuation coefficient [7], and  $C_{EOT}$  is the gate dielectric capacitance per unit area. Conversely, from the study in [6], the  $g_m$  dependence on the gate voltage overdrive [14] is taken into account. In (1), the trap density is supposed to be uniform in energy and in space. Moreover, the traps are considered to be situated close to the channel interface. These assumptions are not verified in the case of multistack gates. Therefore, in this case, the trap density should be read as an effective number.

If mobility fluctuation dominates, then the so-called Hooge parameter can be extracted as [11]

$$\alpha_H = \frac{W L S_{id} f C_{EOT} (V_{GS} - V_T)}{I_D^2 q} \quad (2)$$

#### B. Gate Current

The gate-current power spectral density  $S_{ig}$  is measured in the frequency range of 1–100 Hz, and taken at a fixed frequency ( $f = 1$  Hz) and in accordance with the study in [15], a figure of merit for the quality of the gate stack can be extracted as

$$GNP \equiv \frac{S_{ig} f A}{I_G^2} \quad (3)$$

where  $I_G$  is the dc gate current and  $GNP$  is defined as the gate noise parameter. The extracted value is independent on the gate area and on the bias point in the case of a uniform energy distribution of traps. It is worth noting that the frequency value chosen does not influence the  $GNP$  since this analysis applies for  $1/f$  noise spectra.

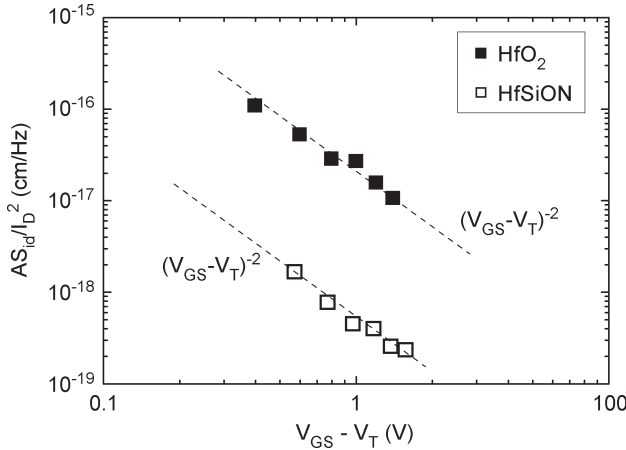


Fig. 3. Normalized drain-current spectral density at  $f = 25$  Hz as a function of the gate voltage overdrive for different high- $k$  dielectrics. In the measured devices, the channel width was  $10 \mu\text{m}$ , while the channel length ranged from  $0.18$  to  $0.25 \mu\text{m}$ . N-MOSFETs with  $\text{HfO}_2$  dielectric show 1 decade higher noise than the ones with  $\text{HfSiON}$ .

Note that the expression of the GNP is similar to the Hooge parameter, generically defined as

$$\alpha_H \equiv \frac{S_i f N}{I^2} \quad (4)$$

where  $N$  is the total number of charge carriers and  $I$  is the dc current. As discussed previously, the Hooge parameter is widely used in the case of the drain noise measurements, where  $N$  is proportional to the gate area  $A$ . Thus, the only difference between the two definitions is that the Hooge parameter contains an additional factor corresponding to the number of charge carriers per unit area. The reason why the GNP is not normalized for this factor is that experimental data show that the GNP is quite independent on the bias point and thus on the number of charge carriers per unit area [15].

The GNP has a twofold meaning. On one hand, it can be considered as an empirical parameter for the measurement of the normalized gate noise. On the other hand, it can be related to physical quantities of the gate stack on the basis of the model proposed in [15]. In the last case, the GNP is proportional to the trap density in the dielectric.

#### IV. EXPERIMENTAL RESULTS

##### A. Impact of High- $k$ Material

N-channel MOSFETs with two different gate stacks were compared: a double layer consisting of a  $4.5\text{-nm}$   $\text{HfO}_2$  film on the top of a  $1\text{-nm}$   $\text{SiO}_2$  IL with an EOT (equivalent oxide thickness) of  $1.7 \text{ nm}$  and a double layer formed by a  $2\text{-nm}$   $\text{Hf}_x\text{Si}_{1-x}\text{ON}$  ( $x=0.23$ ) film on the top of a  $1\text{-nm}$   $\text{SiON}$  IL with an EOT of  $1.6 \text{ nm}$ . Both devices were polysilicon gated [14].

From the drain point of view, two main observations can be made based on the results in Fig. 3. First, the normalized drain-current noise magnitude for the  $\text{HfO}_2$  gate stack is significantly higher with respect to the  $\text{HfSiON}$  one, thus indicating a worsening of noise behavior when the Hf content is increased. Second, it is clear that in both gate stacks, the  $1/f$  noise dominating

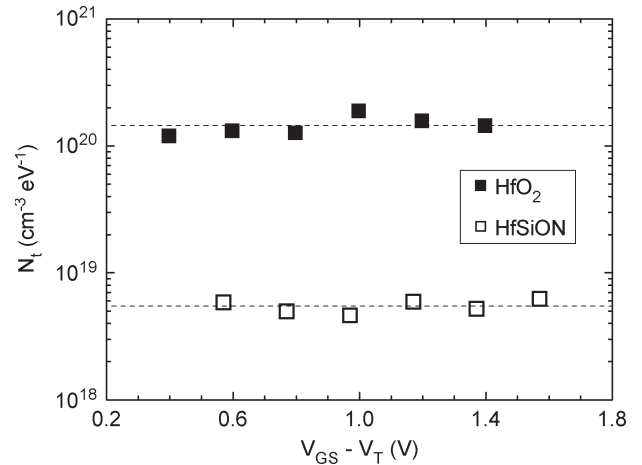


Fig. 4. Trap density per unit volume and unit energy as a function of the gate voltage overdrive. The channel width was  $10 \mu\text{m}$ , while the channel length ranged from  $0.18$  to  $0.25 \mu\text{m}$ . Lower defect density can be observed in the case of  $\text{HfSiON}$  dielectric because of the lower hafnium content with respect to the  $\text{HfO}_2$  dielectric.

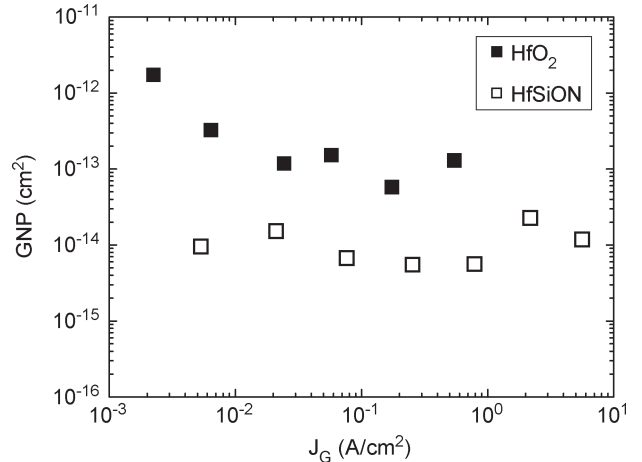


Fig. 5. GNP as a function of the gate-current density for  $\text{HfO}_2$ - and  $\text{HfSiON}$ -based dielectrics. The channel width was  $10 \mu\text{m}$ , while the channel length ranged from  $0.18$  to  $0.25 \mu\text{m}$ . The observed GNP values indicate an improved quality of the gate stack for the  $\text{HfSiON}$  samples.

mechanism is carrier number fluctuation since  $A \cdot S_{id}/I_D^2 \propto 1/(V_{GS} - V_T)^2$ . Under this supposition, the trap density  $N_t$  can be extracted by using (1), and the results are shown in Fig. 4. The defect density in the  $\text{HfO}_2$  layer ( $10^{20} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ ) is more than one decade higher with respect to the case of  $\text{HfSiON}$  gate stacks ( $5 \times 10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ ). Typical trap density extracted for a MOSFET with a conventional  $\text{SiON}$  dielectric and similar EOT is comprised in the range of  $10^{17}$ – $10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$  [22], [23]. Therefore, an increase of defectivity in the gate dielectric is observed in both high- $k$  materials with respect to conventional  $\text{SiON}$ .

The GNP values extracted from gate noise measurements are shown in Fig. 5.  $\text{HfO}_2$  samples exhibit GNP values one decade larger with respect to the  $\text{HfSiON}$  ones. These results confirm what we observed for the drain noise data, i.e., a large trap density in the hafnium dioxide with respect to the hafnium silicate. In [15] and [24], it is shown that a typical value of GNP for a standard  $\text{SiON}$  gate dielectric is around  $10^{-16} \text{ cm}^2$ . That

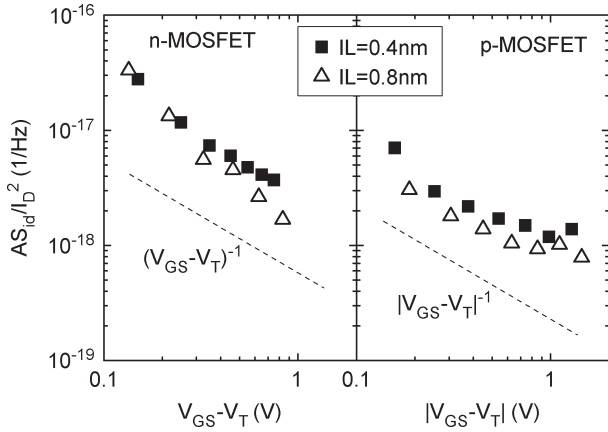


Fig. 6. Normalized drain-current spectral density at  $f = 25$  Hz as a function of the gate voltage overdrive for n-MOSFETs and p-MOSFETs having different IL thicknesses. All the MOSFETs under investigation had  $W = 10 \mu\text{m}$  and  $L = 1 \mu\text{m}$ . A slight increase of noise is observed reducing the IL thickness.

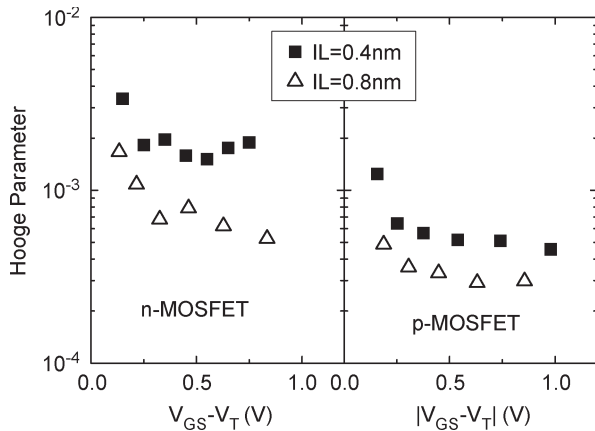


Fig. 7. Hooge parameter values extracted for n-MOSFETs and p-MOSFETs with different IL thicknesses. The MOSFETs had  $W = 10 \mu\text{m}$  and  $L = 1 \mu\text{m}$ . In both types of MOSFETs, the Hooge parameter increases when the IL decreases.

value is three orders of magnitude lower with respect to the  $\text{HfO}_2$  dielectric, while an intermediate value is observed for the hafnium silicate devices.

### B. Impact of IL

The low-frequency drain-current noise properties were investigated in n- and p-MOSFETs with two different  $\text{SiO}_2$  IL thicknesses: 0.4 and 0.8 nm. In both cases,  $\text{HfO}_2$  was deposited as high- $k$  dielectric. For p-MOSFETs, the overall EOT's obtained were 1.31 nm in the case of  $IL = 0.4$  nm and 1.35 nm for  $IL = 0.8$  nm, while for n-MOSFETs, EOT's were 0.92 nm for  $IL = 0.4$  nm and 1.44 nm for  $IL = 0.8$  nm. PVD TiN/TaN was employed as metal gate [25]. Fig. 6 shows the normalized drain-current noise spectral density dependence on the gate voltage overdrive. For n-MOSFETs, the normalized  $S_{id}$  varies as  $(V_{GS} - V_T)^{-1.5}$  for the 0.8-nm IL thickness, which highlights that noise is due to correlated number-mobility fluctuations, and  $(V_{GS} - V_T)^{-1}$  for 0.4 nm, which points out that noise is mainly due to mobility fluctuation. For p-MOSFETs, the noise mechanism points to Hooge's mobility model. For both types of MOSFETs, a small increase of noise is observed for reduced

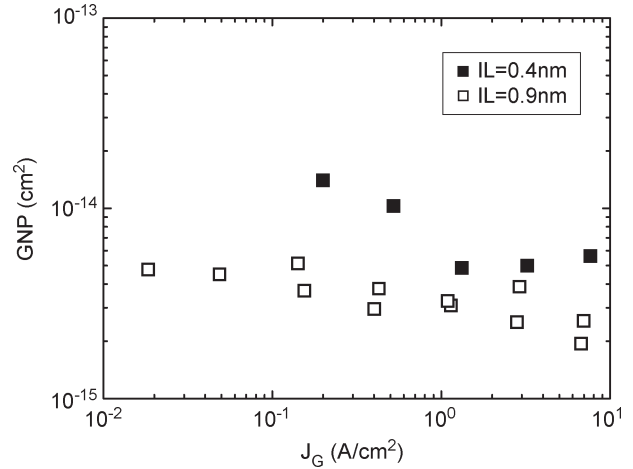


Fig. 8. GNP as a function of the gate-current density in n-MOSFETs with different IL thicknesses. In both cases, the channel width was  $10 \mu\text{m}$ , and the channel length was  $1 \mu\text{m}$ . The higher GNP for  $IL = 0.4$  nm points to a degradation of the quality of the gate stack with respect to  $IL = 0.9$  nm.

IL thickness. Nevertheless, if we look at the extracted Hooge's parameter in Fig. 7, the dependence on the IL thickness is more evident.

The gate-current noise measurements were performed on n-MOSFETs having the following gate stacks: 0.4 nm of  $\text{SiON}$  as interfacial layer,  $\text{HfO}_2$  as gate dielectric, and TiN/TaN as gate electrode ( $EOT = 0.9$  nm); 0.9 nm of  $\text{SiON}$  as interfacial layer,  $\text{HfO}_2$  as gate dielectric, and TiN as gate electrode ( $EOT = 1.4$  nm). The extracted GNP values are shown in Fig. 8. In accordance with the drain noise measurements, an increase of GNP is observed for a thinner interfacial layer thickness. These experimental observations suggest that bringing the high- $k$  layer closer to the Si-SiO<sub>2</sub> interface enhances the  $1/f$  noise in both gate and drain currents. Moreover, the enhanced  $1/f$  drain noise due to mobility fluctuations is consistent with the lower mobility values observed in high- $k$  gate stacks with lower IL thickness [26], [27].

### C. Impact of Gate Electrode

In order to understand the impact on noise of the interface between high- $k$  dielectric and gate electrode in MOSFET devices, a submonolayer of  $\text{HfO}_2$  was sandwiched between conventional  $\text{SiON}$  dielectric and polysilicon gate. N-MOSFETs and p-MOSFETs were fabricated with a conventional  $\text{SiON}$  dielectric. Before the polysilicon deposition as a gate, in some samples, a thin  $\text{HfO}_2$  layer was deposited by means of ALD, resulting in a partially closed film roughly 0.3 nm thick. The overall EOT was around 1.6 nm for both n-MOSFETs and p-MOSFETs [24].

In Fig. 9, the normalized drain-current noise is shown for both n-MOSFETs and p-MOSFETs. In the case of n-MOSFETs, the first observation that we can do is that at low gate voltage overdrive, the noise mechanism is dictated by carrier number fluctuation, while at high gate voltage, other effects become dominant like correlated carrier-mobility fluctuation or noise coming from the series resistance [28], [29]. Second, an increase of noise is observed in the regime of number

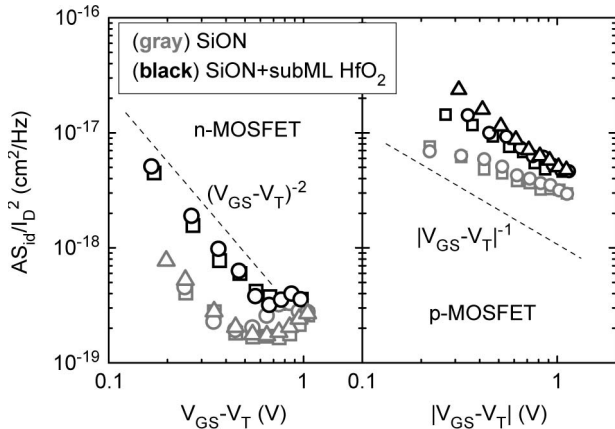


Fig. 9. Normalized drain-current spectral density at  $f = 25$  Hz as a function of the gate voltage overdrive in  $10\text{-}\mu\text{m}$ -wide and  $1\text{-}\mu\text{m}$ -long MOSFETs. A submonolayer of  $\text{HfO}_2$  is able to increase the noise in both n-MOSFETs and p-MOSFETs.

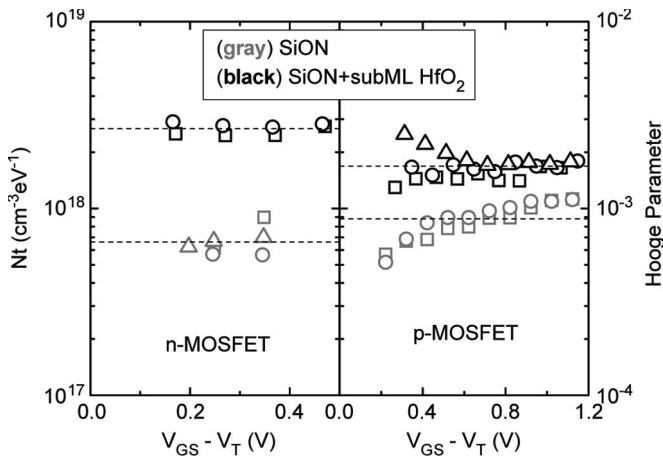


Fig. 10. Trap density and Hooge parameter extracted for n-MOSFETs and p-MOSFETs, respectively. Both figures of merit point to a large amount of defects at the interface between  $\text{HfO}_2$  and polysilicon.

fluctuation in the case of  $\text{HfO}_2$  submonolayer because of the high defect density close to the polysilicon gate. In Fig. 10, the trap density is extracted in the regime of number fluctuation, and an increase of  $2 \times 10^{18} \text{ cm}^{-3} \cdot \text{eV}^{-1}$  is observed in the samples with a submonolayer of  $\text{HfO}_2$ . It is worth noting that in these samples, the trap density value is just an effective value since the model behind (1) is based on the hypothesis that the defects are close to the silicon interface. For p-MOSFETs, the dominant noise mechanism in Fig. 9 seems to be mobility fluctuations in the whole range of bias conditions as usually observed in the case of p-MOSFETs [30], [31]. As suggested in [32], the different dominant noise mechanism in the case of p-MOSFETs with respect to n-MOSFETs can be explained because of the lower carrier mobility in the channel. Since the mobility fluctuation mechanism dominates in p-MOSFETs, it is expected that the remote phonon scattering due to the  $\text{HfO}_2$  submonolayer [33]–[36] should affect the drain-current noise. Nevertheless, that impact is much lower with respect to the case of n-MOSFETs. This is because the noise increase caused by the remote phonon scattering due to the  $\text{HfO}_2$  submonolayer is partially hidden by the high noise level due to the mobility

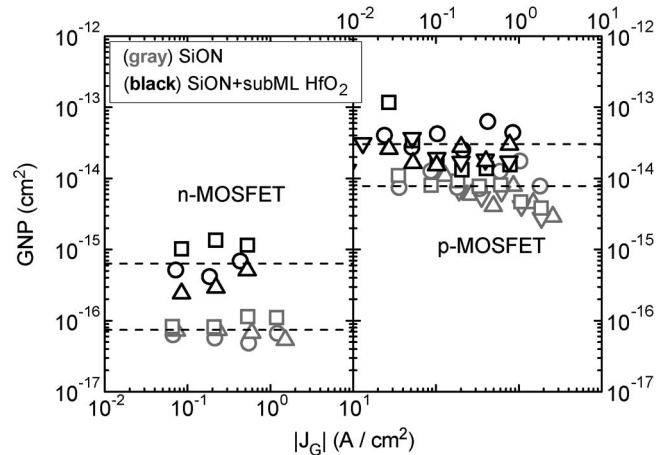


Fig. 11. GNP as a function of the gate-current density for n-MOSFETs and p-MOSFETs. In both cases, the channel width was  $10 \mu\text{m}$ , and the channel length was  $1 \mu\text{m}$ . The increase of noise due to the presence of  $\text{HfO}_2$  is more enhanced with respect to the one observed in Fig. 9. This is because the GNP is more sensitive to the traps close to the upper interface.

fluctuations coming from the lattice scattering. In Fig. 10, one can see that the presence of  $\text{HfO}_2$  at the interface with the polysilicon doubles the value of the Hooge parameter.

In Fig. 11, we can observe that the GNP for n-MOSFETs and p-MOSFETs increases with the presence of the submonolayer of  $\text{HfO}_2$ . Note that the relative increase in GNP is around 4 and 10 for p-MOSFET and n-MOSFET, respectively. The impact of the defects due to the  $\text{HfO}_2$  submonolayer is more evident in the case of gate-current noise than in the case of drain-current noise. This is because the traps far from the channel interface have a limited effect on the drain current, while the gate current is more sensitive to the traps close to the gate side, since they locally influence the potential barrier profile and then the carrier tunneling. Moreover, it is worth noting that noise levels are higher in p-MOSFETs, even in the reference devices. This result is in agreement with the study of Morfouli *et al.* [22]. They reported that in the case of SiON dielectric, p-MOSFETs show a larger trap density with respect to the n-MOSFETs. This can explain why p-MOSFETs have higher noise than n-MOSFETs.

Furthermore, in order to evaluate the impact of the kind of gate electrode, we can compare the previous experiments reported in Sections IV-A and B, where we investigated samples with the same  $\text{HfO}_2$  dielectric but with different gate electrode materials: polysilicon or metal. Comparing Figs. 3 and 6, it is clear that n-MOSFETs with polysilicon gate exhibit 1 decade larger drain noise with respect to the n-MOSFETs with metal gate. Moreover, also the GNP value in the case of polysilicon gate (Fig. 5) is 1 decade larger with respect to the one of metal gate (Fig. 8). This result further confirms the presence of a large defect density at the interface between the hafnium dioxide dielectrics and the polysilicon gates. Pantisano *et al.* [37] showed that this large amount of defects locally changes the electrostatic potential at the dielectric/gate electrode interface, causing unwanted effects such as a shift of the flatband voltage. Therefore, in the case of hafnium-based dielectrics, the interface with polysilicon strongly degrades the overall quality of the gate stack.

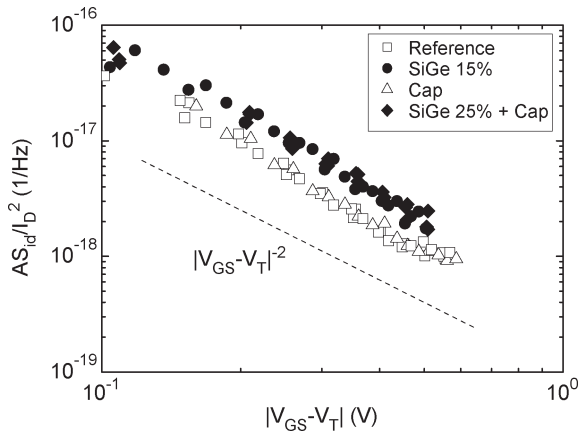


Fig. 12. Normalized drain-current spectral density at  $f = 25$  Hz as a function of the gate voltage overdrive for p-MOSFETs with different strain engineering: (□) Unstressed reference, (●) 15% SiGe S/D, (△)  $\text{Si}_3\text{N}_4$  cap layer, and (◆) 25% SiGe S/D +  $\text{Si}_3\text{N}_4$  cap layer. In all the cases, the investigated devices were  $10\ \mu\text{m}$  wide and  $1\ \mu\text{m}$  long.

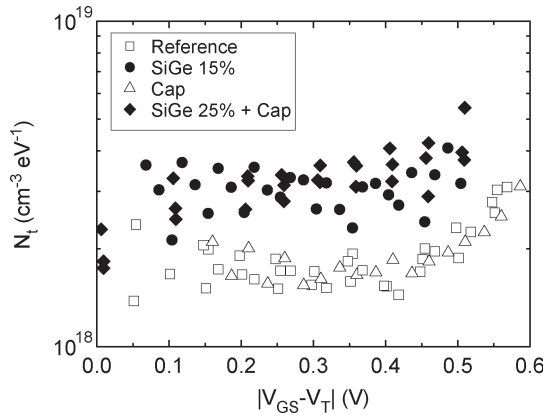


Fig. 13. Trap density for p-MOSFETs with different strain engineering. The devices were  $10\ \mu\text{m}$  wide and  $1\ \mu\text{m}$  long. No increase of defectivity in the gate stack is observed in the case of nitride cap layer.

#### D. Impact of Strain Engineering

The effect of the strain on the quality of the high- $k$  gate dielectric was analyzed by means of drain-current noise measurements in p-MOSFET devices with different strain techniques. The gate stack of the p-MOSFETs consists of 1.8–2 nm of  $\text{HfO}_2$  layer deposited by ALD on a 1.2–1.4-nm chemical oxide IL, resulting in an EOT of around 2.1 nm. A 4-nm-thick TiN gate electrode was fabricated by MOCVD, followed by the deposition of 100-nm polysilicon. Aside from unstressed reference devices, three different kinds of strain engineering were implemented: 15% SiGe recessed S/D regions, 100-nm nitride cap layer with 1.5-GPa compressive intrinsic stress, and a combination of recessed S/D (25% SiGe) and cap layer [38]–[41].

Comparing the normalized drain-current spectral density, some interesting trends can be found in Fig. 12. First, from the quadratic dependence of the normalized noise on the gate voltage overdrive, one can conclude that the  $1/f$  noise is dictated by number fluctuations. A second clear trend is that for SiGe S/D devices, the noise is significantly higher with respect to the reference devices. Moreover, this increase is not depending on the % Ge. Third, no degradation of the noise was

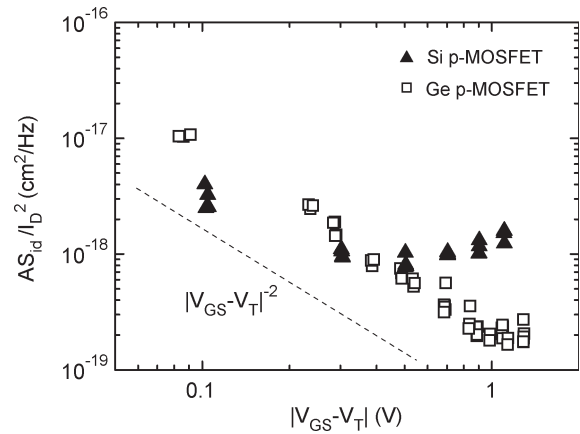


Fig. 14. Normalized drain-current spectral density at  $f = 25$  Hz as a function of gate voltage overdrive for p-MOSFETs with different substrates: Silicon or germanium. For both devices, we investigated channel widths of  $10\ \mu\text{m}$  and channel lengths of  $1\ \mu\text{m}$ . The noise seems to be slightly higher for Ge p-MOSFETs at low gate voltage overdrive.

found for the cap-only devices. The extracted trap densities are reported in Fig. 13. Here, it is possible to observe how the defect content increases when SiGe S/D strain is implemented.

From this experiment, we can conclude that it is possible to implement strain in p-MOSFETs without degradation in the high- $k$  gate stack, by using a nitride cap layer. On the other hand, the additional selective epitaxial deposition step for fabricating the recessed SiGe S/D can induce a worsening of the quality of the high- $k$  gate stack.

#### E. Impact of Substrate Material

In the last years, MOSFETs on germanium, owing to their high charge carrier mobility, are gaining interest as a replacement of the MOSFET with a silicon substrate. In order to evaluate the impact of such a new channel material on the high- $k$  gate stack, noise properties of p-MOSFETs with Si and Ge substrates are compared in this paper when similar gate stacks are implemented. Ge p-MOSFETs were fabricated by using a standard Si-compatible process flow, and the gate stacks comprised as follows:  $1.6\ \mu\text{m}$  of Ge grown by chemical vapor deposition; 0.8 nm of Si as passivation layer, partially oxidized to form a thin  $\text{SiO}_2$  IL;  $\text{HfO}_2$  deposited by ALD; and 10 nm of TaN capped with 100 nm of TiN for the metal gate. The Si p-MOSFET gate stack consisted of the following:  $\text{SiO}_2$  as IL,  $\text{HfO}_2$  as high- $k$  gate dielectric, and TiN as metal gate. The EOT values were 1.3 and 1.2 nm for Ge MOSFETs and Si MOSFETs, respectively [42].

The drain-current noise measurements are reported in Fig. 14 where one can observe that different mechanisms generate the drain-current noise. In the case of a Si substrate, mobility fluctuation dominates, even if at high gate voltage overdrive, the normalized noise increases, probably because of the parasitic series resistance [28]. On the other hand, Ge p-MOSFETs are clearly dominated by carrier number fluctuation.

Although, in Fig. 14, only a slight increase in drain-current noise is observed in the case of Ge p-MOSFETs, in Fig. 15, the GNP for Ge p-MOSFETs is found to be more than two orders of magnitude higher with respect to the Si p-MOSFETs. Ge

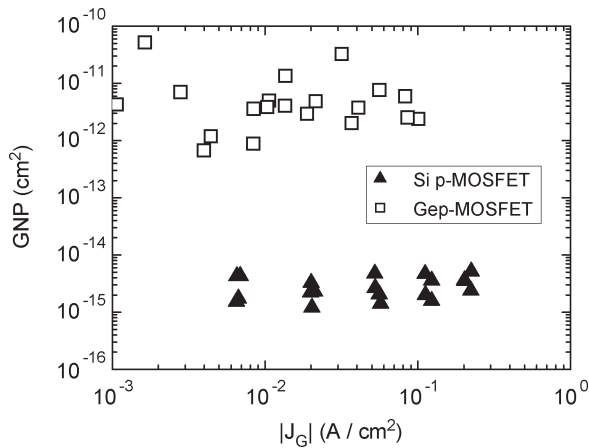


Fig. 15. GNP as a function of the gate-current density for p-MOSFETs with different substrates: Silicon and germanium. The channel widths were  $10\ \mu\text{m}$ , and channel lengths were  $1\ \mu\text{m}$ . A strong degradation of the figure of merit is observed in the case of Ge p-MOSFETs.

outdiffusion can be considered as one of the causes for the lower quality of the gate dielectric when deposited on Ge. In fact, the outdiffused Ge acts as a trap center inside the gate oxide. Hence, a higher gate-current noise is observed in Ge p-MOSFETs.

## V. CONCLUSION

In this paper, we have studied the drain- and gate-current noises of MOSFET devices with high- $k$  gate stacks. We have observed that the use of high- $k$  dielectric such as hafnium dioxide degrades the quality of the gate stack. The trap density in the gate stack can be reduced when using other high- $k$  dielectrics with less hafnium content, like HfSiON. In addition, we have proved that the degradation of the noise performance is not only ascribed to the kind of dielectric implemented. The IL thickness plays a significant role since the closer the high- $k$  layer to the channel interface, the higher the noise in both drain and gate currents. Moreover, we have shown that the interface between the high- $k$  dielectric and gate electrode is a key element in the overall quality of the gate stack. Even a submonolayer of HfO<sub>2</sub> sandwiched between the SiON dielectric and polysilicon gate is able to increase significantly both drain- and gate-current noises. However, much better quality of gate stack can be achieved by using a metal gate as a replacement of conventional polysilicon. We have shown that strain engineering in p-MOSFETs can be implemented by means of nitride cap layer without changing the overall quality of the high- $k$  gate stack. The experimental results (in particular, the gate-current noise measurements) have also highlighted that in the case of a germanium channel, the quality of the high- $k$  gate stack is degraded with respect to the silicon counterpart.

In addition to conventional noise figure of merits extracted from the drain  $1/f$  noise measurements, the GNP has been used in order to characterize the quality of the gate stack from gate-current  $1/f$  noise measurements. The main advantage of using the gate-current  $1/f$  noise as diagnostic in MOS structures is its intrinsic immunity to the large gate leakage, which can corrupt the accuracy of all the other conventional methods. Moreover, we have seen in different experiments that the GNP value is

more sensitive to the traps far from the channel interface with respect to drain-current  $1/f$  noise measurements.

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