$1/f$ Noise in MOS Devices, Mobility or Number Fluctuations?

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Invited Paper

***Abstract*—Recent experimental studies on $1/f$ noise in MOS transistors are reviewed. Arguments are given for the two schools of thought on the origin of $1/f$ noise. The consequences of models based on carrier-number ΔN or mobility fluctuations $\Delta\mu$ on the device geometry and on the bias dependence of the $1/f$ noise are discussed. Circuit-simulation-oriented equations for the $1/f$ noise are discussed.**

The effects of scaling down on the $1/f$ noise is studied in the ohmic region as well as in saturation. In the ohmic region the contribution of the series resistance often can be ignored. However, in saturation the noise of the gate-voltage-dependent series resistance on the drain side plays a role in lightly doped drain LDD mini-MOST's. Surface and bulk p-channel devices are compared and the differences between n-and p-MOST's often observed will be discussed.

The relation between degradation effects by hot carriers or by γ-irradiation on the one hand and the $1/f$ noise on the other is considered in terms of a ΔN or $\Delta\mu$.

Experimental results suggest that $1/f$ noise in n-MOST's is dominated by ΔN while in p-MOST's the noise is due to $\Delta\mu$.

I. Introduction

A GENERALLY accepted model explaining the $1/f$ noise in all p- and n-channel MOS transistors is still lacking. The increase of $1/f$ noise through degradation by hot carriers or irradiation is often used as a proof for the surface and, hence, a number fluctuation ΔN origin of the $1/f$ noise. However, the majority of results obtained not on n-channel MOS transistors but on homogeneous semiconductors and p-MOST's can be described by an empirical relation [1]–[3]

$$\frac{S_G}{G^2} = \frac{\alpha}{Nf} \tag{1}$$

where α is not a constant [2] but a volume and device-length independent [3], [4] $1/f$ noise parameter between 10^{-7} and 10^{-3}. A systematic study by Chang, Abidi and Viswanathan [3] of flicker noise in CMOS transistors from twelve different fabricators (in three continents) shows that for modern p-channel devices holds $10^{-7} < \alpha < 10^{-4}$. N is the total number of free charge carriers in a homogeneous sample with perfect contacts, or it is a well defined reduced number in samples submitted to nonuniform fields [5] as is often the case in contacts.

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The usefulness of (1) lays in the fact that a comparison in $1/f$ noise in α-values is made independent of bias, frequency and size of the device. The misuse of (1) to calculate α values from experimental results by overlooking the nonuniform current densities on a microscopic scale and replacing $1/N$ by $q\mu R/L^2$, always leads to overestimation of apparent α-values as was shown by Vandamme [2], [3], [5]. The equation $1/N = q\mu R/L^2$ with q the elementary charge, μ the mobility, R the sample resistance and L the length between the contacts, only holds for homogeneous fields in homogeneous samples. The empirical relation (1) has been applied successfully for p-n diodes and bipolar transistors by Kleinpenning [3], [6], [7].

The MOS transistor is an interface dominated device par excellence. The $1/f$ noise of n-MOST's has been described successfully by carrier-number fluctuations ΔN, which are caused by tunneling of free-charge carriers into oxide traps close to the Si-SiO_2 interface. Classical arguments in favor of the McWhorter model are the observed proportionality between trap density and $1/f$ noise [8]–[10]. Recent evidence for the ΔN origin of $1/f$ noise in MOS transistors are the change in $1/f$ noise through degradation by hot electrons [11]–[18] or by ionizing irradiation [19]–[30]. The p-MOS transistor often has a channel at a larger distance from the interface and is less noisy [4], [31], [32]. This is often easier to interpret in terms of $\Delta\mu$ than in terms of ΔN [4], [33].

Here, we discuss both points of view and explain why the $1/f$ noise in MOS transistors is still a problem that gives rise to much controversy. Therefore first, geometry and bias dependence will be discussed. From the analysis of geometry dependence we can discriminate between the contributions of the series resistance and the channel. This analysis has to be done before we can discriminate between the number fluctuation formalism and the mobility fluctuation. The ΔN or $\Delta\mu$ origin of $1/f$ noise is suggested by its gate voltage dependence. Some circuit-simulation-oriented equations for the $1/f$ noise in MOST's are discussed in terms of ΔN or $\Delta\mu$. Then some hot carrier degradation experiments will be discussed in view of ΔN or $\Delta\mu$. At last the correlation between $1/f$ noise and radiation hardness for n-channel MOST's will be discussed.

II. Geometry and Bias Dependence in View of ΔN or $\Delta\mu$

The geometry dependence of the $1/f$ noise in submicron MOST's is a diagnostic tool to discriminate between channel

and series resistances noise. Only if series resistance contributions can be ignored, the straightforward circuit-simulation-oriented (9)–(12) can be applied successfully.

The $1/f$ noise parameter α is used in our analysis as a figure of merit and not to suggest a $\Delta\mu$ origin of the $1/f$ noise. Its value is gate-length independent for both models [4]. For the sake of simplicity, in this section we assume no series resistance or edge current problems. This results in generally accepted dependence between the $1/f$ noise in MOST's and the channel area [8]; the dependence on oxide thickness is still under discussion. We start from the empirical relation (1) and do not suggest $\Delta\mu$ fluctuations. The empirical relation is well found for p-MOST's as shown by Chang *et al.* [3]. For n-MOST's we still use the empirical relation but with a gate-voltage dependent α-value as given by (8) in this section. From (1) and $N = C_{ox}V_G^*WL/q$ and the simple current-voltage equations, we find the calculated $1/f$ noise for MOST's biased above threshold voltage [34], [35]. Ignoring the α dependence on scattering we find:

1) Below saturation ($V < V_s$, $I < I_s$) with V_s the drain saturation voltage and I_s the saturation current, for the relative noise in the current

$$\frac{S_I}{I^2} = \frac{\alpha q \mu R}{L^2 f} = \frac{\alpha q}{C_{ox}V_G^* WLf} \propto \frac{1}{WL}. \tag{2}$$

Hence for different MOST's on the same chip at a fixed gate voltage bias we expect the relative noise in current or voltage to be inversely proportional to $1/WL$. For S_I we find with (2) using $I = (W/L)\mu C_{ox}V_G^*V$ and $R = V/I$:

$$S_I = \frac{\alpha q \mu^2 C_{ox}V_G^* V^2 W}{fL^3} \propto \frac{W}{L^3}. \tag{3}$$

In the above, μ is the mobility, V_G^* the effective gate voltage, V the drain voltage, R the channel resistance, C_{ox} the oxide capacitance per unit area, W and L the channel width and length respectively. The Eq. (3) shows that S_I at fixed V_G^* and V is proportional to W/L^3. In the ohmic region $V < V_G^*/10$ holds, $S_I/I^2 = S_V/V^2 = S_R/R^2 = S_G/G^2$. In open circuit S_v is measured and in short circuit condition (a voltage source without series resistance with the sample) S_I is measured.

2) In saturation we find a reduced free carrier number of 2/3 N with N the number of carriers at zero drain source voltage. The relative current noise S_{Is}/I_s^2 is twice the value of S_I/I^2 in the ohmic region at the same effective gate voltage for the $\Delta\mu$ model [35]. For the ΔN model [36], provided $N \ll N_t$ the ratio $(S_{Isat}/I_{sat}^2)/(S_I/I^2) = 2$. We chose for a factor two in our analysis which is in agreement with both models and which is often observed. Ignoring the series resistance and body effect we expect for the saturation current in first order approximation $I_s = (W/L)\mu C_{ox}V_G^{*2}/2$. The L and W dependence of the 1/f noise in the saturation current as a function of V_G^* [35] then becomes

$$S_{I_S} \cong \frac{2\alpha I_s^2}{Nf} = \frac{\alpha q \mu^2 C_{ox}V_G^{*3}}{2}\frac{W}{L^3 f} \propto \frac{W}{L^3}. \tag{4}$$

For S_{Is} versus I_s we then obtain

$$S_{I_s} \cong \frac{2^{1/2}\alpha q \mu^{1/2} I_s^{3/2}}{W^{1/2}C_{ox}^{1/2}L^{3/2}f} \tag{5}$$

only if α is V_G^* independent holds for an array of MOST's biased at fixed I_s, $S_{Is} \propto 1/W^{1/2}L^{3/2}$.

Equations (4) and (5) show the difference in W, L dependence of S_{Is}, depending whether or not V_G^* or I_s was kept constant in the comparison between different geometries. A comparison under constant V_G^* results for both models in $S_{Is} \propto W/L^3$. Under constant saturation current a different dependence is to be expected (5).

For the equivalent input noise voltage $S_{V_{eq}} = S_{Is}/g_m^2$ as a function of V_G^* we find [35] from (4) and the simple expression for transconductance $g_m = \partial I_s/\partial V_G^* = (W/L)\mu C_{ox}V_G^*$

$$S_{V_{eq}} \cong \frac{\alpha q V_G^*}{2WLC_{ox}f} \propto \frac{1}{WL} \tag{6}$$

or for $S_{V_{eq}}$ as a function of saturation current I_s

$$S_{V_{eq}} = \frac{\alpha q I_s^{1/2}}{2^{1/2}(WC_{ox})^{3/2}(L\mu)^{1/2}f} \tag{7}$$

only for α V_G^* independent holds at fixed I_s, $S_{V_{eq}} \propto 1/W^{3/2}L^{1/2}$.

From (3), (4), and (6) it is clear that submicron MOST's are notorious for their $1/f$ noise. To minimize the device thermal noise, very large width to length ratios are used as can be seen from (20) in [10] and (2) in [31].

The $1/f$ noise of devices with different channel areas and W/L ratios have been compared with the proportionalities given in (2)–(7). If the devices do not suffer from important series resistance contributions [27], [28], [33], [37]–[39] or channel edge currents and the electrical dimensions L and W are used in (2)–(7) and the devices are biased at fixed effective gate voltages instead of fixed saturation currents, no deviations between calculated (2)–(4) and (6) and observed LW dependence are seen [4], [8], [31].

In Fig. 1 experimental results in support of (3) are presented. In the ohmic region, S_I is proportional to V^2 and for a fixed drain and gate voltage, $S_I \propto W/L^3$, at least if we take the electrical channel length into account and do not use the mask length. The α value for these devices is inversely proportional to V_G^* in the ohmic region, because $S_I \propto \alpha V_G^*$ coincides for two different values of V_G^*. For this LDD MOST at saturation the typical ΔN behavior, with $S_{Isat} \propto \alpha V_G^{*3} \propto V_G^{*2}$, is not observed possibly due to complications of nonlinear series resistance at the drain [38], [39].

To discriminate between ΔN and $\Delta\mu$ models, the $1/f$ noise must be studied as a function of gate voltage because both models predict the same dependence on L and W at fixed V_G^*. If we consider $\Delta\mu$ here we do not have in mind the induced mobility fluctuations due to fluctuations in the oxide charge from trapping. The straightforward $\Delta\mu$ model predicts a gate voltage independent α value ($10^{-7} < \alpha < 10^{-3}$) if there: 1) is no appreciable mobility degradation with increasing bias voltages [10], [34], [35], 2) a uniform noise source under the SiO_2 can be assumed which is not always the case as can be

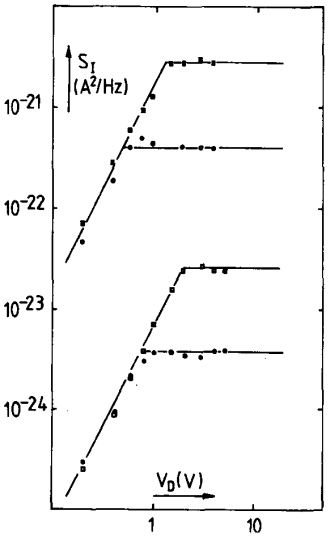

Fig. 1. Current noise S_I at $f = 10$ kHz versus drain source voltage V with the effective gate voltage$V_G^* = V_{GS} - V_T$ as a parameter. Two LDD n-MOST's having the same width but different length are compared at different gate voltage: ■ ($V_G^* = 2.3$ V, $W/L = 20/5$); ○ ($V_G^* = 1$ V, $W/L = 20/5$); □ ($V_G^* = 2.5$ V, $W/L = 20/20$); • ($V_G^* = 1.2$ V, $W/L = 20/20$). *(Reprinted from: L. K. J. Vandamme and X. Li, "1/f noise in MOS transistors due to number of mobility fluctuations," in Proc. Noise in Physical Systems and 1/f Fluctuations, St. Louis, MO, pp. 345–353, 1993).*

seen from Fig. 4 in [3] by Vandamme and [40], 3) the Si-SiO_2 interface is flat and there are no spatial charge nonuniformities in the oxide charge.

The above-mentioned conditions are based on experimental facts not on MOS transistors and some of them are well understood. These are not large "holes" to allow any result in terms of a refined $\Delta\mu$ model. The physical basis is at least that sound as a non uniform trap distribution used in refined ΔN models. These conditions are important because: 1) mobility degradation by scattering mechanism other than lattice scattering reduces the α parameter, as was shown for the first time by Hooge and Vandamme [1], [3], 2) reduced crystal quality results in high α values [3], [41], and 3) at low V_G^* spatial field fluctuations at the interface can induce cavities in the inversion layers. The Si-SiO_2 interface roughness and spatial field fluctuations result in a "Swiss-cheese" channel. An increased interface surface due to roughness results in an increased interface trap number. A Swiss-cheese channel leads to current constrictions and a marked increase in $1/f$ noise at lower V_G^*. By overlooking the nonuniform current density in the channel, an increasing apparent α value is obtained with decreasing V_G^*. The Swiss-cheese model easily explains 10% increase in resistance and a factor of 10 increase in $1/f$ noise, by taking an inhomogeneous current density into account in the same way as in [42]. Increasing cavity holes in the inversion layer with decreasing V_G^* is a good alternative to explain a dependence of $\alpha \propto V_G^{*-1}$ often interpreted as a proof for ΔN [10].

Here we propose to compare the outcomes of the $\Delta\mu$ and ΔN models in their straightforward form. In the straightforward $\Delta\mu$ model we ignore the consequences of an increase

TABLE I
EXPECTED PROPORTIONALITIES BETWEEN NOISE, GEOMETRY, V_G^*, AND T_{ox}

	ΔN $\alpha \propto t_{ox}/V_G^*$ (8)	$\Delta\mu$ α=constant $(\Theta V_G^* << 1)$	tgδ is constant [48]
S_I/I^2	$[T_{ox}^2 V_G^{*2}][1/WL]$ (2)	$[T_{ox} V_G^*][1/WL]$ (2)	no relation
S_{Isat}	$[V_G^{*2}][W/L^3]$ (4)	$[V_G^{*3}/T_{ox}][W/L^3]$ (4)	no relation
S_{Veq}	$[T_{ox}^2][1/WL]$ (6)	$[T_{ox}^2 V_G^*][1/WL]$ (6)	tg$\delta[T_{ox}/WL]$

in V_G^* on the $1/f$ noise parameter α. For the straightforward ΔN model we ignore the dependence of D_0 on V_G. This in contrast to more refined ΔN models [43], [44] explaining the dependence of $S_{V_{eq}}$ on V_G^* as a consequence of the dependence of $D_0(E_F)$ on V_G. The often observed peaks in $D_0(E_F)$ distribution near the band edges are apparent when using the Gray Brown [45] measuring method. Independently Declerck *et al.* [46] have demonstrated that spatial fluctuations in the oxide charge give apparent interface trap peaks near the band edges.

In the ΔN model we find for α [10]

$$\alpha = \frac{qx_0 D_0 kT(x_0/x_2)}{\epsilon_0 \epsilon_r} \frac{t_{ox}}{V_G^*} \doteq \frac{\alpha_r E_c t_{ox}}{V_G^*} \propto \frac{t_{ox} T}{V_G^*} \qquad (8)$$

where x_0 is the characteristic decay length of the electron wave function ($\approx$1 Å), $x_0 D_0 (\approx 10^{10}$ cm^{-2}(eV)$^{-1}$) trap density per unit area and unit energy, x_2 ($\approx$ 30 Å) the largest trapping distance resulting in a $1/f$ spectrum over 13 decades in frequency and ϵ_0 the permittivity of free space and ϵ_r the relative dielectric constant of the gate oxide. Here α_r is a reference value at a field strength of $V_G^*/t_{ox} = E_c$ which is a critical field strength. In the straightforward ΔN model $\alpha_r E_c$ is independent of V_G^* but $\alpha \propto 1/V_G^*$. The proportionality $\alpha \propto t_{ox} D_0 / V_G^*$ from (8) should be proof of the validity of the straightforward from the ΔN model in MOS transistors. The proportionality $\alpha \propto t_{ox}/V_G^*$ has its consequences for the bias and oxide-thickness dependence of the $1/f$ noise in (2)–(7). The expected proportionalities are summarized in Table I.

In the second column and second row is described the expected geometry and effective gate voltage dependence of the relative current noise in the ohmic region S_I/I^2 if the straightforward ΔN model holds. In the third column and the second row the proportionalities for S_I/I^2 are shown if the straightforward $\Delta\mu$ model holds. In the third and fourth row the proportionalities are presented for I_{Isat} or equivalent input noise voltage $S_{V_{eq}}$ for MOST's biased in saturation. Vandamme (Fig. 10) [3] shows how deviations from the above-mentioned proportionalities are a proof for unintentional series resistance contributions in submicron devices.

In both models we can scale down the oxide thickness to improve the noise performance. Liu and Huang [47] compared the noise between MOSTs with different oxide thickness and area. They [47] observed $S_{V_{eq}} \propto 1/WL$ as in [8], [4]. The devices with $t_{ox} = 1100$ Å were twice as noisy as the devices with $t_{ox} = 540$ Å. Their results are in agreement with Van der Ziel's [48] limiting $1/f$ noise for a MOST, in which the thermal noise of the frequency-independent dielectric loss

angle $tg\delta$ in the gate oxide results in $4kT\mathrm{Re}[Z]$ which is inversely proportional to the frequency. This $1/f$ spectrum modulates the gate voltage and the current in the MOST.

We investigated different L-arrays which are groups of devices with the channel length L as the only variable. If the series resistance on the drain side plays a role [38], [39], the results obtained on an L-array at fixed saturation current are more difficult to interpret in terms of geometry dependence or type of noise source. What is a correct comparison in, e.g., $S_{V_{eq}}$ for circuit analysis [30] is less useful for the point of view of noise source comparison [17].

Comparing the noise before and after degradation at fixed I_s also has to be avoided for the above-mentioned reason. After degradation, a threshold voltage shift, a mobility reduction and an increase in series resistance is often observed, resulting in a different gate voltage to obtain the same saturation current. If we are interested in the evolution of the noise source through degradation, the $1/f$ noise in the ohmic region should be measured at comparable V_G^* and can be expressed in α-values in order to avoid misunderstandings [13].

The $1/f$ noise is often expressed in pragmatic circuit-simulation-oriented equations without bother about ΔN or $\Delta\mu$. We find for MOST's biased in

1) saturation, for the noise in the saturation current as a function of saturation current

$$S_{I_S} \doteq \frac{K^* I_S}{f} \quad \text{with} \quad K^* = \frac{\alpha_r E_c t_{ox} q\mu}{L^2} = \frac{\alpha V_G^* q\mu}{L^2} \tag{9}$$

or in terms of transconductance we find with $g_m = (W/L)\mu C_{ox} V_G^* = 2I_s/V_G^*$

$$S_{I_S} \doteq \frac{B g_m^2}{WLf} \quad \text{with} \quad B = \frac{\alpha_r E_c t_{ox}^2 q}{2\epsilon_0\epsilon_r} = \frac{\alpha V_G^* q t_{ox}}{2\epsilon_0\epsilon_r} \tag{10}$$

or as equivalent input noise we obtain from (6) and (8)

$$S_{V_{eq}} \doteq \frac{AV_G^*}{C_{ox}WLf} \doteq \frac{B}{WLf} \quad \text{with}$$
$$A \doteq \frac{BC_{ox}}{V_G^*} = \frac{\alpha_r E_c t_{ox} q}{2V_G^*} = \frac{\alpha q}{2}. \tag{11}$$

Here K^*, B, and A are the parameters often used in circuit-simulation-oriented equations.

2) In the ohmic region the following empirical expression is often used to discuss $1/f$ noise and radiation hardness of devices [19]–[29]

$$S_V = \frac{KV^2}{fV_G^{*2}}$$

with

$$K = \frac{\alpha_r E_c t_{ox}^2 q}{\epsilon_0\epsilon_r WL} = \frac{q^2 t_{ox}^2 x_0 D_0 kT(x_0/x_2)}{WL(\epsilon_0\epsilon_r)^2} = \frac{\alpha q V_G^*}{WLC_{ox}}. \tag{12}$$

An overwhelming number of publications, especially for n-channels, showed $\alpha \propto V_G^{*-1}$ or its consequences in the bias dependence of the $1/f$ noise; see for example [19]–[30], [9], [10]. The straightforward interpretation lends support to the ΔN model. The noise results on n-MOST's from 12 different fabricators Chang *et al.* [3] and our results [4] can be summarized with αV_G^* values which are now V_G^* independent and are between 6^*10^{-5} V and 6^*10^{-4} V (α is dimensionless). Invoking an increase in inhomogeneity of current density in the inversion layer at decreasing V_G^* is also possible to explain $\alpha \propto V_G^{*-1}$ in terms of a refined $\Delta\mu$ model.

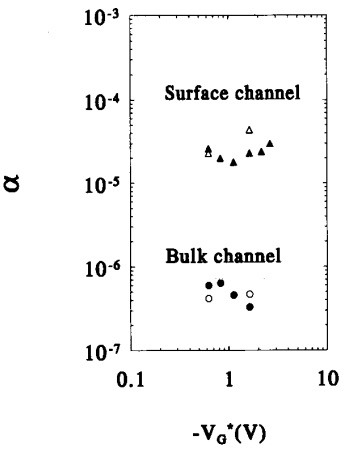

Fig. 2. The $1/f$ noise parameter α versus V_G^* for a surface and bulk p-MOST [33]. The α-values are calculated with (2) from experimental results obtained in the ohmic region: △ surface channel with $L = 5$ μm, ▲ surface channel with $L = 0.8$ μm, ○ bulk channel with $L = 5$ μm, ● bulk channel with $L = 0.8$ μm (*Reprinted from: X. Li, C. Barros, E. P. Vandamme and L. K. J. Vandamme, "Parameter extraction and 1/f noise in a surface and a bulk-type, p-channel LDD MOSFET," Solid-State Electron., vol. 37, pp. 1853–1862, 1994.*).

Klaassen [8] observed for p-MOST's, $S_{V_{eq}} \propto V_G^*$ which means (6) α gate voltage independent. This is in support to the $\Delta\mu$ model. For modern p-MOST's holds α independent of gate voltage with values between 10^{-7} and 10^{-4}.

Fig. 2 shows α-values versus effective gate voltage [33] for p-MOST's with a bulk and surface channel. The devices are enhancement types and have a slightly different threshold voltage ($V_T = -0.6$ V for surface and -0.75 V for bulk). The main difference between the two devices is that: 1) the bulk device has a n^+ polysilicon gate and the surface device a p^+ polysilicon gate. 2) The bulk device has a boron implantation and the surface device a phosphorus implantation of about the same surface concentration in order to keep the difference in V_T rather small. A typical $\Delta\mu$ behavior is shown with a surprisingly low noise ($\alpha \approx 3^*10^{-7}$) for the device with the current path away from the interface. This is in agreement with the results observed in an n-type resistor with gate electrode [40].

A $1/f$ noise model [49] for MOST's in deep saturation based on $\Delta\mu$ and two-dimensional device simulator results showed almost no difference with the ΔN-based results. The results agree with both ΔN and $\Delta\mu$ interpretations.

The proportionality between noise and temperature as predicted by the ΔN model in (8), has been observed for MOST's biased in the ohmic region [50]. However, this is not direct proof of ΔN because the temperature dependence of α in the $\Delta\mu$ model also shows a reduction in α with decreasing temperature as shown by Hooge [3]. The temperature dependence in $S_{V_{eq}}$ or α for p-MOST's is higher than for n-MOST's see Chang *et al.* [3].

III. Hot Carrier Degradation, Proof of ΔN?

The $1/f$ noise has been used as a more powerful tool than dc characteristics to evaluate the quality of a MOST [38] and investigate hot-carrier degradation in devices [11]–[18]. An LDD structure is often used in modern MOST's and the series resistance shows its influence on the dc characteristics, as well as the $1/f$ noise for submicron devices. It was shown that a series resistance with an acceptable value can be the dominant term in the $1/f$ noise behavior of an edgeless MOST [38].

Another study [37] explained how to distinguish the $1/f$ noise from the series resistance and the channel part in a MOST biased in the ohmic region. Especially in a short channel LDD device, not only the value of the series resistance R_s but also its contribution to the $1/f$ noise increases significantly. At saturation the situation becomes worse by a strong increase in the noise of the series resistance on the drain side. An LDD device, as shown in the insert of Fig. 3(a), consists of a conventional MOST in series with two series resistors R_{Dd} on the drain side and R_{sS} on the source side [51]–[54]. Investigations [39], [53]–[56] showed that the series resistance on the drain side behaves differently from that on the source side. The assumption $R_{\mathrm{Dd}} = R_{\mathrm{sS}} = F(V_{\mathrm{GS}})$ is only valid when a MOST is biased in the ohmic region. Above the ohmic region, it was found [53]–[56] that $R_{\mathrm{Dd}} > R_{\mathrm{sS}}$ and R_{Dd} is a function of V_{GS} and V_{DS} (see Figs. 2–5 in [39]), although R_{sS} is still only a function of V_{GS}. When V_{GS} is constant, R_{Dd} increases strongly because V_{DS} increases towards the effective gate voltage V_G^*. Consequently, the internal drain source voltage is clamped, and the channel current is kept constant. This concept is used successfully to explain some experimental results of S_I as a function of V_{DS}/V_G^* [13], [39].

Fig. 3(a) shows R_{sS} versus $1/V_G^*$ for a p-MOST with $L = 0.8$ μm and $W = 10$ μm and in Fig. 3(b) its drain series resistance is shown versus the voltage drop V_{Dd} when the device is biased close to saturation.

Nowadays hot-carrier degradation of submicron MOST's and the evolution of $1/f$ noise are often considered as a direct proof of the number fluctuation origin of the $1/f$ noise. It is thought that the $1/f$ noise increases after hot-carrier stressing due to an increase in the trap density in the oxide layer [11]–[18]. But the consequence of hot-carrier degradation in a MOST is far more complicated.

Among other characteristics; the subthreshold current voltage behavior is often investigated in MOST-degradation experiments. From the slope in the plot of log I versus linear V_G trap densities near mid gap can be derived, this is the so-called subthreshold gradient or subthreshold slope analysis. Generally speaking, the shift of the threshold voltage, the changing slope in the subthreshold region, and the decrease in the channel current are considered as degradation phenomena due to an increase of traps. It was also found after a short time of stressing, that the threshold voltage and the slope in the subthreshold region do not change [57], but that the series resistance increases especially on the drain side. Another degradation phenomenon is the reduction in effective channel length [58], [59], which implies an increase in the series resistance.

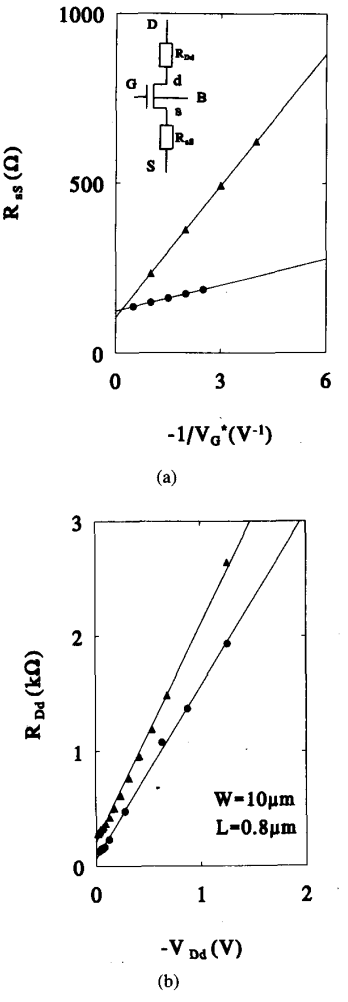

Fig. 3. (a) The source side series resistance R_{sS} versus $1/V_G^*$ for a p-MOST with $W = 10$ μm and $L = 0.8$ μm: ▲ for surface channel, ● for bulk channel p-MOST [33]. (b) The drain side series resistance R_{Dd} versus internal voltage drop V_{Dd} in p-MOST's biased at $V_G^* = -1.63$ V [33]. The triangles ▲ denote a surface channel, and the dots ● are for the bulk channel. The length and width are 0.8 μm and 10 μm, respectively. *(Reprinted from: X. Li, C. Barros, E. P. Vandamme and L. K. J. Vandamme, "Parameter extraction and 1/f noise in a surface and a bulk-type, p-channel LDD MOSFET," Solid-State Electron., vol. 37, pp. 1853–1862, 1994.).*

It was observed that $1/f$ noise level increased a lot in the reverse mode, but hardly changed in the normal mode after hot-carrier stressing when a MOST is biased in saturation [11], [12]. This can be explained without using the ΔN model [13]. Before stressing, a MOST should be symmetric, which means there is no difference between $1/f$ noise levels in the normal mode and in the reverse mode. A post-stressed MOST biased in the ohmic region has nonsymmetric resistance $R_{\mathrm{sS}} < R_{\mathrm{Dd}}$, with about the same dependence on the biasing conditions. Hence, under the same external voltages, the internal biasing conditions and $1/f$ noise remains [11], [12] at low V_G^*. This is independent of the normal or the reverse mode. In saturation, our results [13] showed that the series resistance on the drain side R_{Dd} increases significantly with V_{Dd} (see Fig. 3(b)) and

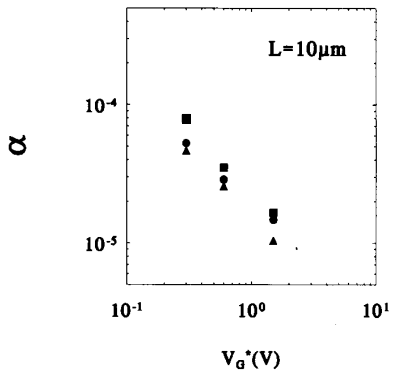

Fig. 4. The $1/f$ noise parameter α versus V_G^* for a long n-MOST ($L = 10$ μm). The symbols used are: ▲ before hot-electron degradation, ● after degradation in normal mode, and $\Delta\mu$ ■ after degradation in reverse mode. Results are taken from [13].

is clamping the current, the voltage drop V_{Dd} across R_{Dd} increases with R_{Dd}.

It has been observed for n-MOST's in a 0.5 μm technology [13], after a stress of only one hour under the bias condition of $V_{\mathrm{GS}} = 2$ V and $V_{\mathrm{DS}} = 5$ V, that hot-carrier degradation causes a decrease in the threshold voltage and the drain current, and a decrease in subthreshold gradient. An increase in the relative current noise and the series resistance R_{Dd} on the drain side has been observed.

The hot-carrier degradation is mainly located close to the stressed drain in a 10 μm length channel and extends more to the whole channel in a 1 μm device. For the same bias conditions, the reduction in the drain current varies for different channel lengths and from normal to reverse mode. It leads to changes by at least factor two more or less in S_I in a pre and post-stressed device depending on channel length. However, when the $1/f$ noise is normalized for frequency, current, and the number of charge carriers, and expressed by the α value, we observe a systematic increase in α by factor two after stressing. The same holds for the relative noise fS_I/I_{DS}^2 for saturation. Both the α value and the relative noise fS_I/I_{DS}^2 in our experiments increase with hot-carrier degradation.

Fig. 4 shows the α-values obtained from the ohmic region versus the effective gate voltage V_G^* for an n-MOST with $L = 10$ μm. The triangles indicate the nonstressed device. The dots and the squares denote the stressed device, biased in normal and reverse mode respectively.

The results are explained as follows [13]. The channel current flows nearer to the interface on the source side than on the drain side. When the damaged part is on the source side, we expect a higher $1/f$ noise. Therefore, a degraded device is often noisier in reverse than in normal mode. The degradation degree is determined by the current density and the electric field. These two quantities differ for devices with different geometry, even for the same bias conditions. Hence, the damaged part decreases with increasing channel length. Thus a short channel device suffers more from hot-carrier degradation than a long channel.

The processes involved in bias stress are complicated and can be summarized as follows for n-MOST's [13]:

1) Depending on the stress conditions, positive and negative shifts in threshold voltage are possible [60]; we found negative shifts in both 10 μm and 1 μm devices,
2) owing to the nonuniform distribution of the trapped oxide and interface charges, the threshold voltage can have a nonuniform value along the channel,
3) the mobility reduction coefficient θ changes (with $\mu = \mu_0/(1 + \theta V_G^*)$, where μ_0 is the low field mobility). There is an increase in series resistance R_{Dd} on the drain side,
4) the position of the depth of the conducting channel on the drain side can shift with aging, so that a noisier or less noisy part of the semiconductor can be probed [40],
5) in the ohmic region, the low field mobility μ_0 decreases 4%, the $1/f$ parameter α increases by about factor two. This makes a $1/f$ noise analysis a more sensitive tool than a mobility or a transconductance measurement. That is at least if the results are presented in α values or in relative current noise as fS_{Is}/I_s^2.

The comparison of $1/f$ noise level, in conventional MOSTs and LDD devices [61] or in devices before and after stressing, should be done under the same internal biasing conditions and not in terms of equivalent input noise voltage. Otherwise the analysis leads to incorrect conclusions. It is clear that, for example, an LDD device can have less noise than the conventional MOST operated under the same terminal voltages because the drain current will be lower due to the series resistances [61].

IV. Correlation Between $1/f$ Noise and Radiation Hardness a ΔN Argument?

A MOS transistor undergoing ionizing irradiation shows a gradual shift in threshold voltage mainly due to an increase in the positive oxide charge. The radiation hardness of a technology is expressed in threshold-voltage shift per Krad (e.g., 3 mV/Krad) and its estimate requires a destructive testing. A strong correlation was observed in n-MOST's between the pre-irradiation $1/f$ noise of MOS transistors and their post-irradiation threshold-voltage shift [19]–[22], [27]–[29], which makes $1/f$ noise a useful nondestructive radiation hardness test. This is not a surprising result, because a $1/f$ noise that is too high is often a good indicator of poor technology or poor crystal quality [41]. (See also Figs. 2 and 3 in [3] by Vandamme.) A poor oxide is easier to degrade than a high-quality oxide and it will result in higher threshold-voltage shifts.

Ionizing radiation not only causes oxide charging, but also an increase in interface-state density. The increase in interface-state density causes a considerable decrease in channel mobility and a decline in g_m [62]. This makes explanations in terms of ΔN or $\Delta\mu$ possible. On the one hand, carriers in a channel which is farther from the interface could experience fewer carrier trappings with defects in the oxide, thereby reducing the $1/f$ noise. On the other hand farther from the interface the α values can be lower due to a better crystal quality [40]. In this way we can understand: 1) the experimental results on $1/f$ noise in n- and p-MOST's through

irradiation and annealing [23], 2) $1/f$ noise prior to and after the bias temperature stress [63].

First, [23] irradiation results in a positive charge at the interface. n-MOST's become noisier because the channel is closer to the interface and p-MOST's show about the same or less noise. After irradiation the noise decreases during positive-bias anneals in n-MOST's but increases during positive-bias for p-MOST's. In the former case the channel is farther away from the interface and in the latter case the channel comes closer to the interface. Conversely, negative bias anneals, increase the noise in n-MOST's but decrease the noise in p-MOST's.

Second, [63] n-MOST's after a positive bias temperature stress show a decrease in noise and after a negative bias temperature stress an increase in noise. For p-MOST's the opposite holds. Under both temperature stress conditions an increase in interface state densities has been observed for n- and p-MOST's [63].

All these results through irradiation and annealing together with the bias temperature treatment do not generally support the proportionality between the equivalent input noise and oxide trap density $S_{V_{eq}} \propto D_0$. The results of annealing after γ-irradiation [23] and bias temperature stress [63] are summarized in Table II. The plus and minus signs in the columns indicated by ΔK, ΔD_i and $\Delta S_{V_{eq}}$ indicate an increase and decrease, respectively. The results can be understood in terms of bulk $1/f$ noise due to mobility fluctuations with decreasing α-values away from the interface [40], [41]. By changing the charge at the SiO_2-Si interface, the position of the conducting path is slightly modified. This can have large consequences on the α-values as can be seen from Fig. 2.

Threshold-voltage shift ΔV_T after γ-irradiation [19]–[30] is attributed to an increase in oxide charge ΔV_{ot} and to a smaller extent to a change in the charge at the Si-SiO_2 interface traps ΔV_{it}, and is given by $\Delta V_T = \Delta V_{ot} + \Delta V_{it}$. The $1/f$ noise observed in the ohmic region is given by (12) where K is proportional to t_{ox}^2. Fleetwood, Meisenheimer, and Scofield [3] show that ΔV_{ot} is also proportional to t_{ox}^2. Then we can expect that $K \propto \Delta V_{ot}$ keeping other parameters constant, which lends support to the ΔN model. All n-MOST's in [19]–[23], [27]–[29] obey $KWL \propto |\Delta V_{ot}|$ although no proportionality has been observed with ΔV_{it}. The latter does not support the ΔN model. Fleetwood *et al.* [20], [3] are presenting experimental support obtained on n-MOST's for the relation between the $1/f$ noise before irradiation and radiation hardness. For the $\Delta\mu$ model we expect $K \propto t_{ox}$ and that increasing K and ΔV_{ot} should go hand in hand but not linearly.

Fig. 5 shows the resistance noise S_R versus V_G^* of a p-MOST through γ-irradiation [28]. No evolution of the $1/f$ noise is observed in this radiation hardened devices at least if the $1/f$ noise is compared at the same effective gate voltage. Although a shift in V_T is observed and radiation damage goes hand in hand with an increase in traps, the $1/f$ noise remains constant. The proportionality $S_R \propto V_G^{*-4}$ points to a proportionality $\alpha \propto V_G^{*-1}$. This is in agreement with the straightforward ΔN model. At higher V_G^* the slope in the S_R versus V_G^* is less steep due to the series resistance contribution [28], [29].

TABLE II
CHANGES IN $1/f$ NOISE AFTER BIAS TREATMENT

	Annealing after γ-irradiation [23]		Bias-temperature treatment [63]		
	gate polarity	ΔK	gate polarity	ΔD_i	ΔS_{Veq}
n-MOST's	+	-	+	+	-
	-	+	-	+	+
p-MOST's	+	+	+	+	+
	-	-	-	+	-

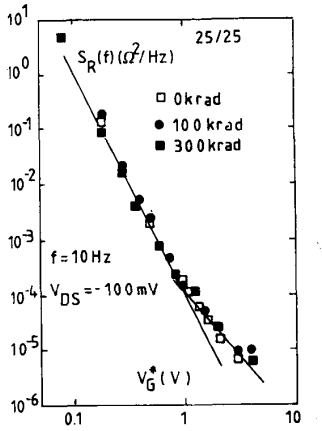

Fig. 5. The resistance fluctuations S_R versus V_G^* of a large p-MOST put through irradiation. (*Reprinted from: A. Hoffmann, M. Valenza, D. Rigaud, and L. K. J. Vandamme, "Radiation effects on radiation hardened LDD CMOS transistors," Noise in Physical Systems and $1/f$ Fluctuations, St. Louis, MO 1993, P. H. Handel and A. L. Chung, Eds.AIP Conference Proceedings 285, AIP Press, New York, 1993, p. 362.*)

The effective gate voltage should be kept constant at a low enough V_G^* in order to compare the $1/f$ noise through irradiation [27], [28]. N-channel devices are sensitive for leakage resistance through irradiation [29]. A dramatic increase in noise says nothing about a ΔN or $\Delta\mu$ origin [17], [18], rather it says more about the creation of a noisy leakage-current path. This path is situated in parallel to the channel close to the so-called bird beaks at the gate oxide rims. The creation of a noisy leakage current path is observed from the change in subthreshold characteristic and noise after degradation. The edge current problems have been investigated from a set of MOST's all having the same length but different width and from the comparison between edgeless and open structures.

The experimentally observed $1/f$ noise in n-MOST's is often in agreement with the ΔN model and oxide trap density D_0, see Chang *et al.*, Fleetwood *et al.* [3], and in [8]–[10] and [64]. However, from the results in Table II where increase in interface state density after bias temperature treatment not always goes hand in hand with an increase in $1/f$ noise as should be expected from (8) in the ΔN-model, we see problems for interpretation. In Fig. 2 and from Chang *et al.* [3] we see gate voltage independent α-values for bulk or surface channel p-MOSTs which is in disagreement with the straightforward ΔN interpretation. From Table II and Fig. 2 [23], [63], we conclude that the extraction of oxide trap density

or even its energy distribution based on noise measurements as proposed in [65]–[68] are very doubtful.

V. Conclusion

Geometry dependence is well understood with the exception of the t_{ox} dependence. The width, length and V_G^* dependence can be used as a diagnostic tool to trace series resistance and edge current contributions in submicron devices. In short LDD MOST's deviations from the simple bias dependence are observed especially close to saturation due to a strong increase in the series resistance on the drain side [13], [37]–[39], [61].

The $1/f$ noise parameter α is a perfect figure of merit to describe the $1/f$ noise in a MOST as was done by Chang *et al.* in a comparative study of CMOS transistors [3]. In this way we can compare different technologies and study the change in noise source through degradation independent of geometry, frequency and current passed through the sample.

Both schools of thought have their favorite devices: n-MOST's for the ΔN school and p-MOST's for the $\Delta\mu$ school. Bias dependence of the $1/f$ noise parameter α points to a straightforward interpretation in terms of ΔN if $\alpha \propto V_G^{*-1}$, but $\Delta\mu$ is also possible [39], [40]. The gate voltage independent α value often seen in p-MOST's is easy to interpret in terms of $\Delta\mu$. We observed $\alpha \approx 4{*}10^{-7}$ which is among the lowest values ever observed for bulk p-MOST's, while for n-MOST's holds $6{*}10^{-5}$ V $< \alpha V_G^* < 6{*}10^{-4}$ V, with $\alpha \propto V_G^{*-1}$. In general n-MOST's are noisier than p-MOST's and easier to interpret in the straightforward ΔN formalism, while for low-noise p-MOST's the straightforward $\Delta\mu$ formalism holds.

Due to series resistance complications and charging of the gate oxide in hot-carrier degraded MOSTs, the interpretation in terms of ΔN is not the only one. If the charging of the interface results in a channel which is farther from the interface the result is often a reduction in the $1/f$ noise [13]. This holds for n- and p-MOST's independently if the charging was provoked by γ-irradiation, hot-carrier stressing, annealing under bias treatment after irradiation or simple bias temperature stress (Table II).

$K \propto |\Delta V_{ot}|$ is in agreement with ΔN and $\Delta\mu$. This makes the $1/f$ noise in n-MOST's before irradiation a useful non destructive tool to characterize radiation hardness.

The irradiation-independent behavior of the $1/f$ noise up to 300 Krad, although there is a shift in threshold voltage, is more difficult to understand in terms of ΔN.

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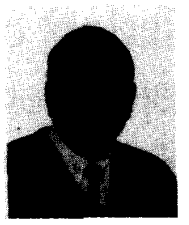

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