1-GHz Bandwidth Digital Spectro-Correlator System for the Nobeyama Millimeter Array

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Abstract

We have developed 1-GHz bandwidth digital spectro-correlator system for the Nobeyama Millimeter Array (NMA). It consists of 2Gsample/sec·2bit analog-to-digital (A/D) converters and an ultra-wide band digital correlator. We developed two kinds of special-purpose LSI having functions of delay compensation and correlation, respectively. With these LSIs, the ultra-wide band digital correlator realizes 1024-MHz bandwidth spectroscopy with 128-channel resolution for 15-correlation data. This system allows us to observe radio continuum emission with about a two-times better signal-to-noise ratio than that of the previous correlator system. We started common-use observations with this new system from 1997 March; the system has been extended in order to obtain 21-correlation data for a 7-element "Rainbow" (NMA + 45-m telescope) interferometer system.

Key words: instrumentation: interferometers — radio continuum: general — radio lines: general — techniques: signal processing — techniques: spectroscopic

1. Introduction

In the last decade, aperture synthesis observations with millimeter-wave arrays have revealed many important facts about diverse astronomical objects, e.g., circumstellar disks associated with young stellar objects, gaseous envelopes around evolved stars, and molecular clouds in nearby and high-z galaxies (see Sargent, Welch 1993 for a review). In order to obtain more fruitful results from these arrays, their instrumental performance should be improved further. A receiver system with a wider bandwidth ($\gtrsim 1$ GHz) is one of the desirable features for these millimeter arrays. It would enable us to make more sensitive continuum observations, because the signal-to-noise ratio for continuum emission is proportional to the square root of the total bandwidth. Some galaxies show molecular line emission with its total velocity width greater than 700 km s⁻¹, or 300 MHz in frequency width at 115 GHz; hence, an observing bandwidth wider than 500 MHz is needed to explore all of the emission components from such galaxies simultaneously. A wideband receiver system also makes it possible to detect a visibility calibrator with a higher signal-to-noise ratio, resulting in an improvement of the quality of the obtained synthesis images.

The development of a new spectro-correlator is an essential task for expanding the receiving bandwidth of a millimeter array, because the available bandwidth is usu-

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Table 1. Comparison of the specification of the old and new NMA correlator systems.

Correlator	Nobeyama FX	UWBC
Bandwidth (MHz) Spectral channels	320, 160, 80 1024	1024, 512*, 256* 128, 256*
Velocity coverage at 115 GHz (km s ⁻¹)	832, 416, 208	2662, 1331, 666
Velocity resolution at 115 GHz (km s ⁻¹)	0.8, 0.4, 0.2	20.8, 5.2, 2.6

*In case of 512 and 256 MHz bandwidth, the number of spectral resolving points is 256.



Fig. 1. Basic structure of the 1-GHz bandwidth digital spectro-correlator system.

ally limited by the signal-processing speed of the correlator. In the case of the Nobeyama Millimeter Array (NMA), which was completely constructed in 1983, an FX-type digital spectro-correlator, called Nobeyama FX, made a fast Fourier transformation (FFT) of the signal before a cross-correlation, was originally employed (Chikada et al. 1987). However, its total bandwidth of 320 MHz was too narrow to satisfy the increasing scientific demands in the mid 1990's, leading us to construct a new correlator with a wider bandwidth, called "Ultra-Wide Band Correlator" (hereafter UWBC). The design and development of UWBC as well as a high-speed analog-to-digital (A/D) converter for it were started in 1991, and the installation of the whole correlator system was completed in 1997 February. It has been dedicated to common-use observations of NMA since 1997 March.

Table 1 gives the comparison of the specifications of two correlators, Nobeyama FX (Chikada et al. 1987) and UWBC. The specifications of UWBC were optimized for the observations of continuum emission, and those of molecular lines from extra-galactic objects; the total bandwidth is as wide as possible with the present technology, while the number of frequency channels is relatively small. The best scheme to realize a spectrocorrelator with these specifications is the so-called "XF", in which a cross-correlation of signals from two antennas is performed first, and then the cross-power spectra are calculated through the FFT. In this scheme, the part calculating the cross-correlation can be easily integrated into a small chip of LSI (large-scale integrated circuit), permitting us to make the size of the correlator fairly small. In addition, XF-type correlator is more cost-effective than the FX-type when the total number of the frequency-channels is less than a few hundred (see Chikada et al. 1983). We therefore designed UWBC as an XF-type spctro-correlator. We have also developed a new FX-type correlator for the observations with higher velocity resolution. This FX-correlator and UWBC can operate simultaneously in the present observing system.

In this paper we describe the implementation and performance of the new digital spectro-correlator system in detail. The system architecture and hardware design are described in section 2, and the performance and recent results are shown in section 3.

2. Architecture and Hardware Design

2.1. Overview

Figure 1 shows the basic structure of the new digital spectro-correlator system. The system consists of 2Gsample/sec·2bit A/D converters and the digital spectro-correlator UWBC. Each A/D converter makes four-level (2-bit) quantization with a sampling rate of

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2048 MHz, and outputs 128-bit (2 bit \times 64) parallel data with a 32-MHz clock cycle. Parallel signal processing is the most important architecture in the digital spectrocorrelator system, making it possible to calculate the cross-correlation with a much slower clock speed than that of the Nyquist rate of the input IF signal, whose maximum bandwidth is 1024 MHz.

In the digital spectro-correlator UWBC, the geometric delay for each baseline is compensated before calculating the cross-correlation. In calculating the cross-correlation coefficient for 2-bit signals, a simple "bit-match" method, introduced by Kawaguchi (1983), is adopted. In this method, a set of 1-bit correlations, $H_x \times H_y$, $H_x \times L_y$, and $L_x \times H_y$ are calculated first, where $H_{x,y}$ and $L_{x,y}$ represent the most-significant bit (MSB) and the leastsignificant bit (LSB) of the 2-bit signals from antennas xand y, respectively. Next the cross-correlation coefficient, $\rho_q(\tau)$, is derived by the following equation:

$$\rho_{\mathbf{q}}(\tau) = 2\langle H_x(t)H_y(t+\tau)\rangle + \langle H_x(t)L_y(t+\tau)\rangle + \langle L_x(t)H_y(t+\tau)\rangle, \qquad (1)$$

where τ indicates the amount of delay and the brackets, $\langle \rangle$, denote time average. In this equation, low-level products are ignored and the weight for MSB is set to be 2 (Cooper 1970). The signal-to-noise ratio relative to that for the unquantized Nyquist-sampled signal takes the maximum value of around 0.85 when the quantization thresholds are $\pm 0.93 \sigma$ and 0, which can be derived in the same way as that described by Hagen and Farley (1973) and Bowers and Klinger (1974). One can estimate the cross-correlation coefficient for the unquatized signals, $\rho(\tau)$ from $\rho_q(\tau)$, using the relationship between $\rho(\tau)$ and $\rho_q(\tau)$, which is usually called as the Van Vleck relationship (Van Vleck, Middleton 1966). UWBC makes the Van Vleck correction before FFT to obtain the crosspower spectra.

We integrated a certain number of digital-delay circuits into a special-purpose LSI chip, named "UWBC1", for compensating the geometric delay in the correlator UWBC. The above method for the cross-correlation calculation is fairly simple, but at the same time a large number of digital circuits are needed for implementation if the technique of parallel signal processing is adopted. This led us to develop another special-purpose LSI chip, named "UWBC2", for correlation calculations of 1-bit signals. We describe these two LSIs in detail in a later section. On the other hand, the Van Vleck correction as well as calculations of FFT, and the correction for residual delay can be made at a much slower processing speed compared with that for calculating the cross-correlation, because these calculations are made using time-averaged cross-correlation coefficients. Therefore, these calculations are performed with a general-purpose DSP chip after calculating the cross-correlation.

2.2. High-Speed 2Gsample/sec-2bit A/D Converter

In the high-speed A/D converter for UWBC we used a high-speed sampling LSI that could convert analog signal into 2-bit digital signals with a clock rate of 2048 or 4096 MHz. It was originally developed to make "burst-mode" VLBI experiments (Kawaguchi 1991) available. With this sampling LSI, Matsumoto, Kawaguchi, and Horiuchi (1995) made a high-speed 4-GHz sample/sec·2bit A/D conerter system for the "burstmode" experiments. We used their design as a prototype for the high-speed A/D converter. The sampling rate of is set to be 2048 MHz with 2-bit(4 level) quantization.

Figure 2 shows a block diagram of the A/D converter. This A/D converter consists of three parts: a sampling LSI unit, a fast demultiplexer (DMUX) unit, and a slow demultiplexer (DMUX) unit. The sampling LSI in the sampling LSI unit converts an 1024–2048 MHz analog signal into 2-bit digital signals at 2048 MHz cycle and proceeds 1:4 demultiplex of the digital signals. Thus, the sampling LSI unit outputs 4-parallel 2-bit data with a clock cycle of 512 MHz. Because both the fast and slow DMUX units have a function of 1:4 demultiplex, the output ECL signals from the A/D converter are in the form of 64-parallel 2-bit with a clock cycle of 32 MHz. In these DMUX units, we used GaAs DMUX LSIs in which 4 sets of a 1:4 demultiplexer are integrated in one package, making it possible to reduce the number of ICs in these units. The fast DMUX unit is operated with 512 MHz clock, provided by the sampling LSI unit; the slow DMUX unit is operated with 128 MHz clock, provided by the fast DMUX unit. This three-part structure allows us to make trouble-shooting and maintenance easier.

The photograph inside the A/D converter is shown in figure 3. The large board at the right is the fast DMUX unit, and a small daughter card surrounded by an aluminun frame on this board is the sampling LSI unit. A sampling LSI is located under the small fan, and the daughter card is isolated, and can be easily separated from the fast DMUX board. They are connected with each other by only coaxial cables. All four boards on the left belong to the slow DMUX unit; the most left-hand one is used to monitor the phase difference among the 32 MHz data clocks in the slow DMUX boards. One can easily adjust the phase difference among these clocks by supplying an external reset signal to the A/D converter. The high-speed A/D converters are manufactured by Nihon Tsushinki Co., Ltd.

We made a performance check of the A/D converter using a device named "A/D converter monitor", which is the D/A converter system to transform 64-parallel 2-bit ECL signals to an analog signal. We had input analog sine waves to the A/D converter, put the output digital signals into the A/D converter monitor, and checked out the waveforms of the output analog signal using an oscil-





Fig. 2. Block diagram of the 2Gsample/sec-2bit UWBC A/D converter. An analog signal of 1024-2048 MHz is put into the A/D converter, and the sampling rate is 2048 MHz with 2-bit sampling. After sampling, the data are demultiplexed three times with 1:4 and the output is 64 parallel ECL data with a 32 MHz clock cycle. It has a phase-lock system of the sampling clock to synchronize the sampling timing among all A/D converters.



Fig. 3. Photograph of the A/D converter boards.

loscope. We also measured the phase differences of the eight 32-MHz data clocks in the slow DMUX boards for a few days to confirm the stability of the timing of the output parallel data.

2.3. Ultra-Wide Band Correlator

2.3.1. Delay compensation and correlation LSIs

We have newly developed two kinds of special-purpose LSI, UWBC1, and UWBC2. UWBC1 has a function to compensate the geometrical delay at a 2048 MHz sampling cycle. The resolution of the delay compensation is 0.146 m and the total delay length is about 590 m per chip. 64-parallel data from the A/D converter are put into the data memory (FIFO) of UWBC1 at a 32 MHz clock cycle, and the 64-parallel data are read out from the memory with timing according to the delay length.

UWBC2 calculates the 32-lag 1-bit correlation at 32 MHz clock for 64 parallel input data. Figure 4 shows a block diagram of the calculation of a 32-lag 1-bit correlation in a UWBC 2 chip. 32-parallel data from antenna X are put into 32 buffers, and are multiplied by 32 sets of 32-parallel data from antenna Y to calculate the correlations with 32 different lag numbers. The pipeline delay of this part is 22 clock cycles. After the pipeline delay time, UWBC2 calculates the 32-lag 1-bit correlation at each clock cycle. The UWBC 2 chip also has a fringe-rotation function; its minimum angular setting unit is 22.°5, and the maximum rotation rate is 10 Hz. The correlated data are integrated up to 0.1–1.0 s with an accuracy of 24 bits.

These two LSIs are designed for both a connected array

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Fig. 4. Block diagram of the 32-lag 1-bit correlation part of UWBC2. 32-parallel data from antenna X are put into 32 buffers, and are multiplied by 32 sets of 32-parallel data from antenna Y to calculate correlations with 32 different lag numbers. X_i and Y_i are the *i*-th data from antennas X and Y, respectively. Σ_i means summing up the data from i = 1 to 32.

and VLBI observations. We are able to expand the tracking delay length and the lag numbers by connecting these LSIs serially. Each of these chips is an 120 K-gate CMOS gate array. The package is a ceramic 401-pin PGA with a fin. The maximum and average power consumption are about 5 and 2.5 Watt at 32 MHz clock cycle. These LSIs are manufactured by Tokyo Electron Ltd.

2.3.2. Correlator UWBC

Using these UWBC chips, we have developed an XFtype ultra-wideband correlator UWBC. Figure 5 shows a block diagram of UWBC for one baseline. It consists of four parts: an A/D interface unit, a correlation unit, a DSP unit, and a host interface unit. 64-parallel data from each A/D converter are put into the A/D interface unit. The data signals are converted from ECL to TTL in this unit, and are put out to the correlation unit with 1:7 fanout. Two sets of parallel data are sent to the correlation unit for one baseline. In the correlation unit a compensation of the delay is made with two serially connected UWBC1 chips before the correlation calculations; the tunable range of the delay is between ± 1170 m. The 256lag 2-bit correlation function is calculated by the method described in subsection 2.1 [see equation (1)]. The three "bit-mach" calculations in equation (1) ($\langle H_x H_y \rangle$, $\langle H_x L_y \rangle$, $\langle L_x H_y \rangle$) are performed with three sets of serially connected UWBC2 chips in the correlation unit, and the assembling of these results and the Van Vleck correction are made in the following DSP unit to obtain the 2-bit cross-correlation coefficients. In the UWBC2 chips, demodulation of $90^{\circ}/180^{\circ}$ phase switching is also made by the function of fringe rotation in these chips. In the DSP unit, 256-point FFT, the correction for residual delays (" ΔW "), and fringe-stopping operation are made to obtain the cross-power spectra with 128 frequency channels. Three weighting functions are available in the spectral estimation, uniform, Hanning, and Blackman (e.g., table 8.3 in Thompson et al. 1986). The cross-power spectra can be integrated up to 60 s in the DSP unit. After that, the spectral data from 21 baselines are sent to the host workstation through the host interface unit.

The correlation unit for one baseline consists of three sets of one delay control board and two correlation boards. Five UWBC1 chips are installed on a delay control board, and eight UWBC2 chips are installed on the correlation board shown in figure 6. UWBC calculates at most 21 sets of 1024 MHz-bandwidth cross-power spectra with 128 frequency channels. In the case of the 512



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Fig. 5. Block diagram of UWBC (one baseline). H and L represent the most-significant bit (MSB) and the least-significant bit (LSB) of the 2-bit signal, respectively. Fifteen UWBC1 chips and forty eight UWBC2 chips are installed in the correlation unit of one baseline. The hached box is the switch to connect the upper series of UWBC2 chips and the lower one in the case of 512- and 256-MHz bandwidths.



Fig. 6. Photographs of UWBC boards. The left panel is a delay control board, and the right one is a correlation board.

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Fig. 7. Relationship between the input noise power and the noise-to-signal ratio of the correlator system. The X-axis shows the input total power of the correlated noise, and the Y-axis shows the standard deviation of the 128-channel corss-power spectra in the 1024-MHz bandwidth mode.

or 256 MHz-bandwidth mode, the lag number can be expanded along with a decrease of the input data rate (see figure 5). 256-channel spectra are available with the 512 and 256 MHz bandwidths. UWBC also has a function to generate test-pattern data in the A/D interface unit, and calculates the 2-bit auto-correlation function in the correlation unit. These functions enable us to make trouble shooting easier. The correlator UWBC is manufactured by Oki Electric Industry Co., Ltd.

System Performance 3.

No. 2]

We checked the noise-to-signal ratio (NSR) of the digital spectro-correlator system in the 1024-MHz bandwidth mode using correlated noise as the input signal; the standard deviation of the cross-power spectra was measured as a function of the input noise power. The threshold levels of the sampling LSI in the A/D converters were set to be 0V and ± 250 mV. The minimum NSR in the "bit-match" method is expected to be around 0.15 when the quantization thresholds are 0 and $\pm 0.93 \sigma$ (see subsection 2.1), which corresponds to an input noise power of -1.4 dB m. Figure 7 shows the relationship between the power of the input noise and the resultant NSR of the system. In the case of an input power of -1.8 dB m, NSR was measured to be 0.17, corresponding to a quantization efficiency of 0.83. This value agrees with the expected quantization efficiency for the optimum case (0.85) within the accuracy of the measurements.

The noise floor was also measured using uncorrelated receiver noise under the 180° switching. Figure 8a shows the typical noise spectra of cross-correlation and fig-



Fig. 8. (a) Typical noise spectra of the cross-correlation with a 1024-MHz bandwaidth. The upper panel shows the amplitude spectrum, and the lower one shows the phase spectrum. (b) the r.m.s. of 128channel spectral data with 1024-MHz bandwidth as a function of the total integration time.

ure 8b is the r.m.s. of 128-channel spectral data with a 1024-MHz bandwidth as a function of the total integration time. The noise floor decreases with a dependence of time.^{0.5} In some auto-correlation spectra, there were small spurious features at the central channel of 400

Relative amplitude

0.

S. K. Okumura et al. Frequency [MHz] 86755.442 86243.442 85731.442 (a) LSB SiO mase (2-1, v=2) SO₂ (8(3,5)-9(2,8)) SO (2(2)-1(1)) HC15N H13CN (1-0) (1-0) 180 90 4. phase 0 90 180 16 32 48 64 Chan 80 96 112 128 Frequency [MHz] 98243.442 98755.442 CS (2-1)



Fig. 9. 1024-MHz bandwidth DSB spectra of Orion-KL region. The upper panel is the LSB amplitude and phase spectra centered on the SiO maser at 86.243442 GHz, and the lower one is the USB amplitude and phase spectra centered on 98.243442 GHz.

1024 MHz bandwidth. These features were probably due to contamination by the 512 MHz data clock from the sampling LSIs in the A/D converters. However, most of these features were removed from the cross-power spectra under 180° switching, because the power of the spurious feature did not change during one cycle of the 180° switching.

In our system, $90^{\circ}/180^{\circ}$ phase-switching modulation is performed at the first local oscillator, while the demodulation is proceeded in the UWBC2 chips. The 90° phaseswitching technique with mixer-type receivers enables us to obtain spectra for both the upper sideband (USB) and the lower sideband (LSB) simultaneously. We have estimated the 180° switching accuracy to be < 40 dB at a switching cycle of 0.1 s from measurements of the correlated noise through the IF transmission lines as the input signals. On the other hand, an accuracy of 90° phase switching (image-band rejection ratio) has been estimated from observations of the Orion-KL SiO maser spectra at 86 GHz. Figure 9 shows the double-sideband (DSB) spectra. Although SiO maser emission was detected in the central channel of LSB, there was no line emission at the corresponding central channel of USB, indicating that the image-band rejection ratio is better than 20 dB at a switching cycle of 0.8 s.

Summary

We have completed the development of a 1-GHz bandwidth digital spectro-correlator system for the Nobeyama Millimeter Array. This system allows us to obtain crosspower spectra from 21 baselines in the DSB mode; the maximum bandwidth is 1024 MHz for each sideband, and the fastest output cycle is every 0.1 s. The input data rate is $2048 \times 10^6 \times 2 \times 7$ bit s⁻¹, and the corresponding processing speed is about 5.5×10^{12} operation s⁻¹. The maximum output data rate is 430 kB s⁻¹. This correlator system calculates the widest continuous spectra among the spectro-correlators for radio astronomy all over the world.

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