10-Gb/s All-Optical Half-Adder With Interferometric SOA Gates

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Abstract—In this letter, we report an all-optical module that generates simultaneously four Boolean operations at 10 Gb/s. The circuit employs two cascaded ultrafast nonlinear interferometers and requires only two signals as inputs. The first gate is configured as a 2×2 exchange-bypass switch and provides OR and AND logical operations. The second gate generates XOR (SUM bit) and AND (CARRY bit) Boolean operations and constitutes a binary half-adder. Successful operation of the system is demonstrated with 10-Gb/s return-to-zero pseudorandom data patterns.

Index Terms—Half-adder, high-speed optical logic, optical gate, optical signal processing, ultrafast nonlinear interferometer (UNI).

I. INTRODUCTION

ALL-OPTICAL signal processing concepts and technologies have evolved significantly in the past few years, primarily due to the development of advanced semiconductor-based all-optical switching devices [1] and their commercialization. Exploiting the maturation of these devices, Boolean logical operations have been previously shown in single-gate experiments [2], [3]. However, as research in all-optical signal processing continues, improvements and innovation will relate more and more to better circuit design and less to improvements in the "optical transistor" itself, in a way very similar to the research evolution of electronic very large scale integration. So far, all-optical digital processing circuits using multiple gates, capable of performing more complex logic operations as in a full-adder, counter, or parity checker, have been reported in [4]–[6]. All of these modules employ a half-adder unit as the basic functional block. However, optimization of optical circuit designs in terms of power efficiency, number of gates, and required input signals that will allow scalability and operational speed enhancement, still remains an issue.

The initial realization of the all-optical half-adder was implemented using three optical gates and was shown to operate at 1 Gb/s [5]. This circuit required data signals of different wavelength, while the SUM signal consisted of two distinct wavelengths. Hence, strictly speaking, the logical operation was not obtained in the optical domain since it required electronic square-law detection. More recently, a dual-rail implementation of the half-adder was made using two semiconductor optical
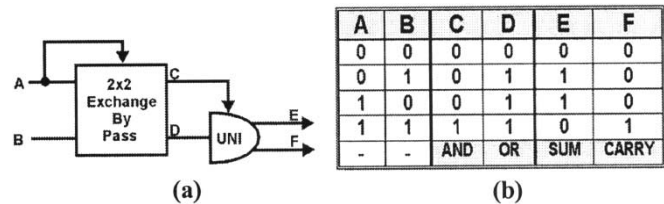
Fig. 1. (a) Concept block diagram and (b) device truth table.

A	B	C	D	E	F
0	0	0	0	0	0
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	1
-	-	AND	OR	SUM	CARRY

amplifiers (SOAs) operated nonlinearly with gain saturation and a Mach–Zehnder interferometric switch [6]. Optical circuit design based on single-rail interferometric switches is expected to be preferable due to the inherent operational speed and relative resilience to data pattern effects that may be attained by cross-phase modulation [7], [8]. In contrast, the operational speed of dual-rail optical logic devices is limited due to the SOA saturation properties.

In the present communication, we demonstrate for the first time a simple single-rail optical module that performs a total of four Boolean logic operations including that of a half-adder and operates at 10 Gb/s. This unit uses two cascaded ultrafast nonlinear interferometers (UNIs) and requires only two data signals as inputs to operate. The first gate is configured as a 2×2 exchange–bypass switch [9] and carries out simultaneous AND and OR logical operations, while the second UNI outputs logical XOR (SUM bit) and logical AND (CARRY bit) of the original data streams hosting as the binary half-adder. The design reported outperforms previous results in terms of number of active elements and switching energies required, whereas, no additional control signals are necessary to perform AND–OR–XOR operations. The innovation of this half-adder lies in its optimal circuit design concept and may be used as the basic building unit for future large scale optical circuits.

II. CONCEPT AND EXPERIMENTAL SETUP

Fig. 1 shows the concept upon which the half-adder circuit design was based along with the associated truth table. This configuration uses a 2×2 UNI-based exchange–bypass switch followed by a UNI gate. The exchange–bypass switch is operated with two inputs and one control signal. In the absence of a control pulse, the switch operates in the bar state and the inputs (A, B) pass over to the corresponding output ports (C, D). Whenever a control pulse is present, the switch operates in the cross state and the inputs (A, B) appear switched over at the output ports (D, C).

If, however, the control signal is identical to one of the input signals (e.g. the A signal), the exchange-bypass switch provides
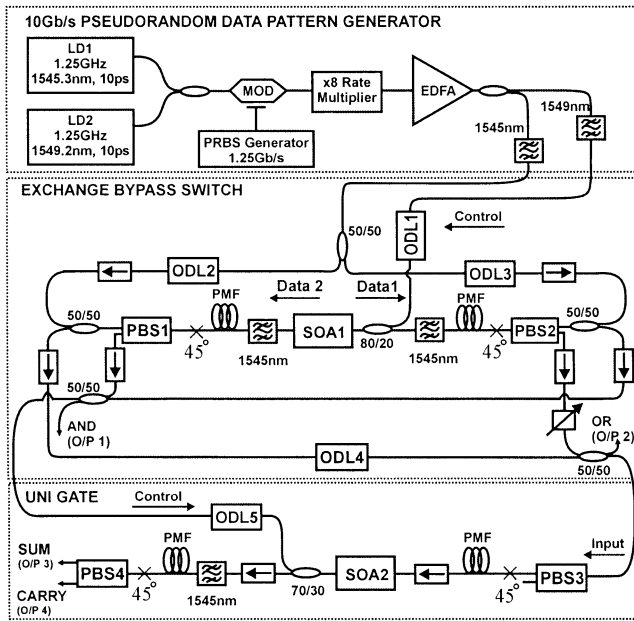
Fig. 2. Layout of the experimental setup distinguishing the three major parts of the circuit (data generator, exchange-bypass switch, UNI gate).

the logical operations AND and OR between Inputs A and B, at Ports C and D, respectively, as illustrated in the truth table of Fig. 1. By inserting the AND pattern as the control signal and the OR as the input signal, to a cascaded UNI gate, logical XOR and logical AND of the initial Inputs A and B is obtained at the output Ports E and F of the second gate, respectively. As a result, this configuration constitutes a half-adder module, where logical XOR stands for the SUM bit and logical AND stands for the CARRY bit.

The experimental setup is comprised of three discrete subsystems, as shown in Fig. 2: a 10-Gb/s test data generator, an exchange–bypass switch, and a UNI gate. Two distributed feedback laser diodes, LD1 (1545.3 nm) and LD2 (1549.2 nm), were gain switched at 1.25 GHz to provide 10-ps optical pulses after linear compression and were used to generate Data 1, Data 2, and the control signal which is a replica signal of Data 1. These pulse trains were combined into a single fiber and modulated with a $2^7 - 1$ pseudorandom binary sequence pattern in a Ti : LiNbO$_3$ electrooptic modulator. The modulated data were passively eight times rate multiplied in a three-stage bit interleaver, in order to produce pseudorandom data patterns at 10 Gb/s. Finally, Data1–Data2 and the control signal were separated with a 3-dB fiber coupler and appropriate filtering and were inserted into the exchange–bypass switch.

The exchange–bypass switch is a specially configured UNI gate with two inputs. Data 1 and 2 entered the switch via polarization beam splitters PBS2 and PBS1, respectively, so as to counterpropagate in SOA1. Each of these signals was analyzed into two orthogonal polarization components in a 45° splice between the output fibers of the PBS and a following piece of polarization maintaining fiber (PMF), used to birefrigently delay these two components. After traveling through the PMF, a relative delay of 50 ps was induced between the two polarization components before entering SOA1. After exiting the semiconductor, the two polarization components of Data 1

and 2, had their relative delay removed in the second piece of PMF and were forced to recombine on their respective output PBS. The nonlinear switching element used was a 1.5-mm bulk InGAsP–InP ridge waveguide SOA, SOA1 (Optospeed S.A.) exhibiting 27 dB small-signal gain at 1550 nm and 24 dB at 1545 nm with 80-ps recovery time, when driven with 700-mA current. Optical filters centered at 1545 nm were included adjacent to SOA1 to reject amplified spontaneous emission noise and the control signal.

The control signal was inserted into SOA1 via a 80 : 20 fiber coupler so as to copropagate with Data 1 and to be synchronized with one of the orthogonal polarization components of each data pulse. The switch was biased so that in the absence of control signal pulses, Data 1 exited through the bottom port of PBS 1 (as drawn in Fig. 2) and finally through output 1 (O/P 1), while Data 2 exited through the bottom port of PBS 2, and finally through output 2 (O/P 2). In the presence of a synchronized control pulse with one of the polarization components from Data 1 and 2, the phase of these components is changed through cross-phase modulation in the SOA, so that when the respective polarization components are recombined in the output PBSs, their polarization state rotates by 90°. Consequently, pulses from Data 1 exited through the top port of PBS 1 and finally through O/P 2, while pulses from Data 2 exited trough the top port of PBS 2 and, in turn, through O/P 1. Provided that the control signal is identical to Data 1, the exchange–bypass yields the logical AND at O/P 2, and the logical OR at O/P 1, the former of which consisting of switched pulses from Data 2, while the latter consists of both Data 1 switched pulses and Data 2 unswitched pulses. Synchronization of the three signals in SOA1 was achieved by using optical delay lines ODL1, ODL2, and ODL3, whereas, ODL4 served to combine appropriately the bits from Data 1 and 2 at the OR logical output.

The third and final stage of the system was a UNI gate in its simple configuration with one input and one control signal. The OR output pattern of the exchange–bypass switch was fed as the input signal, while the AND output pattern was inserted as the control signal in a counterpropagating fashion. The gate was biased in a way that in the absence of a control pulse, the input signal exited through O/P 3 (unswitched port), yielding the XOR logical operation (SUM bit) between Data 1 and 2 signals, while in the presence of a control pulse, the input signal exited through O/P 4 (switched port), providing the AND logical operation (CARRY bit) between Data 1 and 2. The semiconductor used in this gate as the nonlinear element (SOA2) was an identical device to that used in the exchange-bypass switch. Bit synchronization in SOA2 was achieved using ODL5.

III. RESULTS

Various data patterns were used to test the performance of the half-adder at 10-Gb/s nominal rate. Fig. 3 illustrates a typical example of the performance of the system showing the evolution of the signal through each individual section. In detail, Fig. 3(a) shows a set of typical input traces, including Data 1, Data 2, and the control signal, which is identical to Data 1, entering the exchange-bypass switch. Fig. 3(b) illustrates the corresponding logical AND and OR operations as they appear at the output ports
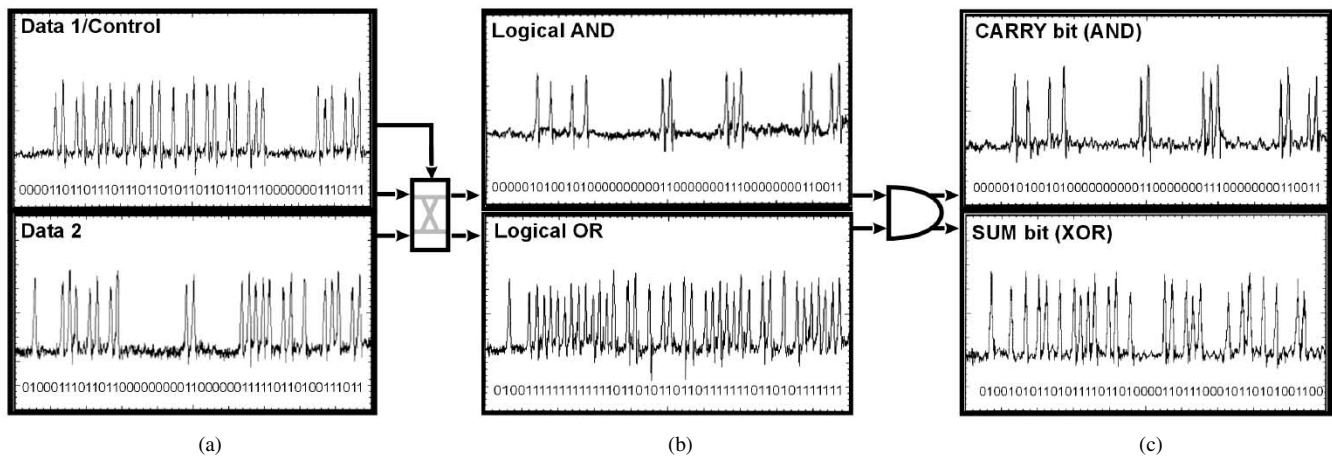
Fig. 3. Oscilloscope traces obtained through the system representing (a) input signals to exchange-bypass switch, i.e., Data 1 and control, which are identical and Data 2, (b) logical AND and logical OR operations at the output of the switch, and (c) the CARRY and the SUM bit at the output of the UNI gate. The timebase for all the traces is 500 ps/div.

of the exchange-bypass switch. The crosstalk of the 2×2 switch was approximately -12 and -10 dB for the bar and cross states, respectively. The illustrated AND pattern enters the second UNI gate as the control signal and the OR pattern as the input signal. Fig. 3(c) depicts the outputs of the second gate as they appear at its unswitched and switched ports. Bit-by-bit checking reveals successful XOR and AND logical operations between Data 1 and 2, providing the SUM and CARRY bit, respectively, of a half-adder module. The extinction ratio between the ON–OFF states of the gate was approximately 8 dB and this was due to incomplete signal switching in the gate.

The pulse energies required for switching were 4, 3, and 9 fJ for Data 1, Data 2, and control signals, respectively, in the exchange–bypass switch, whereas, in the second gate the pulse energies were 8 fJ for the control and 2 fJ for the input signal. The small pulse amplitude modulation being present in the generated traces shown in Fig. 3 is primarily due to imperfect rate multiplication and can be avoided with a 10-Gb/s data transmitter. The half-adder module operated successfully for various different input patterns revealing no pattern dependence. Finally, it is important to note that the system requires only the two data signals as inputs (control signal being identical to Data 1) and exhibits very low switching energies, suggesting that it may be deployed without optical preamplifiers in a loss-optimized optical circuit.

IV. CONCLUSION

We have presented an all-optical half-adder operating with return-to-zero pseudorandom data pattern at 10 Gb/s. The circuit exploits a 2×2 UNI-based exchange–bypass switch to obtain the logical OR and logical AND operation, and a cascaded UNI gate to obtain the SUM bit (XOR) as well as the CARRY bit (AND) of the original data. The module employs only two optical gates, requires low pulse energies to operate, and if integrated using Mach–Zehnder interferometric gates [10], the complexity of the design would be reduced making the module highly power efficient. Finally, given that the circuit uses only single-rail logic operations, its speed should be extendable well beyond 10 Gb/s [7].

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