IEICE Electronics Express, Vol.VV, No.NN, 1–6

LETTER

10 Gb/s burst-mode driver circuit with on-chip bias switch for in-Vehicle optical networks

Daisuke Ito[1a)], Yasuhiro Takahashi[1], Makoto Nakamura[1], Toshiyuki Inoue[2], Akira Tsuchiya[2], and Keiji Kishine[2]

Abstract The recent progress of in-vehicle communication networks has been highlighted by the intensive investigation of optical packet communication systems using a modulation and detection device. This paper proposes a burst-mode driver circuit with an on-chip bias switch to achieve a stable and quick response in bias switching operation. The proposed circuit comprises a driver core and two types of bias circuits. Moreover, the proposed circuit changes output bias voltages using a MOS transistor as a switch. To verify the operating principle, we design the proposed circuit using a high-voltage tolerant 65-nm CMOS technology and obtain the post-layout simulations and measurement results. As a result, we achieve quick bias switching operation with 90% faster response time than the conventional one.

key words: in-vehicle optical packet networks, burst-mode driver circuit, on-chip bias switch

Classification: Integrated circuits

1. Introduction

In-vehicle data traffic is rapidly increasing and will continue developing explosively with the increasing use of self-driving car technologies and in-vehicle communications. To realize the widespread adoption of Level 4 automated driving technology, high-capacity and low-latency in-vehicle networks are urgently required [1], [2]. Various protocols have been standardized [3], [4]. Conventional networks such as the controller area network (CAN) [5] and FlexRay [6] employ a star or bus network topology. They aim to expand the effective data rate per lane. The devices for automated driving technology, including many sensors, high-resolution cameras, and their processing systems, require broader data rate networks between electronic control units (ECUs) [7], [8]. The multimedia gigabit optical automotive Ethernet (OMEGA) has been discussed as a potential standard for gigabit in-vehicle networks [9], [10]. It is based on optical Ethernet systems and aims to realize networks faster than 10 Gb/s. However, transceivers in electronic control units (ECUs) should read the destination of received packets, thus retimers and SerDes have a delay time. This issue remains as "latency." Therefore, a novel in-vehicle network architecture (SiPhON) based on a packet network has been proposed [11], [12]. The proposed packet communication system utilizes silicon photonics technology (Fig. 1(a)) and is similar to the Token ring network [13].

The SiPhON has a broadband characteristic with a low-latency transmission [14], [15]. In the SiPhON, each ECU composes a link topology containing unidirectional fibers. Gateway (GW) devices that handle optical signals from the master come in ECUs. GW devices contain a modulation and detection device, such as LN modulators and photodiodes, which process the received optical signals. The master sends out optical packet signals. The optical packet signals are then processed by the ECU, and the signals are returned to the master. There are two types of packets: data frames, which transmit data to the ECU, and continuous-wave (CW) frames, which extract data from ECUs. The ECUs establish communication in the ring topology by processing the two types of packets. The GW devices have three types of processing: through, receive, and modulation, as shown in Fig. 1(b). The GW device passes packets that are not addressed to itself. Such packets move to the next GW device. The GW device receives the packets addressed to itself and deliver them to detection devices. In the case of sending the data from ECUs, the GW device modulates CW lights with the data by driving modulation devices. Therefore, in addition to high-speed modulation, the transmission circuit (Tx) that drives the GW device requires certain features: stable bias application to switch processing and high-speed bias switching to increase the transmission efficiency in packet communications.

This paper proposes a driver circuit with quick-response and high-stability burst-mode bias switching. The proposed bias switch uses MOS transistors to achieve high-speed responses and operational stability. The proposed circuit is designed with a high-voltage tolerant 65-nm CMOS technology to verify its effectiveness. Post-layout circuit simulations and measurement results confirmed that the proposed circuit can quickly switch output bias voltages. Consequently, the response time was reduced by 90% compared to that of the conventional circuit.

[1]Faculty of Eng., Gifu University, Gifu-shi, Gifu 501-1193, Japan
[2]School of Eng., The University of Shiga Prefecture, Hikone-shi, Shiga 522-8533, Japan
a) ito.daisuke.r8@f.gifu-u.ac.jp

DOI: 10.1587/elex.20.20230238
Received May 22, 2023
Accepted June 09, 2023
Publicized June 19, 2023

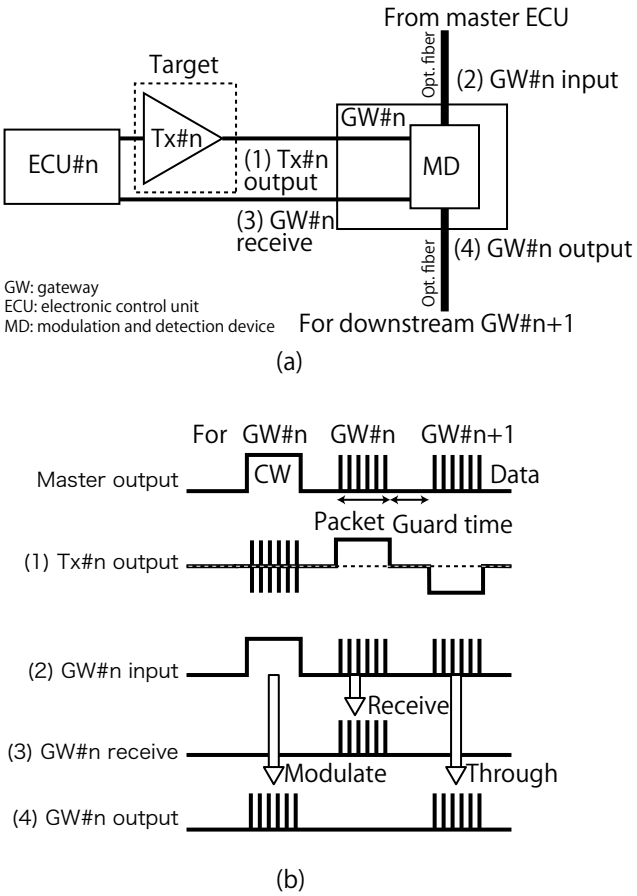


Fig. 1. Gateway device of the SiPhON in-vehicle network [15]. (a) Topology, (b) Timing chart of packet communications.

2. Conventional bias tee

A simple way to implement a bias voltage source involves using a bias tee [16], [17], [18]. The bias tee comprises a capacitor and a bias element. The capacitor C separates DC voltages between the driver core and the output stage. The bias element applies DC voltages to the output stage. Generally, a large capacitor is used to suppress the loss of low-frequency components. An inductor is used as the bias element to apply DC voltages; however, using a large inductance value to prevent losses in the low-frequency components requires an occupied chip area. Therefore, the exclusive area of the bias tee becomes large [19].

In contrast, wide-band bias tees using a high resistance value have been proposed [20], [21]. Figure 2 illustrates a conventional circuit configuration, where, $Z_{\mathrm{in,GW}}$ represents the input impedance of the GW device. The use of high-sheet resistive elements R enables the bias tee to have a smaller area than the spiral inductors. Thus, the size of the chip area can be reduced, and driver circuits can be integrated with the bias tee. The response time of this bias tee is determined by the time constant RC, and the time required for 90% convergence is approximately $2.3RC$.

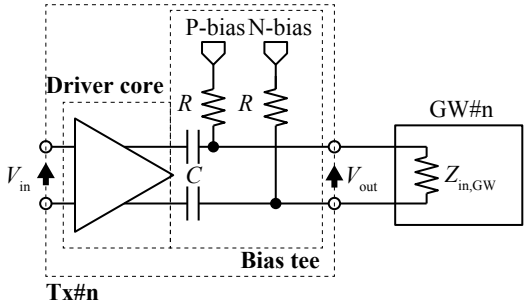


Fig. 2. Driver circuit with a conventional bias tee.

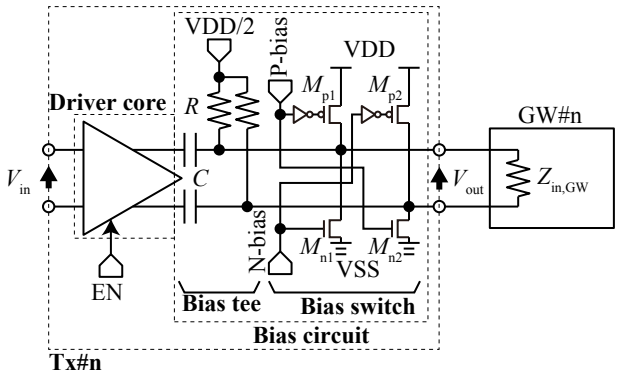
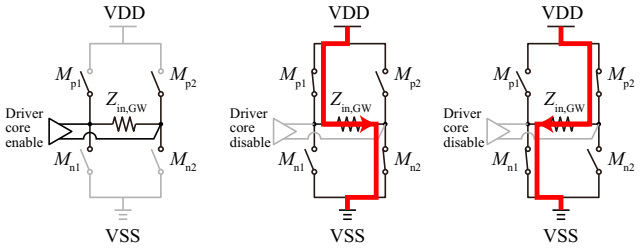


Fig. 3. Driver circuit with the proposed bias circuit.

3. Proposed bias circuit

Figure 3 shows a driver circuit with the proposed bias circuit. The circuit contains two parts: a driver core and a bias circuit. The driver core amplifies input signals and outputs. It employs an exponential inverter horn circuit [22], [23], [24] to achieve large voltage swing and wide-band characteristics. The bias circuit employs two types of circuits after the first part. The resistor-based bias tee applies a stable DC voltage ($V_{\mathrm{DD}}/2$) for the modulation. The circuit has sufficiently small implementation area for LSI fabrication. The time constant of the bias tee is 100 ns, which is shorter than the preamble period referring to 10G-EPON [25], [26]. This resistance value should be sufficiently larger than a matching impedance of the driver core and the GW device.

The bias tee which is only composed of RC network cannot be set for the desired output bias voltages quickly. Therefore, we propose a bias switch circuit to enable output bias switching. The bias switch contains four transistors, and these transistors act as a switch. The circuit consisting of the four transistors are connected in an H-bridge configuration. The equivalent resistance of a transistor depends on the gate-source voltage V_{gs}. Since the transistor behaves similarly to a switch referring gate voltages, the H-bridge composed of four switches can change the current direction. Figure 4 illustrates the operation principle of the proposed bias switch. The four transistors turn off if P-bias and N-bias pins are low voltage (Fig. 4(a)). In this case, the output signals of the driver core are applied to the load $Z_{\mathrm{in,GW}}$. When M_{p1} and M_{n2} turn on, the forward bias voltage is applied to the



(a) Modulation (b) Forward bias (c) Reverse bias

Fig. 4. Operating principle of the proposed bias switch, (a) stable bias, (b) forward bias, and (c) reverse bias for $Z_{in,GW}$.

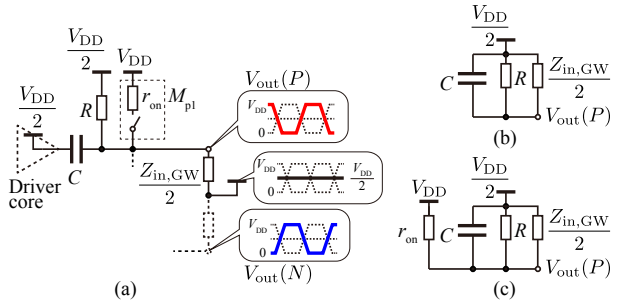


Fig. 5. (a) Half-circuit of the bias circuit and its equivalent circuits ((b) MOS switch OFF, (c) MOS switch ON).

load $Z_{in,GW}$ (Fig. 4(b)), and when M_{p2} and M_{n1} turn on, the reverse bias voltage is applied in the opposite direction (Fig. 4(c)). A high/low voltage for the P-/N-bias pins can be controlled by the current flow as shown in Fig. 4(b) and 4(c). Accordingly, the proposed driver circuit conforms to the three-processing modes.

Subsequently, we analyze the response time of the bias switch. The proposed output bias circuit drives the output voltage differentially. Therefore, the half-circuit concept can be adopted [27]. The half-circuit simplifies the proposed output bias circuit to the form shown in Fig. 5(a). The switch and the series-connected resistor r_{on} correspond to the transistor M_{p1}. Assuming the intermediate voltage $V_{DD}/2$ of the differential signal, we can deal the output load resistor $Z_{in,GW}$ to be the half value at P- and N-phases. The driver core employs an inverter-based configuration. Thus, the operating voltage of the output of driver core is $V_{DD}/2$. The OFF state switch simplifies the half-circuit to the form shown in Fig. 5(b). In this case, the time constant becomes $C(R//\frac{Z_{in,GW}}{2})$. On the other hand, when the switch is ON, the half circuit can be considered as that shown in Fig. 5(c). Therefore, its time constant is $C(R//\frac{Z_{in,GW}}{2}//r_{on})$. To provide a stable bias, a value of R is a few kΩ. The r_{on} value depends on the size of the transistor M_{p1}. $Z_{in,GW}$ represents the matching resistor of the GW device. They have significantly small values compared to the resistor R. Therefore, the time constant is shorter than the conventional one, and the proposed circuit can accelerate response time.

Signals from the driver core perturb output voltages. The signals should be blocked when the bias circuit applies constant bias voltages. Therefore, the driver core has the enable control function with the pin EN signal. The pin EN with a low voltage suspends the inter-amplifier of the driver core by blocking a power source. Thus, the driver core does not amplify input signals.

Based on the aforementioned analysis, the proposed circuit performs three processing operations quickly to drive the GW device.

4. Simulation and measurement results

The proposed circuit was designed by using a 65-nm CMOS technology. The design parameters are listed in Table I. These values are selected to achieve a response time of approximately 100 ns. The transistor size of the bias switch implies an on-resistance r_{on} of approximately 20 Ω. The response time during bias switching given by the time constant is less than 1 ns. The bias switch occupies a small area because it only contains four transistors. Therefore, the entire circuit can be compactly implemented with the bias circuit.

Table I. Design parameters of the proposed circuit.

M_{p1}, M_{p2}	M_{n1}, M_{n2}
L=400 nm, W=160 μm	L=500 nm, W=80 μm

R	C	$Z_{in,GW}$
2.5 kΩ	20 pF	100 Ω

A post-layout simulation was performed to verify the proposed circuit, where the input signal is composed of the burst packet signal with 250 mV_{ppd}, 10 Gb/s, PRBS7. Figure 6 is the time waveform for a burst packet input signal. These waveforms correspond to the differential input data signal, control signals (EN, P-bias, and N-bias), and differential output voltage. As shown in this figure, the output voltage is +2.1 V when P-bias is high, which means a forward bias. On the other hand, when N-bias becomes high, the output voltage becomes −2.1 V representing a reverse bias. When EN is high, and P-bias and N-bias are low, the circuit utilizes modulation, and the output voltage follows the input signal. Based on the simulation result, the proposed circuit can be performed through three processing operations to drive the GW device.

Subsequently, we examine the quick response characteristics during bias switching. Figure 7 shows the enlargement waveform of the P-bias and output in Fig. 6. The solid line corresponds to the output response characteristics of the proposed circuit. The dashed line shows the switching response of the conventional circuit. The P-bias changes in the order of 0 V (0–0.5 μs), 3.3 V (0.5–0.8 μs), and 0 V (0.8–1.3 μs). Based on the results, the output voltage rises gradually in the conventional circuit, and the time required for 90% convergence is approximately 150 ns. On the other hand, the proposed circuit raises the output voltage steeply and achieves a quick response time of approximately 10 ns. It is considered that the response time increases because of a parasitic impedance of a wire in the layout and a rise time

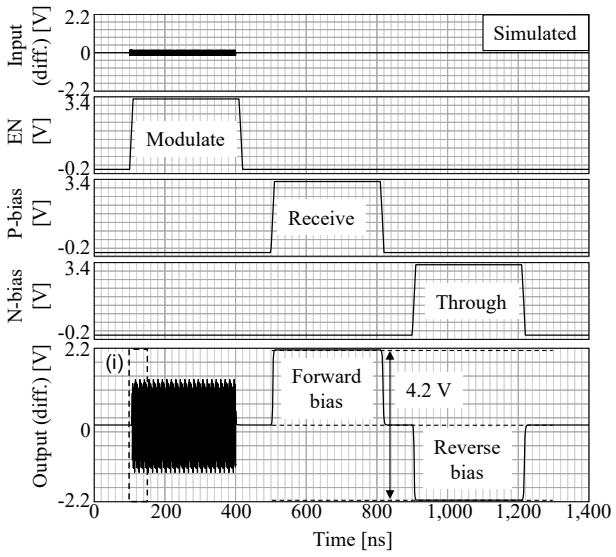


Fig. 6. Time waveforms for the burst signal (differential input, EN, P-bias, N-bias, and differential output signals).

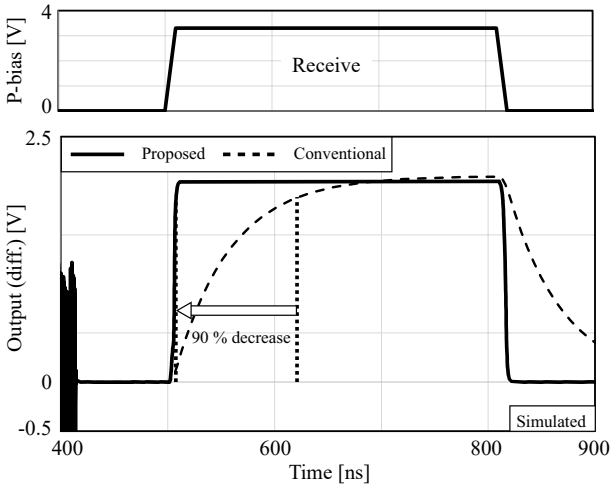


Fig. 7. Comparison of the switching response waveform for the conventional and proposed bias circuits.

of the P-bias signal (10 ns). Compared with the response time of the conventional circuit, the response time of the proposed circuit can be reduced by approximately 90%

Figure 8 shows the enlargement waveform of the area (i) in Fig. 6 to confirm the burst-mode modulating output characteristic. The rise time of the EN signal is 10 ns. The driver core resumes from the suspended state in approximately 15 ns and operates as the modulation to output data signals. Finally, we investigate an output eye pattern during the modulation. Figure 9 shows the eye diagram of the output signal during modulation. Owing the effect of the bias circuit, DC offset voltages shift gradually, resulting in a large amount of jitter, regardless the figure shows a clear eye aperture at 10 Gb/s.

The proposed circuit was fabricated using a high-voltage tolerant 65 nm CMOS process, as shown in Fig. 10. This

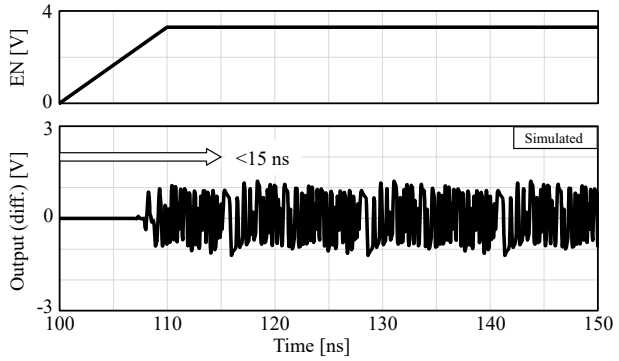


Fig. 8. Enlarged waveform of area (i) in Fig. 6 as a burst-mode output waveform for 250 mV_{ppd}, 10 Gb/s, PRBS7, NRZ input signals.

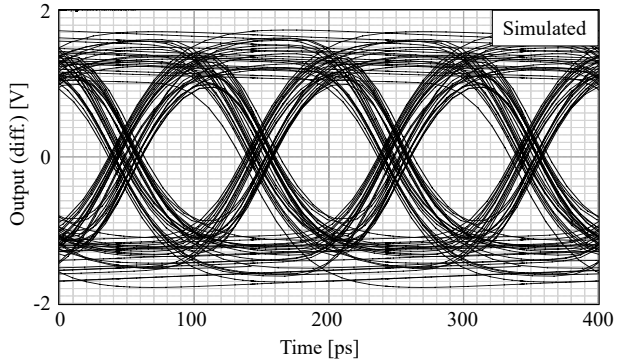


Fig. 9. Eye diagram of the proposed circuit for 250 mV_{ppd}, 10 Gb/s, PRBS7, NRZ input signals.

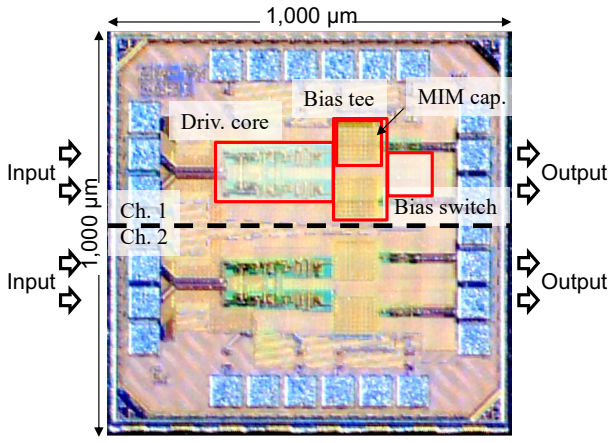


Fig. 10. Chip micro-photograph of the proposed burst-mode driver circuit (includes two circuits).

layout has two proposed circuits vertically. The rectangles in the center of the chip are metal-insulator-metal (MIM) capacitors with a capacitance of 20 pF. A MIM capacitor has a small capacitance variation on the fabrication compared to a MOS capacitor; however, its occupied area is larger than a MOS capacitor. The size of the DC-applied resistor R is extremely small. Thus, we chose a MIM capacitor. The resister R of the bias tee is a 2.5 kΩ P+ poly resistor without silicide. The size of chip area of the proposed circuit is

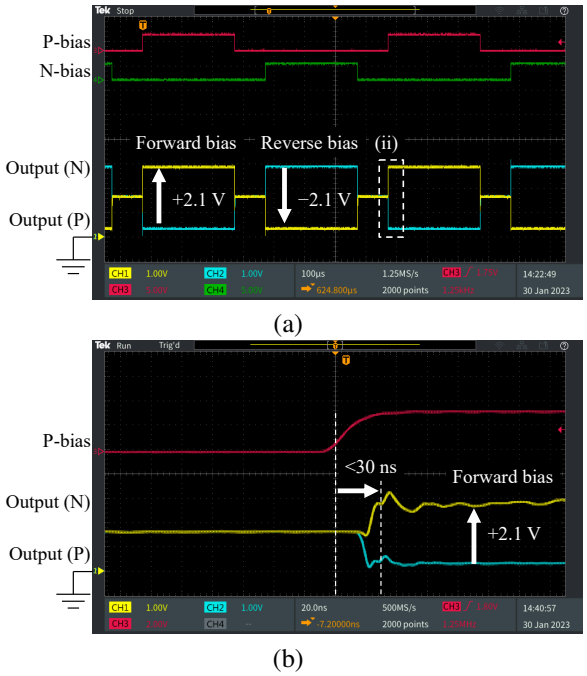


Fig. 11. Measured bias switching responses, (a) forward and reverse bias switching, (b) enlargement of (ii).

1,000 μm × 500 μm per channel.

We verified the operation of the actual chip. We measured the fabricated chip using an on-wafer probe. Figure 11 shows the waveform response characteristics during bias-switching operation. The upper two waveforms represent the control signals P- and N-bias. The output bias voltage is switched appropriately according to the control signals. When the two control signals are low, the output differential voltage is zero. Figure 11(b) displays an enlarged view of the area (ii) in Fig. 11(a). The output bias voltage responds quickly in approximately 30 ns after the rise of the control signal P-bias.

Figure 12 shows the eye pattern characteristics during modulation. Notably, the output signals were measured on a single-end form. The input signal was 10 Gb/s, PRBS31, 250 mV_{ppd}. A good eye aperture was obtained for 10 Gb/s signals. The output amplitude is approximately 2 V_{ppd}. The proposed circuit has a large amplitude output characteristic. Based on the aforementioned results, the output bias voltage of the proposed circuit can be quickly changed without using an external bias circuit and has a large amplitude output characteristic at 10 Gb/s.

Table II summarizes and compares the performance of the proposed circuits with burst-mode driver circuits for a PON system. We adopted a high-voltage tolerant transistor to achieve a large output voltage swing. The proposed circuit has the output bias switching function to apply a forward and reverse bias voltage to the GW device; however, the chip size increases. Based on this result, the proposed circuit is expected to apply to the SiPhON. Reference [29] used bipolar transistors, which consume a large amount of power. The power consumption of the proposed circuit is

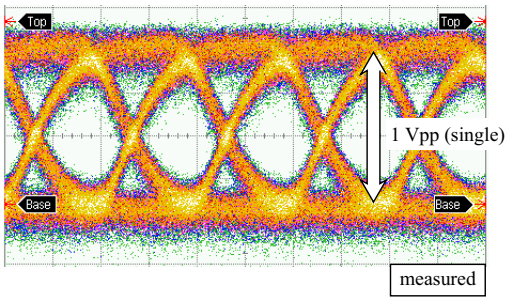


Fig. 12. Measured single-end eye-pattern for 250 mV_{ppd}, 10 Gb/s, PRBS31, NRZ input signals.

large compared to other CMOS technologies due to large output voltage swing. The response time of the proposed circuit is comparable to that of other works. Further study of power reduction techniques is desirable. We employ a figure of merit (FoM) that considers power and area efficiencies and response time to evaluate the performance of a burst-mode electrical circuit.

$$\text{FoM} = \frac{\text{Data rate}}{\text{Chip size} \times \text{Response time} \times \text{Power}} \quad (1)$$

The response time is particularly important for burst-mode circuit performance. The FoM of the proposed circuit is better than references [29] and [31] due to the low power consumption of a CMOS technology and inductor-less implementation.

5. Conclusion

This paper proposed the burst-mode driver with an on-chip bias circuit for an in-vehicle optical packet communication system. The proposed bias circuit is capable of high-speed bias switching using a transistor switch. Three operations (namely modulation, receive, and through) were confirmed by the circuit simulation and measurement using a high-voltage tolerant 65-nm CMOS technology. The response time was reduced by 90% compared to the conventional circuit. The aforementioned results highlight the prospect of the in-vehicle packet communication (SiPhON) using the proposed circuit.

Acknowledgment

This work was supported by the National Institute of Information and Communications Technology (NICT, PO: Ryo Takahashi), Japan. A part of this work was also supported by JSPS KAKENHI 22K14300.

References

[1] S. Tuohy, M. Glavin, C. Hughes, E. Jones, M. Trivedi, and L. Kilmartin: "Intra-Vehicle Networks: A Review," IEEE Trans. Intell. Transp. Syst., **16**, 2, (2015), 534.
[2] NHTSA, SAE International, SAE J3016, (2021).
[3] H.-C.V.D. Wense (Ed.), LIN Specification Package, LIN Consortium, (2003).

Table II. Performance Comparison with recently published driver circuits.

	This work	[28]	[29]	[30]	[31]
Technology	65-nm CMOS (high-voltage tolerant)	-	0.18-μm BiCMOS	32-nm CMOS	180-nm CMOS
Type	MZ driv.	LD driv.	LD driv.	MZ driv.	LD driv.
Data rate	10 Gb/s	10.3125 Gb/s	10.3125 Gb/s	25 Gb/s	1.25 Gb/s
Output Swing	2 V_{ppd}	-	1.1 V_{pp}	2 V_{ppd}	-
Chip size/ch.	0.5 mm^2	-	2.85 mm^2	0.51 mm^2	0.75 mm^2
Response time	30 ns	736 ns	15.1 ns	-	250 ns
Burst mode function	Fwd./Rev. output bias	Dynamic pow. saving	Pow. saving	-	LD turn-on/off
Avail. for SiPhON	Yes	No	No	No	No
Power consumption	390 mW	2,100 mW	1,116 mW	143 mW	200 mW
FoM*	1.709	-	0.215	-	0.033

*: Figure of merit = $\frac{\text{Data rate [Gb/s]}}{\text{Chip size [mm}^2\text{]} \times \text{Response time [ns]} \times \text{Power consumption [W]}}$

[4] MOST Cooperation, MOST Media Oriented Systems Transport, rev 2.4 ed., (2005).

[5] International Standard ISO 11898, "Road vehicles– Interchange of Digital Information– Controller Area Network (CAN) for High Speed Communication," 1st ed., International Organization for Standardization, (1994).

[6] FlexRay Consortium, FlexRay Communications System Protocol Specification, version 2.1 Edition, (2005).

[7] S. Heinrich: "Flash memory in the emerging age of autonomy," Flash Mem. Summit, (2017).

[8] A. Nasseri, et al.: "2020 Autonomous Vehicle Technology Report," WEVOLVER, (2020), https://www.wevolver.com/article/2020.autonomous.vehicle.technology.report.

[9] T. Aiba, H. Yasuda, A. Kanno, N. Yamamoto, T. Kawanishi, and T. Wakabayashi: "High SHF band RF Signal over Multi-Mode Fiber Employing Directly Modulated VCSEL," 2019 AP-RASC, (2019), 1.

[10] IEEE 802.3cz multi-gigabit optical automotive ethernet task force, (2022), https://www.ieee802.org/3/cz/.

[11] D. Kraus, H. Ivanov, and E. Leitgeb: "Novel optical network design for automotive applications using ROADMs," ConTEL 2019 - 15th Int. Conf. Telecommun. Proc., (2019), 1.

[12] O. Alparslan, S. Arakawa, and M. Murata: "Next Generation Intra-Vehicle Backbone Network Architectures," IEEE Int. Conf. HPSR, (2021).

[13] IEEE standard 802.5-1998, (1998).

[14] T. Inoue, A. Tsuchiya, K. Kishine, D. Ito, Y. Takahashi, M. Nakamura: "A Burst-Mode TIA with Adaptive Response and Stable Operation for in-Vehicle Optical Networks," IEEE ICECS 2021, (2021), 1.

[15] H. Tsuda et al.: "Proposal for a Highly Reliable In-Vehicle Optical Network: SiPhON (Si-Photonics-Based In-Vehicle Optical Network)," 2022 27th OECC and 2022 International Conference on PSC, (2022), 1, doi: 10.23919/OECC/PSC53152.2022.9849883.

[16] J. B. Carvalho, et al.: "An ultra low cost Bias Tee unit," 2011 SBMO/IEEE MTT-S IMOC 2011, (2011), 199.

[17] N. T. Kim: "Ultra-wideband bias-tee design using distributed network synthesis," IEICE Electron. Express, **10**, 15, (2013), 20130472.

[18] H. Hettrich and M. Moller: "Linear low-power 13GHz SiGe-Bipolar modulator driver with 7 V_{pp} differential output voltage swing and on-chip bias tee," in 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, (2014), 80.

[19] Marki, "Miniature surface-mount bias-tee data sheet," (2021), https://www.markimicrowave.com/Assets/datasheets/BT-0010SMG.pdf.

[20] M. P. J. Tiggelman, K. Reimann, and J. Schmitz: "Reducing AC impedance measurement errors caused by the DC voltage dependence of broadband high-voltage bias-tees," 2007 IEEE International Conference on Microelectronic Test Structures, (2007), 200.

[21] Nalli et al.: "Extremely low-frequency measurements using an active bias tee," 2013 IEEE MTT-S International Microwave Symposium Digest, (2013), pp. 1.

[22] W. J. Dally and J. W. Poulton: *Digital Systems Engineering*, Cambridge University Press, (1998).

[23] Maekawa, S. Amakawa, N. Ishihara, and K. Masu: "Design of CMOS inverter-based output buffers adapting the Cherry-Hooper broadbanding technique," ECCTD 2009, 1, (2009), 511.

[24] D. Ito, et al.: "Burst-mode driver circuit with on-chip bias tee for in-Vehicle optical networks," AVIC2022, (2022), 55.

[25] IEEE standard 802.3av, (2009).

[26] K. Tanaka, A. Agata, and Y. Horiuchi: "IEEE 802.3av 10G-EPON standardization and its research and development status," Journal of Lightwave Technology, **28**, 4, (2010), 651.

[27] B. Razavi: *Design of Analog CMOS Integrated Circuits*, McGraw-HillEducation, (2000).

[28] E. Igawa, et al.: "Symmetric 10G-EPON ONU burst-mode transceiver employing dynamic power save control circuit," OFC/NFOEC 2011, **NtuD5**, (2011), 5.

[29] H. Koizumi, et al.: "A 10Gb/s burst-mode laser diode driver for burst-by-burst power saving," Int. Solid-State Circuits Conf., **55**, (2012), 414.

[30] T. N. Huynh et al.:"Flexible Transmitter Employing Silicon-Segmented Mach-Zehnder Modulator With 32-nm CMOS Distributed Driver," IEEE J. Lightwave Technology, **34**, 22, (2016), 5129.

[31] Yong-Hun Oh, et al.: "A CMOS burst-mode optical transmitter for 1.25-Gb/s ethernet PON applications," IEEE Trans. Circuits Syst. II Express Briefs, **52**, 11, (2005), 780.