10 kV SiC MOSFET Power Module with Reduce Common-Mode Noise and Electric Field

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Abstract- **The advancement of silicon carbide (SiC) power devices with voltage ratings exceeding 10 kV is expected to revolutionize medium- and high-voltage systems. However, present power module packages are limiting the performance of these unique switches. The objective of this research is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the more recent and prominent electrostatic and electromagnetic interference (EMI) issues associated with high-speed, 10 kV devices. The high-speed switching and high voltage rating of these devices causes significant EMI and high electric field. Existing power module packages are unable to address these challenges, resulting in detrimental EMI and partial discharge that limit the converter operation. This paper presents the design and testing of a 10 kV SiC MOSFET power module that switches at a record 250 V/ns without compromising the signal and ground integrity due to an integrated screen reduces the common-mode current by ten times. This screen connection simultaneously increases the partial discharge inception voltage by more than 50 %. With the integrated cooling system, the power module prototype achieves a power density of 4 W/mm^3.[1]**

I. INTRODUCTION

Wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC), have demonstrated improved efficiency, reduced size and weight, and lower system cost compared to silicon [1],[2],[3],[4],[5]. SiC semiconductors have also demonstrated superior high-voltage capability [3],[4],[6]. While silicon devices have proven reliability and ruggedness, they have limited voltage ratings (typically 6.5 kV or less), thus requiring complex series connection of devices or multilevel converter topologies [7]. Moreover, medium-voltage silicon devices have slow switching speeds, which constrain the efficiency and switching frequency of the power converter [8],[9].

10 kV SiC MOSFETs are of great interest due to their high blocking voltage, fast switching speed, simple drivability, reverse conduction capability, and moderate on-state losses. These features can increase the efficiency, reliability, and switching frequency, and reduce the complexity, si weight of medium- and high-voltage power con systems [10],[11]. Applications include electric ship traction [9],[13], data center distribution, direct rene integration [14], fast charging stations [15], HVDC [1 FACTS [17],[18], and transformer-less intelligent substations [11],[14],[19],[20],[21].

Due to the vast possibilities for ≥10 kV SiC devices resources have been devoted to their development. T the majority of the reports on these devices have been f on the characterization [6],[11],[19],[22],[23],[24], gate design [25],[26],[27],[28], and converter eva [11],[24],[29]. However, the packaging of the semicor dies has a significant impact on the performance, currently hindering their switching speed, voltage current rating, and operating temperature. It is nontr design a suitable package for 10 kV SiC MOSFE addition to the well-known electromagnetic and t challenges associated with packaging WBG devices, t voltage rating creates new and more prominent elect and electromagnetic interference (EMI) issues, which n addressed to utilize the full capabilities of these devices

The first-generation 10 kV SiC MOSFETs were ass into a power module using a modified 6.5 kV silicon package [30]. Upon analysis and testing of the power r it was found that the parasitic inductances and capac were large and unbalanced [31], limiting the d performance and causing significant EMI. An im package for third-generation 10 kV SiC MOSFE presented in [32]. This package has lower and symmetrical parasitic inductances [32], thoug improvement in the EMI is unknown.

EMI arises from the voltage and current tran occurring during operation of the switching cell, and conducted through the electrical connections, or radiat the surrounding space. Typically, filters are added to the EMI; however, these increase the cost, siz complexity of the power conversion system. Addin external filters diminishes the power density and sin benefits gained by using 10 kV SiC MOSFETs.

In particular, conducted common-mode (CM) noi major issue with high-speed devices. CM noise is cau the high-dv/dt switching of the semiconductor devices. causes current to flow through the parasitic capaci These capacitances exist in the power module and au circuitry, such as the gate driver isolation. The latter ha

addressed in other work by reducing the isolation capacitance of the gate driver power supply [25],[26],[27],[28].

To address the issue of current flowing through the parasitic capacitances within the package, [33] proposed a method for diverting the current back to the dc bus by using two stacked direct-bonded-copper (DBC) substrates, where the intermediate metal layer is connected to the positive or negative dc bus. The amount of current that is diverted will strongly depend on the high-frequency impedance of the connection back to the dc bus. Accordingly, the implementation of this screen is critical. In [33], wire bonds are used for the interconnections, and "lugs" are used for the terminals. These connection methods have large parasitic inductances, which will reduce the effectiveness of the screen.

In [34], a similar screen is proposed. The 1.2 kV SiC MOSFET power module in [34] uses a multilayer DBC substrate, and dc-link capacitors located close to the dies. Vias in the multilayer substrate create a low-inductance connection between the middle metal layer and the negative dc bus [34]. The module has a 14-dB reduction compared to the reference module [34],[35]. While this module has several advantageous features, there are some areas for improvement. First, by connecting the middle metal to the negative dc bus, as in [33], the top ceramic is providing all the voltage isolation, and thus the second ceramic is not being fully utilized. Second, by placing the capacitors on the same plane as the MOSFETs, the footprint of the module is significantly increased. Third, the module parasitics are not well balanced, which has been shown to cause greater high-frequency noise compared to balanced designs [36].

The high-voltage rating of the 10 kV SiC MOSFETs poses a challenge for the electrostatic performance. If the electric field exceeds the breakdown field strength of the insulation materials, such as the encapsulation or insulating substrate, then partial discharge (PD) can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate, as shown in [37], thus destroying the power module. Furthermore, the PD inception voltage (PDIV) has been shown to decrease with increased dv/dt and switching frequency [38]. Due to the high-speed switching capabilities of these 10 kV SiC MOSFETs, measures must be taken to reduce the electric field concentration within the power module to ensure sufficient PDIV and breakdown voltage.

In this work, an optimized high-voltage power module package was designed, prototyped, and tested using 10 kV SiC MOSFETs. With the proposed package, the 10 kV SiC MOSFETs are able to switch at record speeds with minimal ringing and voltage overshoot. This fast switching results in significantly reduced switching losses compared to medium-voltage silicon transistors, and allows the switching frequency of medium- and high-voltage converters to be increased by orders of magnitude, which drastically reduces the size of passive components, thereby increasing the system power density. To mitigate the conducted EMI that could result from this high dv/dt, this work proposes to fully integrate a low-inductance screen into the package that limits the amount of

CM current that flows out of the power module. implementation, the capacitors are arranged above MOSFET switch pair to balance parasitic inductances maintaining a small footprint. The middle metal l connected to the dc bus midpoint, which evenly distribu electric field in the ceramic layers and reduces th electric field at the critical triple points. Thus, the pr implementation will mitigate the CM current, whi improving the voltage isolation, increasing the PDIV power module, and maintaining a small footprint fo power density.

In this paper, the EMI issues encountered during tes the first-generation 10 kV SiC power modules from [3 be presented, followed by a description of the proposed module for 10 kV SiC MOSFETs. The a implementation, and preliminary testing of the integrat screen will then be discussed. Methods for reduci electric field concentration within the power module reviewed, and the proposed technique will be an Finally, the experimental switching tests that demonstr high-speed transients and low CM current of the pr package will be presented. Partial discharge tests val the improved voltage capability provided by the CM will also be shown.

II. EMI LIMITATIONS FOR HIGH-VOLTAGE SiC POW MODULES

The development of 10 kV SiC MOSFETs [39] and SiC junction barrier Schottky (JBS) diodes [40] gave the first 10 kV SiC power module [30]. The half modules comprise twelve parallel 10 kV, 10 A DMOSFETs, and six parallel 10 kV, 10 A SiC JBS dio switch position, yielding a current rating of 120 A [30] 10 kV SiC modules demonstrated higher efficien switching frequency potential than 6.5 kV silicon modules [8], and were critical components in the devel of a high-density 1 MVA solid-state power substation. employed soft switching techniques and was capa switching up to 20 kHz [41]. These modules were also demonstrate the first medium-voltage impedance measu unit (IMU) capable of characterizing in-situ source a impedances of dc and ac networks up to 4160 V ac, 6 dc, 300 A, and 2.2 MVA [42]. Unfortunately, the full and power levels could not be achieved due to sign unresolvable EMI. Upon further evaluation, it was fou substantial current was flowing through the system g The contaminated ground was causing the contro malfunction, thereby limiting the operating conditions.

As mentioned previously, under a voltage exc parasitic capacitances can become a path for CM cur flow. Within the power module, parasitic capacitance across the ceramic substrate that isolates the semicon devices from the cooling system. Since the cooling sy generally grounded for safety, under high-speed transients, this parasitic capacitance becomes a path f current to flow through the system ground [36]. Therefo

capacitance should be minimized, especially for fast-switching devices.

From ANSYS Q3D simulations, the parasitic capacitance between the output node of the half-bridge and the module baseplate is approximately 300 pF. Discrete switching tests were conducted on these power modules to characterize the dynamic performance [43]. At 4.7 kV and 100 A, the power modules had a maximum dv/dt of 22 V/ns [43]. This measured dv/dt and simulated parasitic capacitance give a calculated peak current of nearly 7 A. It should be noted that the 22 V/ns switching speed was achieved with internal and external gate resistances slowing down the devices. If these resistances were reduced or eliminated, then the switching speed would increase, which would raise the efficiency, but worsen the CM current. Therefore, this capacitance is limiting the operation of the 10 kV SiC MOSFETs. The package proposed in this work reduces this EMI without sacrificing the efficiency by minimizing the parasitic capacitance, and integrating a screen that contains the generated CM current within the power module.

III. MODULE OVERVIEW

Fig. 1 shows the designed half-bridge power module, which has three 10 kV, 350 mΩ SiC MOSFET dies in parallel per switch position. No external anti-parallel diodes are used. The module has a planar, sandwich structure, using metal posts and direct-bonded-aluminum (DBA) substrates as the die interconnection instead of wire bonds. Similar structures were proposed in [44] and [45] for lower-voltage silicon IGBTs. This type of structure allows for increased power density, and reduces the parasitic inductances and capacitances in the module, thereby improving the dynamic performance. Furthermore, by eliminating the wire bonds, the module will be able to withstand higher-energy faults, as shown in [46]. This structure also allows decoupling capacitors to be embedded within the module to further improve the dynamic performance without increasing the module footprint.

In total, four substrates are used in the power module: two beneath the dies (DBA1 and DBA2) and two on top (DBA3 and DBA4). DBA1 and DBA2 are used to reduce the CM current flowing through the system ground and to decrease the peak electric field strength within the power module. With the housing and integrated cooler, the module dimensions are 70 mm × 80 mm × 25 mm. Details on the design and prototyping of this power module are reported in [47],[48],[49].

Fig. 2 shows two module prototypes: a low-current module with two dies (Fig. 2(a)), and a high-current module with six dies (Fig. 2(b)). The low-current module was fabricated to test the prototyping procedures, and was used for initial testing. The testing of these module prototypes will be presented in section VI.

IV. COMMON-MODE SCREEN

A. Impedance Analysis

In this section, the CM path impedances will be analyzed. Fig. 3 shows a schematic of the power module with the key impedances that will be considered. For the generated CM
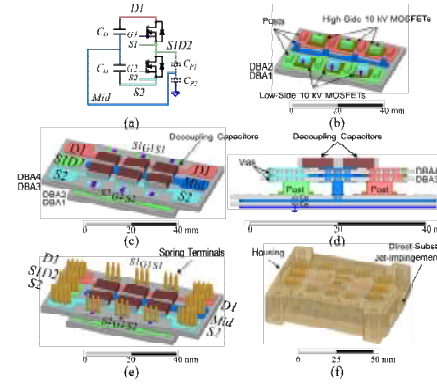

Fig. 1 (a) Schematic and 3D models of the (b) bottom and (c) cor[...] assemblies, (d) side-view of the module, (e) terminal arrangement[...] housing with integrated cooler. The colors in the 3D models corre[...] to the nodes in the schematic with the same color.
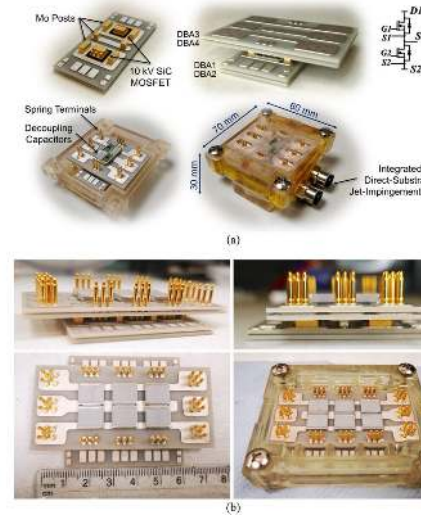

Fig. 2 10 kV SiC MOSFET module prototypes with (a) two 10 kV [...] MOSFET dies, and (b) six 10 kV SiC MOSFET dies.

current to be diverted from the ground to the scre[...] impedance of the screen path must be much lower than[...] the ground path, especially at high frequency. The co[...] required for the screen to effectively divert the CM [...] from the ground path to the dc bus may be summar[...] follows:

$$Z_{screen} << Z_{gnd}$$

where Z_{screen} and Z_{gnd} are the impedances of the screen and ground paths, respectively. Considering the parasitic elements shown in Fig. 3, these impedances can be defined as:

$$Z_{screen} = \omega L_{screen} + 1/(j\omega C_D) + R_{screen} \qquad (2)$$

$$Z_{gnd} = \omega L_{gnd} + 1/(j\omega C_{P2}) + R_{gnd} \qquad (3)$$

where L_{screen} and L_{gnd} are the parasitic inductances in the screen and ground paths, R_{screen} and R_{GND} are the parasitic resistances in the screen and ground paths, C_D is the decoupling capacitance, and C_{P2} is the parasitic capacitance of the bottom substrate, which is connected to ground (Fig. 1(d)). As shown by (2), to minimize Z_{screen}, L_{screen} should be as small as possible, while C_D should be large. From (3), it can be seen that a smaller C_{P2} results in a greater Z_{gnd}. Substituting (2) and (3) into (1) gives:

$$\omega L_{screen} + 1/(j\omega C_D) + R_{screen} << \omega L_{gnd} + 1/(j\omega C_{P2}) + R_{gnd} \qquad (4)$$

From (4), it can be seen that the effectiveness of the screen is dependent on the parasitic elements, which are determined by the implementation. To effectively reduce the CM current, the power module should be compact such that C_{P2} and L_{screen} are small, yet capable of accommodating sufficient decoupling capacitance C_D. The L_{gnd} and R_{gnd} will vary depending on the system integration, and are therefore out of the control of the power module designer. Accordingly, this work focuses on minimizing C_{P2} and L_{screen}, and maximizing C_D. A more general theoretical analysis of CM impedances is presented in [50].

B. Preliminary Testing

Prior to constructing the 10 kV SiC MOSFET power modules, it was desirable to understand the effects of the proposed screen on the CM noise. Accordingly, a half-bridge module with 1.2 kV, 80 mΩ SiC MOSFETs (C2M0080120D) was built and tested in a boost converter. For the test, the module substrate was directly mounted onto a copper ground plane. No cooling system was added between the substrate and the ground plane to improve the measurement results. Due to the absence of a cooling system, the tests were conducted at
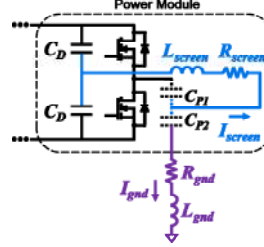

Fig. 3 Power module schematic with parasitic impedances of the ground (purple) and screen (blue) paths.

low power (360 W). The output voltage was 60 V, a switching frequency was 50 kHz.

For the prototyped 1.2 kV SiC modules, the p capacitance from the output node to the middle meta C_{P1}, was 20 pF, and the parasitic capacitance from the metal layer to the ground, C_{P2}, was 150 pF. These valu measured on the prototype using an impedance analyz were verified by calculation and Q3D simulation. C_{P2} i than C_{P1} because the middle and bottom metal layers co entire substrate area, whereas the output terminal mak small portion of the footprint.

For the tests, a high-frequency current transformer (was used to measure the current of the line imp stabilization network (LISN). The output of the HFC connected to an EMC analyzer. The measured current cases are shown in Fig. 4. The first case has a single su and no decoupling capacitors. The second case h stacked substrates and no decoupling capacitors. Th case has two stacked substrates and two 680-pF dec capacitors in parallel and two in series, but the middl layer of the substrate stack is left floating. The fourth similar to the third, but has two series 10-nF capacito fifth case connects the middle metal layer of the su stack to the midpoint of the series decoupling capacitor

When two substrates are stacked together (case 2), th decreases by just a few dB compared to case 1 with a substrate. This indicates that the reduction in the p capacitance offered by the second substrate is not suffi lower the CM noise. The addition of 680-pF dec capacitors in case 3, on the other hand, reduces th frequency noise by more than 10 dB compared to case a single substrate. The decoupling capacitors also ca resonant frequency to decrease. When the dec capacitance is increased to 10 nF (case 4), then the r frequency further decreases, and the high-frequency n reduced by a few more dB. This is in agreement w which shows that increasing the decoupling capacitanc to reduce the high-frequency impedance of the scre When the middle metal of the substrate stack is conne the midpoint of the two series 10-nF capacitors (case the high-frequency noise decreases by more than 15 dB larger frequency range. This is because there is now impedance, high-frequency path for the generated CM to flow. This preliminary testing demonstrates the pote the screen to reduce the CM noise.

The gate-source and drain-source voltages and drain of the 1.2 kV SiC MOSFET were also monitored dur testing. By adding decoupling capacitors, the frequency in the drain-source voltage reduced, and th increased, resulting in greater current overshoot and amplitude ringing. This ringing and overshoot can be r by decreasing the power-loop inductance, which w optimized in this module prototype. Connecting the metal layer to the decoupling capacitor midpoint did n noticeable changes in the MOSFET voltage and waveforms. Therefore, if the parasitic inductances and
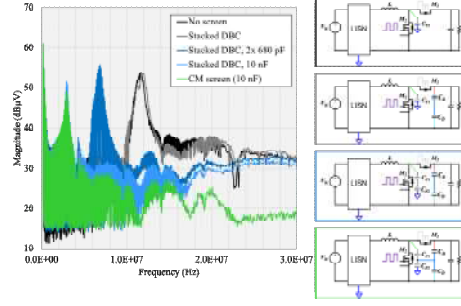
Fig. 4 Measured LISN current in 1.2 kV-SiC-based boost converter with (green waveform) and without (black, grey, and blue waveforms) the proposed CM screen.

decoupling capacitors are carefully designed, the proposed CM screen will have minimal impact on the MOSFET losses.

C. Implementation

To achieve a low-impedance implementation for the CM screen in the 10 kV power module, it is proposed to embed capacitors, and to use vias within the insulating ceramic substrates to make the connection between the middle metal layer and the capacitor potentials. In [50], the capacitors are placed above the semiconductor devices, creating a vertical high-frequency power loop that does not increase the module footprint, as it takes advantage of the third dimension. In this work, this vertical-capacitor-loop concept was adopted with some modifications. Each 10 kV SiC MOSFET switch pair has its own set of decoupling capacitors located above it (Fig. 1(c)), resulting in a symmetric power loop inductance of just 4.4 nH for each. In this embodiment, two capacitors are placed in series, and the midpoint, which is at half of the dc bus voltage, is connected to the middle metal of the substrate stack. By connecting the screen to the decoupling capacitors within the power module, the influence of the parasitic impedances external to the package are diminished thereby improving the effectiveness of the screen.

According to ANSYS Q3D simulations, this connection method has less than 2 nH parasitic inductance, allowing for a high proportion of the CM current to be diverted to the dc bus and contained within the power module. Additionally, the S1D2 pad area was designed as small as possible to minimize C_{P1}. For the proposed high-current 10 kV power module shown in Fig. 1 and Fig. 2(b), C_{P1} is 46 pF, and C_{P2} is 160 pF, according to ANSYS Q3D simulations. For the decoupling capacitors (C_D), a surface-mount, 680 pF, C0G, 5 kV multilayer ceramic capacitor was selected. As shown in Fig. 1(c), there are three capacitors in parallel—one above each MOSFET switch pair—giving an equivalent capacitance of 2.04 nF.

V. ELECTRIC FIELD REDUCTION

To address the enhanced electric field associated high-voltage, high-density package, the ceramic su must be thoughtfully designed and evaluated. In modules, the electric field concentrates at the intersec the ceramic, metal, and encapsulation [52],[53],[54],[55 is known as the triple point. If this electric field exce breakdown field strength of the insulation materials, the ceramic or encapsulation, then PD can occur. Rep PD events can ultimately result in insulation failure, cracking of the ceramic substrate as shown in [37 destroying the power module.

In the literature, it has been shown that the PD standard 1-mm-thick aluminum nitride (AlN) DBC su is less than 10 kV rms [37], and can be as low as 5 k [56]. This does not provide sufficient margin for 10 k MOSFETs. Accordingly, methods for reducing the electric field within the power module need to be ex There have been several proposed solutions to redu electric field strength at the triple point, including: inc the ceramic thickness [37]; varying the metal pad si pad corner curvature [37], offset between the top and pads [37], and metal-ceramic interface ge [57],[58],[59]; and stacking multiple substrates [56]. N these previously proposed solutions were implement tested in an actual power module, and several of the complicate the module manufacturing. The method pr in this work, is an adaptation of the latter meth effectively increases the PDIV, and is simple to implem

In [56], it was shown that stacking DBC sub reduces the electric field strength within the bulk ceram at the critical triple points. The PD tests revealed t PDIV could be increased by 94 % by stacking two 0. Al_2O_3 substrates compared to having a single 0. substrate [56]. However, the practical implementation method was not explored. In a power module, the t bottom metal layers are not symmetrical; the top m patterned to create the circuit (e.g., half bridge), a various traces are at different potentials during the operation. As a result, it is not clear what potential sh applied to the middle metal layer to achieve a mea reduction in the electric field strength. This key factor realization of this method is explored in this work.

Fig. 5 shows the simulated 2D electric field distr for the case when the top metal is patterned and h different potentials. One of the potentials represents th of the high-side switch, and the other represents the d the low-side switch. The former is consistently at the p dc bus potential while the latter switches between the p and negative dc bus potentials. The worst-case scen when the low-side switch is conducting and its drain is negative dc bus potential. This worst-case was simulate positive dc bus is set to 10 kV, and the negative is set The bottom-most metal is at the same potential as the system, which is grounded (0 V).

Fig. 5(a) shows the simulated electric field plo single DBA substrate. It can be seen that the electri

distribution is non-uniform within the bulk of the ceramic, and that the peak electric field occurs at the triple points. The peak electric field exceeds 20 kV/mm, which is the typical breakdown field strength for ceramic substrates.

Fig. 5(b) shows the simulated electric field plot for two stacked DBA substrates with the middle metal layer connected to the negative dc bus (0 V), as proposed in [33] and [34]. Comparing Fig. 5(a) and Fig. 5(b), it can be seen that connecting the middle metal to the negative dc bus does not reduce the peak electric field at the triple point, nor does it improve the distribution within the bulk ceramic, compared to the single substrate case. This is because the bottom substrate has 0 V across it, while the top substrate has 10 kV. In this implementation, the bottom substrate is not helping to support the voltage, and is therefore not being fully utilized.

If the middle metal is connected to the positive dc bus, as proposed in [33], then the triple points at which the peak electric field occur will change, and the electric field distribution within the bulk ceramic will shift. This is shown in Fig. 5(c). Although the distribution and critical triple points have changed, the peak electric field, and therefore the PDIV, are similar to the case with a single substrate. This is because both the top and bottom substrates have 10 kV across them.

If instead the middle metal is connected to half of the applied voltage, then both the top and bottom substrates have a potential of 5 kV across them. The simulated electric field distribution for this case is shown in Fig. 5(d). The simulated peak electric field is reduced by 58 % compared to the single-substrate case (Fig. 5(a)), and the electric field in the bulk ceramic is uniformly distributed in the two substrates. Therefore, in this work, the middle metal layer of the DBA stack is connected to half of the bus voltage.

The connection of the middle metal layer to half of the bus potential can be realized with the embedded decoupling capacitors. Each set of decoupling capacitors shown in Fig. 1(c) consists of two, 5 kV ceramic capacitors placed in series. From Fig. 1(d), it can be seen that the midpoint of the capacitors is connected to the middle metal layer of the bottom DBA stack through vias and metal posts. This connection allows the middle metal layer to be connected to half of the bus voltage, thus reducing the peak electric field in the power module.

VI. EXPERIMENTAL RESULTS

A. Switching Testing

To evaluate the switching performance of the proposed 10 kV power module, double-pulse tests (DPT) were performed on the low-current prototype shown in Fig. 2(a). The DPT schematic and setup are shown in Fig. 6. The gate driver used for the DPTs was adapted from the one presented in [60]. The low-side 10 kV SiC MOSFET was driven from +20 V in the on-state to -5 V in the off-state. The body diode of the high-side 10 kV SiC MOSFET was used as the free-wheeling
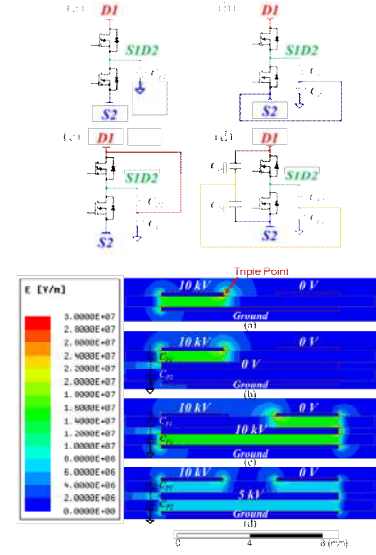

Fig. 5 Simulated 2D electric field distribution for (a) a single subst... and two stacked substrates with the middle metal at the (b) negative... bus, (c) positive dc bus, and (d) dc bus midpoint.
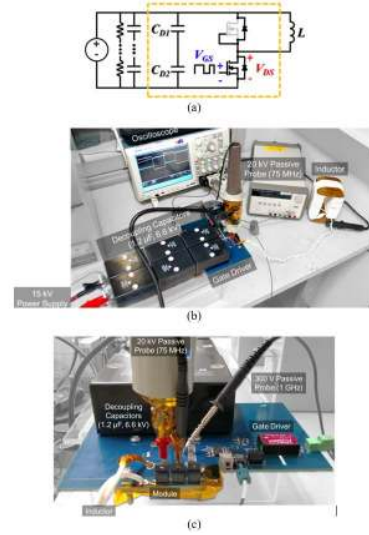

Fig. 6 Double-pulse test (a) schematic with the power module indi... by the yellow box, (b) hardware setup, and (c) module connection.

diode. The gate driver PCB is mounted on top of the power module to achieve small gate-loop inductance between the driver and the module.

The gate-source and drain-source voltages of the low-side SiC MOSFET were monitored using a 300 V passive probe with a bandwidth of 1 GHz, and a 20 kV passive probe with a bandwidth of 75 MHz, respectively. As shown in Fig. 6(c), these probes are placed directly above the MOSFET terminals to minimize the parasitic inductance in the measurement loop. Due to the embedded decoupling capacitors, the drain current of the SiC MOSFETs could not be measured. A 15 kV power supply was used to charge the external decoupling capacitors. Each capacitor is 0.82 µF and rated at 3.3 kV (MP80CV824K [61]). Six total capacitors were used—two in series and three in parallel for a total capacitance of 1.2 µF and voltage rating of 6.6 kV. Three capacitors were put in parallel to increase the capacitance and to reduce the inductance; each capacitor has an equivalent series inductance of 30 nH [61].

Fig. 7 shows the gate-source and drain-source voltage waveforms for the turn-on and turn-off transients for the DPTs performed on the module shown in Fig. 2(a). The switching tests were performed up to 5 kV and 20 A with turn-on and turn-off gate resistances of 0.33 Ω and 0.17 Ω, respectively. Table I lists the measured overshoot, undershoot, rise and fall times, and switching rates from the DPTs. During the turn-on transient, the fall time of the drain-source voltage is 16 ns, giving a dv/dt of 250 V/ns. At turn-off, the voltage rise time is 50 ns, which is a dv/dt of 80 V/ns. The voltage rise time is longer because it is controlled by the output capacitance and load current. Negligible voltage overshoot and ringing were measured, indicating low power- and gate-loop inductances. This is due to the low-inductance module design, as well as careful layout and connection of the gate driver, bus bar, external decoupling capacitors, and measurement probes.

To the best of the author's knowledge, these are the fastest switching speeds reported for similarly-rated SiC MOSFETs and IGBTs. In fact, this is more than two times faster than those reported in [24],[32],[62],[63]. In [32], switching results for a module populated with a single die had turn-on and turn-off transition times of approximately 80 ns and 120 ns, respectively, giving switching speeds of 88 V/ns and 58 V/ns at a bus voltage of 7 kV, drain current of 15 A, and gate resistance of 21 Ω. The switching waveforms also showed a moderate voltage overshoot of approximately 300 V (4.3 %) [32].

For a discrete 4 kV silicon IGBT, the datasheet reports voltage rise and fall times of 146 ns and 514 ns at 1.25 kV, 30 A, and 2 Ω external gate resistance [64]. These switching times result in dv/dt values of 8.6 V/ns and 2.4 V/ns for the rise and fall, respectively, which are 10 and 100 times slower than the switching speeds achieved in this work. Accordingly, the proposed power module can enable faster-switching, higher-voltage power converters while maintaining high efficiency.
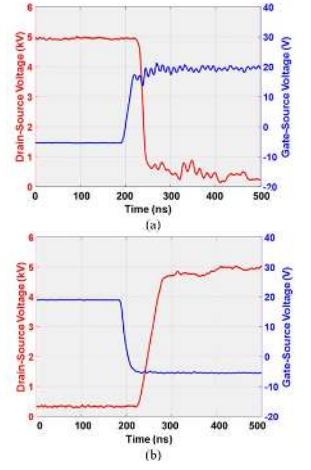

Fig. 7 (a) Turn-on and (b) turn-off gate-source (blue, right axis) and drain-source (red, left axis) voltages.

TABLE I
10 kV, 350 mΩ SiC MOSFET Module Prototype Switching Res...

Parameter	Value	
	Gate-Source Voltage	Drain-Source Voltage
Overshoot	None	None
Undershoot	None	None
Rise Time	24 ns	50 ns
Rise dv/dt	0.9 V/ns	80 V/ns
Fall Time	26 ns	16 ns
Fall dv/dt	0.8 V/ns	250 V/ns

B. Common-Mode Screen Testing

To evaluate the effectiveness of the integrated CM screen on the 10 kV power module, switching test performed. As mentioned earlier, the CM current incre the dv/dt and parasitic capacitances increase. To impr signal-to-noise ratio of the CM current measurement, th was reduced. This was achieved by lowering the voltage to 2 kV. To ensure sufficient CM current co measured, the larger power module with three 10 k MOSFET dies in parallel per switch position was use 2(b)) [65]. The C_{P1} and C_{P2} of this 10 kV prototype ar and 162 pF, respectively.

Fig. 8(a) shows the schematic of the tests when t screen is not connected (the middle metal layer of the substrate stack is floating). Fig. 8(b) shows the schem the tests when the CM screen is connected to the ca midpoint. An inductor with high-voltage wire for the v was connected across the high-side switch of the half module. The body diode of the high-side SiC MOSF used to freewheel the current in the inductor when th side switch was off.

To validate the performance of the CM screen, the through the ground path, I_{gnd}, was measured, as shown i
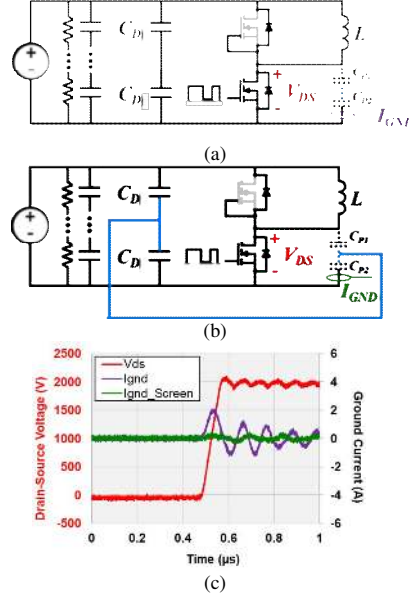
Fig. 8 Schematic of the testing setup when the screen is (a) not connected and (b) connected, and (c) drain-source (red, left axis) and ground current (right axis) waveforms with (green) and without (purple) the common-mode screen.

8, using an RF current transformer with a bandwidth of 200 MHz. For these tests, the middle metal layer was connected to the midpoint of the two series 680-pF decoupling capacitors. Three capacitors were placed in parallel.

Fig. 8(c) shows the turn-off drain-source voltage and ground current waveforms with and without the screen at 2 kV and 20 A with no external gate resistance. The voltage rise time at turn off is 66 ns, which gives a dv/dt of 24 V/ns. This dv/dt is lower than the previous switching tests because of the lower bus voltage and larger device capacitance due to the three MOSFET dies in parallel. The measured peak current through the ground path without the proposed screen is 2 A. This peak current will increase as the dc bus voltage, and therefore the dv/dt, increases. With the CM screen connected, the measured peak current through the ground path is reduced to 0.2 A. This is an order of magnitude reduction.

C. Partial Discharge Testing

PD tests were conducted to validate the electrostatic simulation results. The PD tests were performed using a 50 kV, 100-mA, 60-Hz power supply as the excitation source. To detect the PD events, a Doble PD Smart with HFCT-300 sensor was used [66]. The Doble PD Smart complies with IEC 60270 and VDE 0434, among other standards [66]. PD signals at frequencies from 35 kHz to 20 MHz and an apparent charge as low as 0.2 pC can be measured [66].

PD tests were performed on a patterned, 1-mm-thic DBA substrate. The spacing between metal traces an the metal traces to the edge of the ceramic was 2 mm cases were tested: 1) a single substrate, 2) two substrates with the middle metal connected to the ground, and 3) two stacked substrates with the middle connected to half of the applied excitation voltage. Eac was tested under two conditions: 1) S1D2= D1 (the hi switch is conducting and the low-side switch is blockin 2) S1D2= S2 (the high-side switch is blocking and th side switch is conducting).

First, the PD tests were performed with the sample to have a high signal-to-noise ratio. These tests reveal as was shown in the electrostatic simulations, the PD DBA substrates will occur at the triple points. Specifica PD will take place along the edge of the metal pad wh high potential is applied. The resulting PDIV for th when the samples are tested in air are listed in Table II S1D2 is equal to D1 (the applied voltage), and the metal is connected to half of the applied voltage, the increases by 53 % compared to the single-substrate cas The same increase in PDIV was observed when S1D2 i to S2 (ground). These results, which are in good agr with the simulations, demonstrate that connecting the metal to half of the applied voltage gives pred consistent results for both switching states.

Since the power module will be encapsulated, P were also performed on a stacked substrate sample th encapsulated with SilGel 612 from Wacker. For this the S1D2 potential was connected to S2 (the worst cas measured PDIVs for this sample are listed in Table II the middle metal is connected to the source ground, th is 7.4 kV rms (10.5 kV peak). For this same case, brea occurred at 8.5 kV rms (12.0 kV peak). This means middle metal is connected to ground, or if a single subs used, then there is 20 % margin between the peak brea voltage and the voltage rating of the 10 kV SiC MOSFE

When the middle metal is connected to half of the voltage, no PD could be measured up to 10.5 kV rms (1 peak). The testing was stopped at 10.5 kV rms due reduced signal-to-noise ratio. This suggests that encap stacked substrates with the middle metal connected to the applied voltage will have more than a 40 % higher F

TABLE II
Partial Discharge Testing Summary

Sample	Voltage of Middle Metal	Surrounding Medium	S1D2 Potential	PDIV (rms)
Single Substrate	N/A	Air	D1	1.7 kV
	N/A	Air	S2	1.7 kV
Stacked Substrates	½ × V_{AC}	Air	D1	2.6 kV
	½ × V_{AC}	Air	S2	2.6 kV
Encapsulated Stacked Substrates	0 V	SilGel 612	S2	7.4 kV
	½ × V_{AC}	SilGel612	S2	>10.5 kV

compared to a single substrate or a stacked substrate with the middle metal connected to ground. Therefore, it is advantageous to use the stacked substrate structure with the middle metal connected to half the applied voltage to increase the high-voltage performance of the power module.

VII. CONCLUSIONS

This work proposed a high-density power module for 10 kV SiC MOSFETs with reduced CM current and electric field strength. The optimal layout and system interface enable the module to switch 5 kV in tens of nanoseconds with negligible ringing and voltage overshoot. This is the fastest switching speed reported to date for 10 kV SiC MOSFETs. To reduce the adverse EMI effects of this high-speed switching, a CM screen was incorporated into the power module design. This screen was realized by stacking two DBA substrates and connecting the middle metal to the midpoint of embedded decoupling capacitors through vias and metal posts. This proposed method creates a low-impedance path at high frequency, and contains the current that would normally flow to the system ground within the power module. With this screen, the measured CM current leaving the power module decreases by ten times. This proposed integrated screen will reduce the need for filtering at the system level, thereby increasing the power density, lowering the cost, and simplifying the design of power electronic systems. Moreover, it will permit the operation of the 10 kV SiC MOSFETs at faster speeds, thereby reducing losses and increasing efficiency.

This screen also increases the voltage rating of the power module. PD tests showed that stacking two substrates and connecting the middle metal to half of the applied voltage increases the PDIV by 53 % compared to a single substrate. When testing two encapsulated stacked substrates with the middle metal connected to the source ground, breakdown occurred at 8.5 kV rms (12.0 kV peak). This breakdown voltage limits the voltage rating of the package. When the middle metal of the encapsulated substrates is connected to half of the applied voltage, the PDIV exceeds 10.5 kV rms. This method for reducing the electric field is effective and simple to implement, and will enable high-voltage packages with greater power density.

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