10 nm electron beam lithography and sub-50 nm overlay using a modified scanning electron microscope

P. B. Fischer and S. Y. Chou
University of Minnesota, Department of Electrical Engineering, Minneapolis, Minnesota 55455

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Gratings of 10 nm wide metal lines 30 nm apart, and quantum transistor gates with 10 nm wide gaps over 300 nm long between two metal rectangles have been repeatedly achieved on thick GaAs substrates using a modified scanning electron microscope operated at 35 keV and liftoff of Ni/Au. Furthermore, multilevel electron beam lithography with a standard deviation (3σ) of an overlay accuracy (30 deviation) of 50 nm has been achieved using the same modified scanning electron microscope.

The desire to study the high-speed operation and quantization effects of semiconductor devices has motivated research on the fabrication of 10 nm lateral structures. For examples, lateral quantum effect devices require ultrasmall gate geometry,[1] and metal-semiconductor-metal photodetectors require extremely dense patterns of very fine interdigitated metal fingers for high performance.[2] In addition to high resolution, high overlay accuracy is another requirement in the lithography for many novel semiconductor devices. Modified scanning electron microscopes (SEMs) are an attractive tool for nanofabrication and nanodevice research due to their high resolution, high flexibility, and low cost. However, a modified SEM does not offer a direct means for high-accuracy multilevel overlay.

Previously, modified SEMs have been used to produce 10 nm wide isolated lines and gratings of 40 nm period with 12 nm linewidth on membranes,[3] as well as 10 nm wide isolated lines and gratings of 40 nm period with 10 nm linewidths on bulk GaAs substrates using a 250 keV beam exposure and chemically assisted ion beam etching with polymethyl methacrylate (PMMA) as an etch mask.[4] However, little work has been reported on ultrahigh overlay accuracy in multilevel e-beam lithography using a modified SEM.

This letter presents the study of lithographic resolution as well as overlay capability of a modified SEM operated at 35 kV. Using a liftoff technique with PMMA resists, 10 nm metal features, either isolated or periodic with periods as small as 40 nm, have been consistently achieved on bulk GaAs substrates. A liftoff process is used because it is more difficult and challenging to achieve nanostructures than etching with a PMMA etch mask. Moreover, sub-50 nm overlay accuracy has been accomplished.

In order to achieve ultrasmall structures in PMMA, the exposure of the resist by backscattered and laterally scattered electrons must be minimized. This can be accomplished by using thin resists and relatively small exposure areas. In our experiment, GaAs wafers were coated with a 45 nm thick layer of 950 K PMMA by spinning a 1.6% solution of 950 K PMMA (in chlorobenzene) at 6.0 krpm for 60 s. The samples were then baked for 12 h at 165 °C. Our e-beam lithography system consists of a modified JEOL-840A SEM with a tungsten filament gun and equipped with a magnetic beam blanking unit and electronic rotation system. The writing field can vary from 3×4 μm to 150×250 μm by selecting different magnifications of the microscope. A personal-computer controlled pattern generator is used to control the SEM. The pattern generator was designed and built in house, utilizes a commercial computer-aided design package for pattern specification, and offers a digital-to-analog converter resolution of up to 14 bits. Several measures have been taken to reduce noise from floor vibrations and electronics. High resolution exposures are performed using a field size of 34×26 μm^2, and DAC resolution of $2^{12}\times2^{12}$ pixels.

Exposures were performed with an accelerating voltage of 35 kV, and a beam diameter of about 4 nm. In order to achieve ultra-small features, a high contrast developer-resist system was used. Development was done at 23 °C using 2-ethoxyethanol:methanol (3:7) for 7 s, methanol for 10 s, and isopropanol for 30 s. The contrast of this development process for 950 K PMMA has been measured to be seven. After development, metals were deposited by e-beam evaporation. Liftoff was performed by alternately soaking in warm acetone and spraying with a pressurized acetone jet.

Both isolated and densely spaced patterns with 10 nm features have been obtained. Figure 1 shows a scanning electron micrograph of a 40 nm period grating with 10 nm linewidths on bulk GaAs. In this particular example only 3.5 nm of Ni and 4 nm of Au have been used, but liftoff is still possible with total metal thicknesses of 20 nm. The exposure dose for the grating was 0.9 nC/cm and must be carefully controlled. The exposure area is 2 μm$\times$1.3 μm and the liftoff was successful over the entire area. Gratings with a period smaller than 40 nm were patterned in PMMA, but did not liftoff properly.

Figure 2 shows a scanning electron micrograph of a Ni/Au (7 nm/8 nm) constricted gate for a quantum field-effect transistor with a gap of 10 nm and a gate length of 330 nm on bulk GaAs. The constricted gate was exposed with a dose of 480 μC/cm^2. This demonstrates that not only 10 nm lines but also 10 nm spaces can be achieved using a modified SEM operated at 35 kV with liftoff techniques.

To use the modified SEM to achieve high overlay accuracy, we selected a writing field size of 12×9.3 μm^2, corresponding to a SEM magnification of 10 K. The writ-

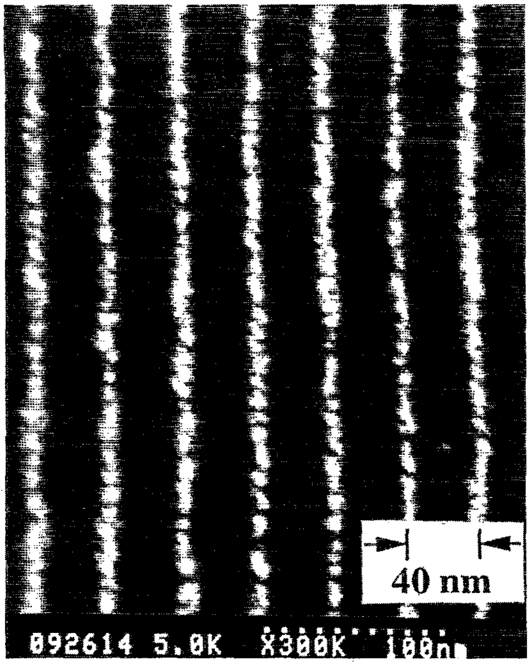

FIG. 1. Scanning electron micrograph of a 40 nm period Ni/Au grating with 10 nm linewidth on bulk GaAs.

ing field is further divided into (a) the "device" area of $9\times 9.3\ \mu m^2$ located in the middle of the field, and (b) two alignment areas of $1.5\times 9.3\ \mu m^2$ located on each side of the device area.

In the first level of the multilevel e-beam lithography, test patterns consisting of paired nanoscale metal squares with various separations were defined in the $9\times 9.3\ \mu m^2$

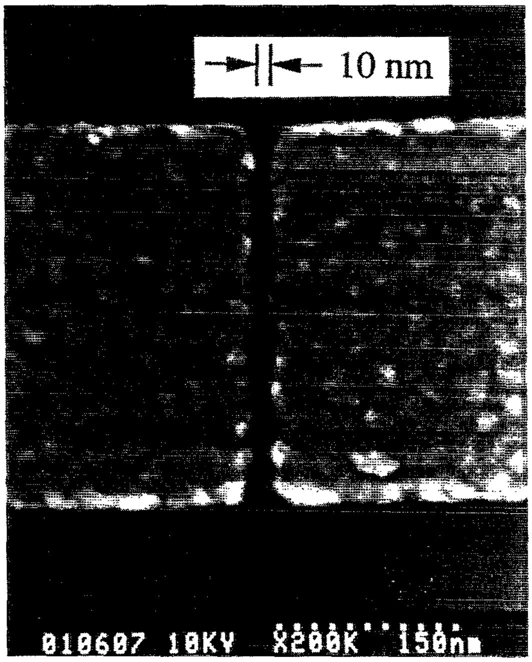

FIG. 2. Scanning electron micrograph of a Ni/Au constricted gate structure with a gap of 10 nm and a length of 330 nm on bulk GaAs.

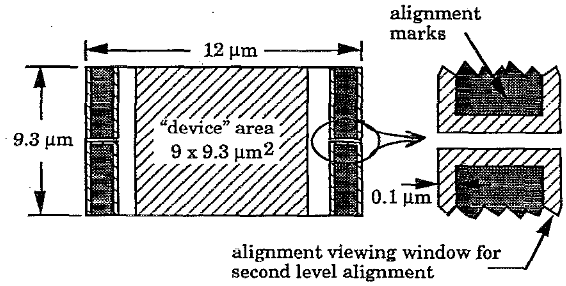

FIG. 3. Schematic of the alignment scheme.

device area by a liftoff process, and $4.5\times 0.5\ \mu m^2$ rectangular metal alignment marks for the second level e-beam lithography were defined in the alignment areas. The alignment marks consisted of 15 nm of Ni and 35 nm of Au and were sufficiently thick for "viewing" in the second level of alignment.

As illustrated in Fig. 3, in the second level of lithography, rectangular viewing windows were opened in the alignment area. The windows have a size which is just 0.1 μm larger than each edge of the alignment mark produced in the first level of the lithography. For perfect alignment each alignment mark from the first level should be centered in each viewing window. The alignment marks were detected using a backscattered electron detector. Coarse alignment was performed manually using the SEM stage movement micrometers; final alignment was achieved manually using electronic image shifts and electronic rotation

The device area was blanked during the alignment Even so, the resist in the device area is indirectly exposed by backscattered electrons from the alignment areas since the alignment windows are only 0.8 μm away from the device area. To minimize such proximity effects, the pixe resolution was reduced to $2^{10}\times 2^{10}$, to reduce the e-beam intensity while still maintaining sufficient resolution for the alignment. In such a way, the exposure dose in the alignment area during the whole alignment process was an order of magnitude lower than the minimum dose required to expose PMMA.

To check the overlay accuracy, paired metal lines o nanoscale linewidth were defined in the device area in the second level of lithography. With perfect alignment, one end of each metal line defined in the second level lithography should lay in the center of the squares placed by the first level. Figure 4 is a scanning electron micrograph showing typical results. The four unintended dots were due to a software error in the second level of lithography. Such errors have since been resolved. Figure 5 is the summary o 19 alignment tests, indicating that the standard deviation of the overlay accuracy is 17 nm. Both x and y results have been superimposed on the same plot due to the limited number of data points. The results show that high overlay accuracy can be achieved with a modified SEM.

In conclusion, a modified SEM has been used to fabricate ultrasmall features and achieve ultrahigh overlay accuracy, thus demonstrating the effectiveness of modified SEMs in cutting-edge nanoscale device research. By using

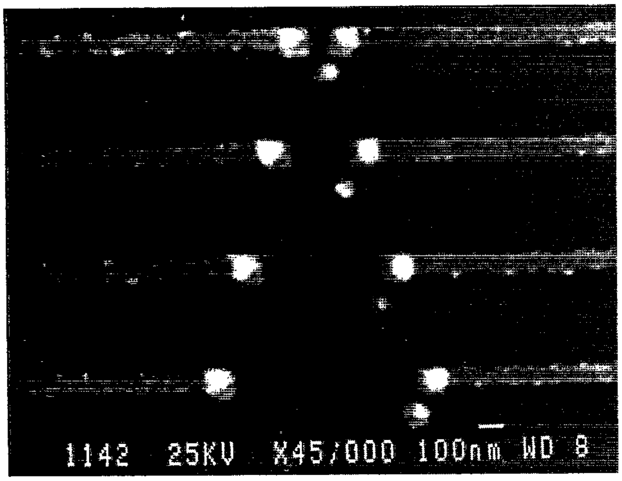

FIG. 4. Scanning electron micrograph of two e-beam lithography levels with 20 nm accuracy.

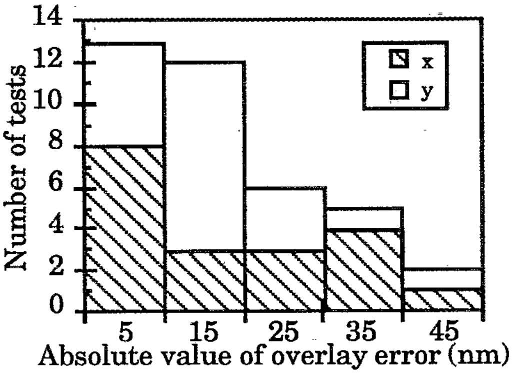

FIG. 5. Histogram showing the overlay accuracy in the *x* and *y* directions vs the number of tests. The standard deviation is 17 nm.

thin resists and minimizing exposure areas, gratings of 10 nm wide lines 30 nm apart, and quantum field-effect transistor gates with 10 nm wide gaps over 300 nm long have been repeatedly defined on bulk GaAs substrates using a modified SEM operated at 35 keV, and liftoff of Ni/Au. Sub-50 nm overlay accuracy in multilevel e-beam lithography has also been achieved using the same modified SEM.

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