10GHz SiGe design for phase and amplitude management of signal

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Abstract: - This paper presents a core chip design in SiGe Heterojunction Bipolar Transistor base for X-band phased array Transmit/Receive (T/R) module. Usually phase shifters for X-band application were done by using of GaAs technique. Some commercial GaAs products for this type of integrate circuits are considered. The structure of the Core Chip for Phased Array T/R Modules is presented. Methods for the formation of a phase delay for X-band phase shifters are considered. An original differential design of SiGe core chip for X-band is presented. The advantages of SiGe technique is observed. The schematic of 5 bits phase shifter and attenuator are designed. It consist of a series number LPF and HPF filters. Gain of phase shifter is 1.5 dB. Attenuator has the adjustment range from 0 to 24dB. Linear output power of the core chip is 5dBm. The total consumed current of the device is 158mA, at 5V power supply.

Key-Words: - Core Chip, Phased Array, T/R Module, SiGe, Heterojunction Bipolar Transistor

1 Introduction

Improving the efficiency of microwave radio and radar equipment is associated with integration increasing, mass-dimensional characteristics improving, reliability increasing due to the reduction of wire bonding between the chips, repeatability of parameters improving; unification of the transceiver equipment increasing, radiation resistance increasing due to the use of wide-bandgap semiconductors of the A_3B_5 group, increasing resistance to electromagnetic radiation by reducing the length of the connections. Regarding of that, the transceiver module parameters improving, of which core-chip is an integral part, is an important task.

The block diagram of the core-chip is shown in Fig. 1.

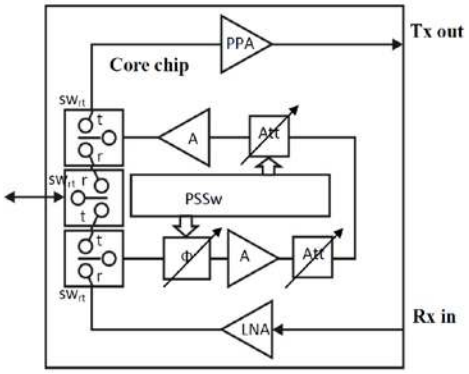


Fig. 1. Core chip block diagram

It contains of three ports switch (sw_{rt}), an attenuator, a phase shifter (Φ), signal amplifiers (A), a low-noise amplifier (LNA), a power preamplifier (PPA) and a switching device (PSSw), based on parallel or series to parallel interface.

Three-port switches (SPDT) for receiving/transmitting can be realized as solid-state electronic or micromechanical switches, made by using of integrated technology.

Phase shifters are a set of, usually, sequentially connected elementary cells. Elementary phase-shift cells can be performed in the next configurations: delay lines (for example microstrip lines, figure2a), combinations of high pass (HPF) and low pass (LPF filters (figure2b), differently loaded transmission lines (figure2c), use of vector summing of mutually orthogonal I and Q signals (Figure 2d), which can vary in amplitude.

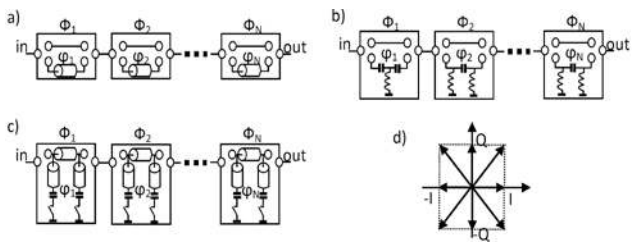


Fig. 2. Methods for forming phase delay

As a disadvantage of sequential connected elementary phase shifters is the influence of the impedance of the previous stage on the subsequent stage, which leads to a weakening of the transmitted signal, as well as to an additional phase shift.

Schematics of attenuators are also a series connection of elementary attenuators. It is most appropriate to use resistive dividers as signal attenuators.

At present, there are a large number of industrially mastered solid-state core-chips containing phase shifters and attenuators manufactured by such companies as OMMIC [1], MACCOM [10] (USA), UMS (France) [2], SELEX Sistemi Integrati SpA (Italy) [4], METDA (China) [8] based on A_3B_5 semiconductor (Table 1). There are a number of works in which silicon technology based on nanoscale CMOS [6,10] or hetero junction bipolar transistors (HBT) [4, 5] are used (Table 2). It should be noted the merits of using silicon technology based on SiGe bipolar transistors, which have a high cut-off frequency [11] up to 300 GHz. This allows you to receive devices operating in the X and Ku frequency bands.

Table 1. Core chip parameters based on GaAs

Parameters	[3], [6] RFcore	[4]	[5]	[7] Peregreen
Technology	CMOS	SiGe	SiGe	CMOS
Operation frequency (GHz)	9-10	8-11	8-11	8-12
Phase shift range/step (°)	360/5.6	360/11.2	360/11.2	360/5.6
Attenuation range/step (dB)	31/1	31/1	31/1	31.5/0.5
Tx/Rx gain (dB)	12/9[a"]	17/17	30/20	-
RMS phase error (°)	2.3	6	6	8
RMS attenuation error (dB)	0.4	2	1.5	0.25
Output P1dB in TX mode	11	12	18	-
Power Supply,V	2.4.	0.8	1.5	3.3;-3.3
Chip Size (mm^2)	6.9 x 1.6	3.8 x 4.1	3.5 x 2.4	4.6x2.6

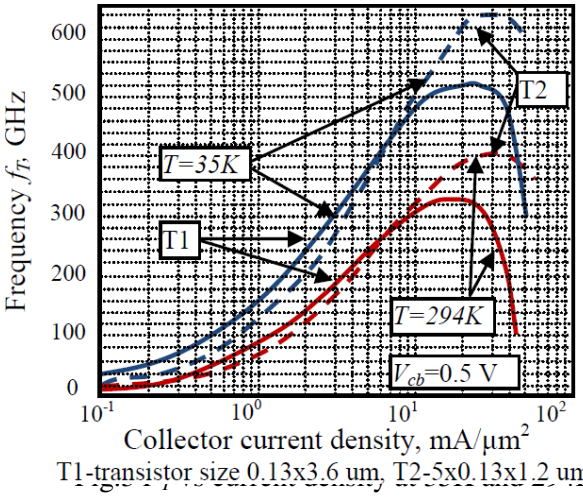
Table 2. Core chip parameters based on Si

Parameters	Ommic[1] GaAs	UMS[2] GaAs	Metda[8] GaAs	Micran[9] GaAs
Frequency (GHz)	8…12	8…12	8…12	8-11.5
Tx/Rx gain (dB)	8/8	23.5/12.5	11/10	15.5/16.5
Phase shift range, °	0…360	0…360	0…360	0…360
Phase step, °	5,625	5,625	5,625	5,625
Attenuation range, dB	24	34,65	48	27.9
Attenuation step, dB	-	0,55дб	0.75	0.5
TX OP1dB, dBm	11.1	13	12	20
RX OP1dB, dBm	8.5	16,5	10	16
RX noise figure, dB	7	5,8	8	5.2
Power Supply,V	-6, +6		-5, +5	-5, +5
Chip Size (mm^2)			5.06x3.8	4.0x5.1

The rest of this paper is organized as follows. SiGe components advantages are described in section 2. Core chip SiGe HBT design and simulation results are discussed in section 3. Conclusions are discussed in section 4.

2 Advantages of Sige Components

The main advantage of HBT is an extremely high speed (Fig.3, Fig.4). The high cut-off frequency f_T for industrial development of the transistor under normal conditions and at cryogenic temperatures reaches 300 GHz and 500 GHz, respectively [12]. This is achieved by the built-in electric field in the crystal lattice after introdusing of Ge, the short transient time throw the base area and the small time constant of the base-emitter junction charge.



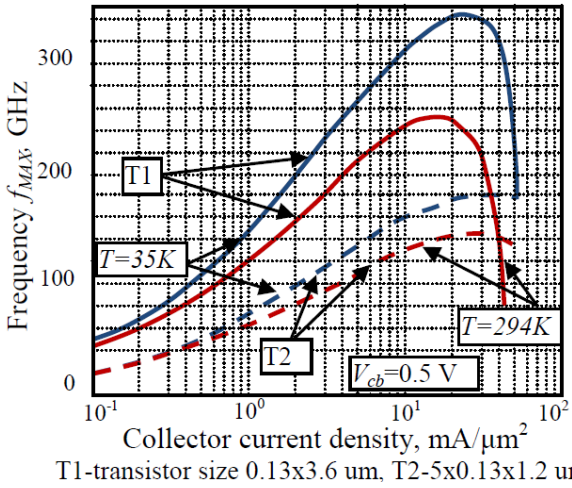


Fig.4 F_{MAX} vs current density at 35K and 294K

The gain in time performance compared to a regular silicon bipolar junction transistors (equation

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2(\overline{D}_{n,b})_{Si}}{(\overline{D}_{n,b})_{SiGe}} \frac{kT}{\Delta E_{g,Ge}} \left(1 - \frac{kT}{\Delta E_{g,Ge}} \left[1 - \exp(-\Delta E_{g,Ge}/kT)\right]\right) = 0,5...1$$

2.1) only due to the difference in width of bandgap (ΔE_g) is more than two times [13].

(2.1)

где $\overline{D}_{n,b}$- the diffusion coefficient of carriers in the base, $\Delta E_{g,Ge}$ - the difference in width of bandgap due to *Ge* introdusing, $kT = 4{,}11\ 10^{-21}$ - thermodinamic constant, τ_b -. charge carrier transient time throw the base area.

At the same time with high speed performance a high gain (β_{SiGe}) can be achieved due to the difference in width of emitter bandgap and base bandgap. The advantage in the gain compared to regular integrated bipolar transistor (equation 2.2) can range from 3 to 10 times [13].

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \frac{(\overline{D_{nb}})_{SiGe}}{(\overline{D_{nb}})_{Si}} \frac{(N_C N_V)_{SiGe}}{(N_C N_V)_{Si}} \frac{(\Delta E_{g,Ge}/kT) e^{-\Delta E(0)_{g,Ge}/kT}}{(1 - e^{-\Delta E_{g,Ge}/kT})} = 3...10 \quad (2.2)$$

It should be noted that hetero junction bipolar transistors operate at high current densities than regular integrated bipolar junction transistors with thin base. The problem of the high collector current density is solved by choosing its optimal values not exceeding the peak one, the using of constructive and technological solutions that optimally distribute the currents and to prevent the destruction of the HBT.

A significant advantage of hetero junction bipolar transistors is the high value of Early voltage in the operational range of collector voltages. High impurity concentration in the base ($N_{Ge}=8\cdot10^{19}cm^{-3}$) leads to the fact that the main part of the space charge are located in the collector and the emitter junction area of the transitions, and thus the thickness of the base will be weakly dependent on collector-base voltage and base-emitter voltage. In this case, the Early voltage (V_A) of the transistors can reach up to 100 volts, which is 2-4 times more than regular silicon integrated transistor [13] (equation (2.3)). The consequence of high Early voltage tension is the possibility of gain increasing, while maintaining a high punch off voltage of the base.

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{Vbe} = \exp(\Delta E_{g,Ge}/kT) \frac{1 - \exp(-\Delta E_{g,Ge}/kT)}{\Delta E_{g,Ge}/kT} = 2...4 \quad (2.3)$$

The price that has to be paid for high speed and high gain is lower than the usual integral transistors, the collector-emitter breakdown voltages and the base-emitter breakdown voltages are respectively 3.5V and 1.3V (foundry dependent), which is the result of high electric field strength in thin base.

Thus, a heterojunction bipolar transistor with a base of germanium doping, compatible with the CMOS technology, is a suitable active component for the microwave system. Using HBT transistors will expand the frequency range of devices for controlling the amplitude and phase of signals for RF block and modules till several tens of gigahertz.

3 Sige Core Chip Design

The aim is to investigate the possibilities for designing a control chip (core chip) for X-frequency band using SiGe BiCMOS technology.

The chip should include the following blocks: attenuator, phase shifter, receive/transmit switches, compensating amplifiers, control circuit with parallel interface with TTL levels. Given the high high cut-off frequency of heterojunction bipolar transistors, it is advisable to design the crystal by using of SiGe BiCMOS technology [11]. Differential current switches with a stabilized reference voltage were selected for base schematic high-frequency data signal processing units.

With this approach, the implementation of switches and amplifiers with the required parameters at frequencies up to 11 GHz has not technical difficulties, with the exception of output drivers, which have fundamental limitations in signal amplitude. The most critical are two blocks: a phase shifter and an attenuator. To demonstrate the capabilities of the technology, a four-phase phase shifter with HBT as active components was analyzed. The proposed schematic of the device is shown in Figure 5.

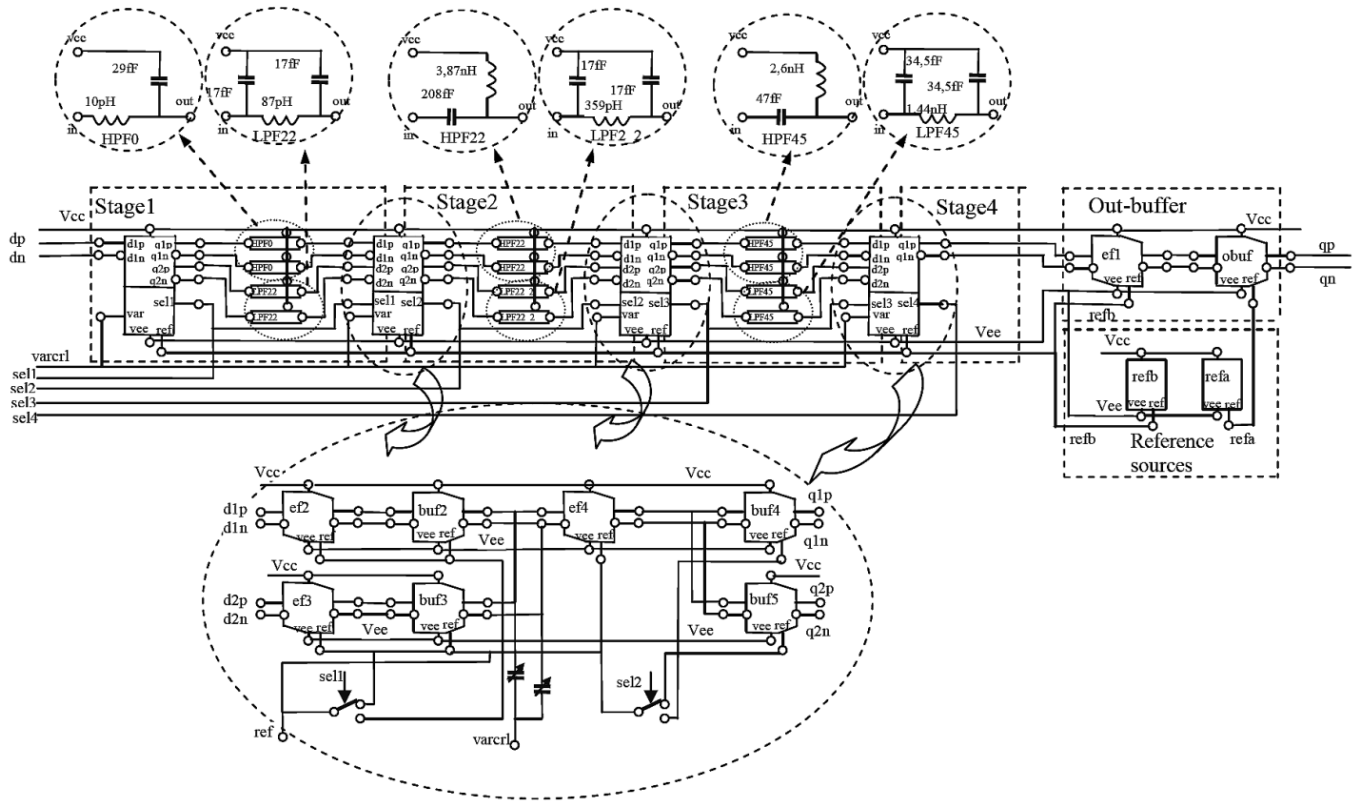


Fig. 5 Phase shifter schematic

The phase shifter contains three stages SPDT (SPDT - Single Pole, Double Throw) amplifying switches (Stage 1, 2, 3) with LC filters, providing a relative phase shift from 0 ° to 180 ° in 22.25 ° increments. The fourth stage (Stage4) is a switchable inverter. The subsequent output amplifier consists of a preamplifier and an output driver (Out buffer), both of which contain linear differential cascades.
The reference system uses stabilized reference voltage sources and special CMOS switches.

SPDT switch is a two-stage linear amplifier with a current consumption of 15.4 mA, the second stage of which performs the function of an analog demultiplexer 1:2. One of the outputs of the multiplexer is activated by the digital signal sel2, which ON/OFF the reference voltages by CMOS switch (sw2rfb25m_2v5). The principal feature of this circuit is the possibility of smooth phase adjustment within 2 ° by changing the analog voltage (varcrl) on varactors.

Two pairs of phase-shift filters are connected to the outputs of the first amplifying switch. In this schematic, the HPF0 cells are equivalent transmission line, and the LPF22a cells are LC low-pass filters.

The second and third amplifying switches (selector2to2_14m3) are identical to each other, consume 14.3 mA of current and perform the function of 2:2. Like the first switch, these have a smooth phase adjustment by changing the voltage (pin varcrl).

The inputs of the second switch are connected to the outputs of the two channels of the first switch, and its outputs are loaded on pairs of filters HPF22 and LPF22b. Similarly, the inputs of the third key are connected to the outputs of the two channels of the second switch, and its outputs are loaded onto the HPF45 and LPF45 filter pairs.

The fourth amplification switch (selector2to1_14m3), consumes 14.3 mA of current and performs the function of an analog multiplexer 2:1 with an activated or disabled inversion of the output signal.
The developed phase shifter was simulated using the Cadence system under various operating conditions in the frequency range from 9.1 GHz to 10.3 GHz. Absolute and relative phase shifts in the first three stages of the phase shifter at a frequency of 10 GHz and at two limiting temperatures of 0 ° C and + 125 °C are given in Table 3.

Table 3. Phase shift in amplification switches

Phase shift, degree	**Stage 1**		**Stage 2**		**Stage 3**	
	0°*C*	125°*C*	0°*C*	125°*C*	0°*C*	125°*C*
(HPF)	40.8	48.9	15.5	24.2	5.4	4.0
(LPF)	63.2	71.3	59.3	67.8	85.5	94.2
Difference	22.4	22.4	43.8	43.6	90.9	90.2

The presented data demonstrate the acceptable stability of all stages. Additional phase adjustments can be made using a varcrl test voltage, which provides an additional adjustment range of about 8 °. The relative phase shift in steps at 125 ° C (worst case) in the frequency range from 10.0 GHz to 10.3 GHz is shown in Figure 4a. The accuracy of the phase setting is not worse than ± 0.7 °. The relative phase shift in steps at 125 ° C (worst case) in the frequency range from 8.0 GHz to 12 GHz is shown in Figure 6b.

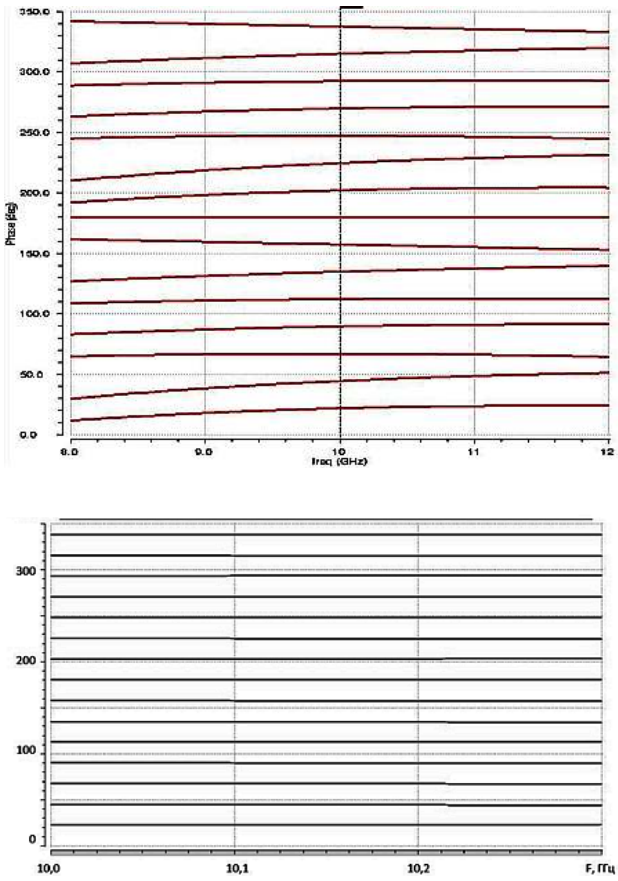


Fig. 6. The relative phase shift in steps a)- range 8-12GHz, b)- range 10-10.3 GHz

The output stage in this circuit provides a linear power of 1 dBm. In this case, four stages of the phase shifter consume a current of about 58 mA, and full circuit is about 123 mA. It is possible to increase the output power by a factor of 2 (to +4 dBm) by increasing the current consumption.

The phase shifter is the most significant block in the area of the core chip. The main area in the layout of the phase shifter is occupied by inductors, capacitors and varactors. The area of the block is 1,0x1,0 mm^2.

The main task of designing a controlled attenuator is to maintain the linearity of the input buffer at substantially different amplitudes of the input signal. For this, it is necessary to attenuate the signal before feeding it to the first amplification stage. This problem is solved by using a resistive ladder R-2R. The diagram of such ladder is shown in Figure 7. It is easy to calculate that the equivalent resistance of the ladder at node d1 is 50 Ohm. At the same time, the signal at the node d2 is divided by 2 times, at the node d3 - 4 times and at the node d4 - 8 times. Combining signals from all four nodes, you can get a total signal with a transmission factor from + 5.5 dB to - 18 dB, which corresponds to the adjustment range from 0 to 23.5dB.

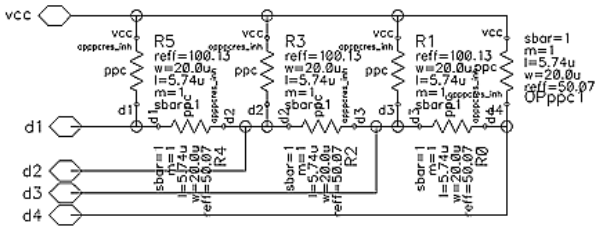


Fig. 7 The schematic of the resistive ladder R-2R

It should be noted that such system provides a binary adjustment of the attenuation, which allows simplify circuit implementation with a lower power consumption. The logarithmic adjustment system requires a much more complex circuit that contains a decoder and one or two switches per attenuator state, which contains up to 30 switches for a 4-bits. In this regard, a schematic of 4-bit binary controlled attenuator was implemented. The schematic is shown in Figure 8.

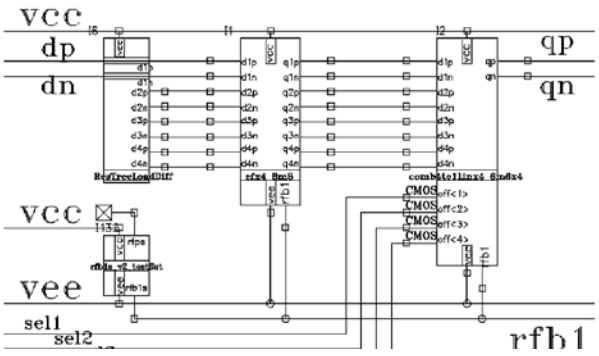


Fig. 8. Block diagram of attenuator with amplitude control

It contains a double input resistive ladder (ResTreeLoadDiff), four double emitter followers (efx4_8m8) and a 4-bit linear differential mixer-selector (comb4to1Linx4_6m6x4). Schematics of the emitter follower and mixer-selector are shown in Figures 9 and Figures 10 respectively.

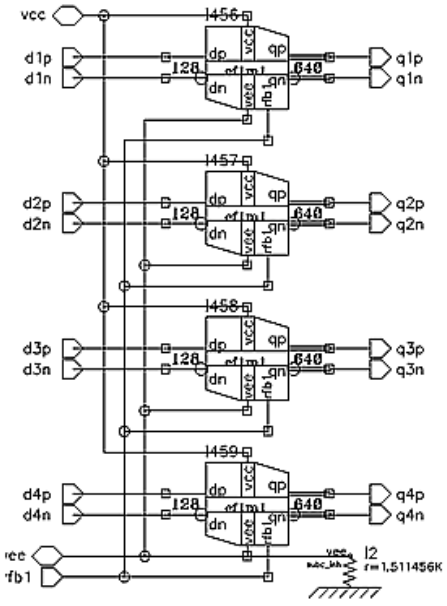


Fig. 9. Block diagram of emitter followers

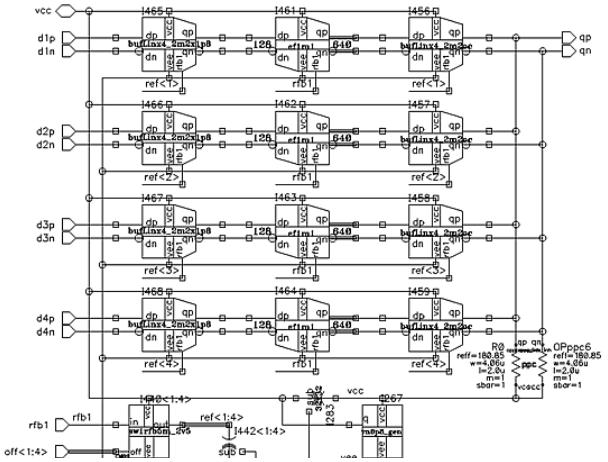


Fig. 10. Schematic of the mixer-selector

The developed attenuator was simulated by using the Cadence system under various operating conditions in the frequency range from 0 to 12 GHz. The attenuation drop by 3 dB occurs at a frequency of 11.8 GHz with a current consumption of about 35 mA.

The adjustment modes were checked by sequentially switching the binary signals sel1, sel2, sel3 and sel4 as shown in Figure 11.

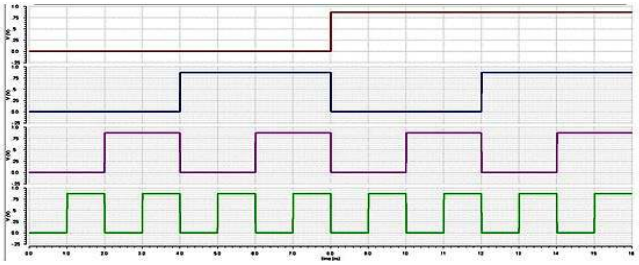


Fig. 11. Control bits at the attenuator input

The resulting differential output signal for the case of a constant amplitude of the input signal at a frequency of 10 GHz is shown in Figure 12.

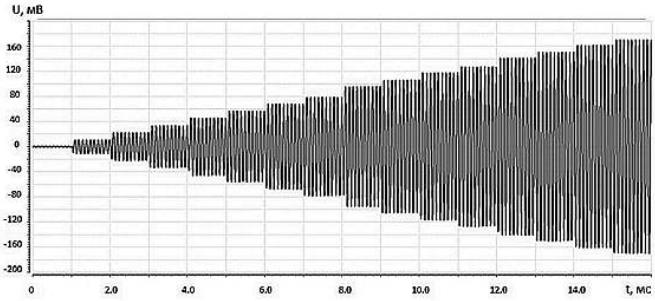


Fig.12. Attenuator output signal

The linearity of the attenuator was determined from the attenuation of the second and third harmonics with respect to the magnitude of the signal at the fundamental frequency with three values of the amplitude of the input signal. The attenuation of second harmonic is -50 dBc and third harmonic is -45 dBc**.**

4 Conclusion

The estimated design of the core chip, by using of SiGe technological process, satisfying the different requirements for transmitting and radar equipments.

Phase shifter provides a phase shift from 0-360 degrees, phase discrete is not worse than 11 degrees, which corresponds to 5 bits of control(at the 9.1 to 10.3 GHz). A phase shifter without a fourth stage and an output amplifier provides a gain of 1.5 dB (at 125 °C). In this case, four stages of the phase shifter consume a current of about 58 mA, and the complete circuit is about 123 mA.

The output stage of the phase shifter provides a differential linear power of about -1 dBm. It is possible to increase the output power by about 2 times (up to + 5 dBm) due to the increase in the current consumption;

The bandwidth of the attenuator (at 3dB level) is 11.8 GHz in the worst case (at 125 °C) with a current consumption of about 35 mA.

The attenuator gain is from + 5.5 dB to -18 dB, which corresponds to the adjustment range about from 0 to 24dB.

The total consumed current of the device is 158mA, (at 5 V power supply) does not exceed 1 W.

The using of different technologies bases (GaAs, GaN, SiGe), allow the implement of a transceiver module with optimal characteristics for any radar or transmitting system.

The future work in this area will contain chip implementation and its introducing in T/R module.

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