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11.2% - efficient solution processed kesterite solar cell with a low voltage deficit

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On the way towards a marketable and industrially-relevant photovoltaic technology, kesterite – $\text{Cu}_2\text{ZnSn}(\text{S},\text{Se})_4$ (CZTSSe) – based thin film solar cells have to overcome several bottlenecks that currently limit their conversion efficiency. As of today, most of the synthesis routes for the CZTSSe absorbers have yielded solar cells with close to or above 10% power conversion efficiency. The current record of 12.6% has been obtained with a solution approach using hydrazine as the solvent,^[1] thermal co-evaporation of CZTSe yielded 11.6%,^[2] whereas devices fabricated by the selenization of sputtered metal precursors resulted in 10.4% efficiency.^[3] A comparison with the related chalcogenide $\text{Cu}(\text{In},\text{Ga})\text{Se}_2$ (CIGS) technology reveals several deficiencies in CZTSSe solar cell parameters, while current research efforts are focused on the identification of bottlenecks that are limiting further improvements. Major limitations are the high open circuit voltage deficit (V_{oc} -deficit) defined as the difference between the measured open circuit voltage and the absorber bandgap, and a comparably low fill factor (FF). Several possible explanations for the V_{oc} -deficit have been proposed. Secondary phases such as binary and ternary copper-, zinc- and tin selenides and sulfides can exist in the absorber or its interfaces, which impede the carrier transport and lead to an increased recombination rate.^[4] Prevention of the formation of secondary phases in kesterite layers is challenging due to the small phase stable region for the formation of the

quaternary CZTSSe compound.^[5] Losses in V_{oc} can also be caused by recombination at the absorber interfaces due to a high density of surface states as well as cliff-like conduction band offsets.^[6] The lack of shallow defect states in CZTSSe is also expected to lower mobility, lifetime and therefore decrease the V_{oc} .^[7] Finally, bandgap fluctuations stemming from structural or compositional inhomogeneities, or potential fluctuations due to a high concentration of charged defects can also lead to lower V_{oc} .^[8]

In this investigation CZTSSe absorbers are prepared from precursors obtained from a solution approach with dimethyl sulfoxide (DMSO) as the solvent with subsequent re-crystallization by annealing under controlled atmosphere of selenium. The DMSO approach,^[9] a safer and low-toxic alternative to the hydrazine route, requires only readily available metal salts and has yielded 10.3%-efficient solar cells with a V_{oc} -deficit of 0.60 V^[10] or recently, even up to 11.8% measured on active area.^[11] Some commonly reported problems of the DMSO-processed kesterite layers are their high porosity, non-uniformity, and numerous grain boundaries that can lead to undesirable recombination.^[12] Here we employ a 3-stage annealing process under controlled selenium atmosphere in a SiO_x coated graphite box to drastically improve the grain size and morphology of the absorber layer. Importantly, the V_{oc} -deficit can be reduced to 0.57 V, which appears to be one of the lowest value reported for any kesterite devices. Systematic electrical characterization of absorbers and finished solar cells with time resolved photoluminescence (TRPL), temperature-dependent current-voltage measurements ($JV-T$), and admittance spectroscopy (AS) are used to identify the reasons of the improved voltage.

Figure 1 shows the scanning electron microscopy (SEM) cross-sections of four different CZTSSe absorbers A – D yielding efficiencies from 6.6% to 10.1% (total cell area of 0.3 cm² including metal grid lines). The annealing conditions are varied from uncoated graphite box

(A, B) to SiO_x-coated graphite box (C, D) and 2-stage temperature gradient (A, C) to 3-stage temperature gradient (B, D); temperature gradients are presented in **Figure S1** in *Supporting Information*. The selenization of sample A was conducted in an uncoated graphite box employing a 2-stage temperature gradient, and the absorber layer exhibits a distinct bi-layer structure with a thick small-grain bottom layer.^[13] Sample B was selenized in an uncoated graphite box similar to A but employing a 3-stage temperature gradient. The SEM cross-section shows an improved crystallization and grain size in both upper crust and bottom layer. However the distinct bi-layer structure of the absorber layer remains. The selenization of sample C was conducted in a SiO_x-coated graphite box using the 2-stage process, and the morphology of the film exhibits a comparably thin upper layer with small grains, but an improved crystallization in the bottom layer in contrast to sample A. Finally sample D was selenized in the SiO_x-coated graphite box with the 3-stage temperature gradient and shows an overall improved crystallization with large grains and a significant reduction of the small-grain bottom layer. X-ray diffraction (XRD) pattern in **Figure 2 b)** shows a double kesterite reflex at 53.4° for all samples, indicating two regions with different S/(S+Se)-ratio in the absorber layer. Grazing incidence XRD with varying incident angles confirms that the region with lower S/(S+Se) ratio coincides with the upper crust and the region with higher S/(S+Se) ratio belongs to the small-grain bottom layer. The reflexes corresponding to the higher S/(S+Se) ratio extenuate with the shift from uncoated to SiO_x-coated graphite box as well as with the change of the temperature gradient from 2-stage to 3-stage process.

No secondary phases can be identified from the XRD patterns of the four samples in Figure 2 a), although the presence of Zn(S,Se) and Cu₂Sn(S,Se)₃ impurity phases cannot be excluded since their reflexes coincide with those of CZTSSe and therefore, cannot be distinguished by XRD.^[14] Reflexes at 14.7°, 17.4° and 22.1° confirm unambiguously the CZTSSe phase. For all samples additional reflexes appear at 31.6° and 56.5°, indicating the Mo(S,Se)₂ layer^[15]

whose thickness depends on annealing conditions. Both changes in graphite box and temperature gradient increase the $\text{Mo}(\text{S},\text{Se})_2$ layer thickness.

The temperature gradient during the annealing step of the 2-stage process features a lower holding temperature at 300°C which is intended to outgas remaining residues of the organic solvent before the dense top crust on the absorber layer starts to form. Additionally, Na_2Se_x phases with low melting points can form, which act as fluxing agents and improve the grain growth.^[16] The higher holding temperature at 500°C facilitates the crystallization, grain growth and selenium incorporation. The selenium vapor pressure during the annealing equals the saturated vapor pressure for the given temperatures, that is 0.3 mbar and 55 mbar at 300°C and 500°C , respectively.^[17] The grain growth at 500°C leading to the bi-layer structure can be split into an abnormal grain growth of the large-grained upper layer and a normal grain growth for the small-grained bottom layer.^[18] The abnormal grain growth is driven by the surface area and total energy difference, and it is also facilitated by volatile Zn-, Sn- and Se-containing species from the gas phase. The third holding temperature at 550°C exclusively at the end of the 3-stage process accounts for increased grain growth, however at this stage no additional selenium is left in the graphite box and the grain growth is presumably governed by redistribution of grain boundaries. The intention behind the SiO_x -coating is to significantly reduce porosity of the graphite box, thus enabling a higher selenium pressure during annealing, which improves crystallization especially in the bottom layer of the absorber. It should be noted, however, that higher temperatures and/or longer annealing times promotes the formation of thicker $\text{Mo}(\text{S},\text{Se})_2$ layers, that at some point can and cause delamination decrease device performance.

The change in metal ratios due to the high temperature annealing is proportional to the annealing time and corresponding temperature. The loss of Sn and Zn is more pronounced for the 3-stage process compared to the 2-stage process, due to the formation of volatile phases of both constituents.^[19] Surprisingly, the change from uncoated to coated graphite box did not

affect the final metal ratios. As a result, metal ratios of samples A, C and B, D are quite close, $\text{Cu}/(\text{Zn}+\text{Sn}) = 0.90 \pm 0.03$ and $\text{Zn}/\text{Sn} = 1.27 \pm 0.04$, which are in the compositional range typically yielding the high efficiencies.^[20] In this off-stoichiometric range, so-called B-type, the presence of defect complexes $[2\text{Zn}^{2+}_{\text{Cu}} + \text{Zn}^{2+}_{\text{Sn}}]$ with a formation energy of 0.86 eV is expected.^[21]

Figure 3 a) shows the J - V characteristics of devices A – D and their basic photovoltaic properties. Changing the reactor from uncoated to SiO_x -coated graphite box leads to a higher FF , whereas the change from the 2-stage to the 3-stage temperature gradient during selenization improves FF , J_{sc} and significantly decreases the V_{oc} -deficit.

In Figure 3 b) the external quantum efficiency (EQE) shows the spectral composition of the J_{sc} together with band gap values E_g extracted from the inflection point of the EQE spectrum in the long-wavelength range. Integration of EQE spectra yields photocurrent of 31.6, 32.8, 28.2 and 35.4 mAcm^{-2} for samples A – D, respectively, which are in good agreement with J_{sc} values obtained from J - V -measurements. The extracted bandgaps are similar to bandgaps estimated from XRD measurements assuming 1.0 and 1.5 eV for CZTSe and CZTS respectively.

Figure 4 shows the TRPL decay curves and the PL spectra both acquired at room temperature of the devices A – D. The TRPL decay curves indicate an increased radiative lifetime for the samples annealed with the 3-stage process. In comparison with the SEM cross-sections the radiative lifetime correlates with the thickness of the large-grain upper layer of the absorber. The TRPL results are in good agreement with the long-wavelength characteristics of the corresponding EQE spectra, so that a lower EQE is observed for the samples with a faster TRPL intensity decay. The PL spectra exhibit a broad peak for all samples, and the peak maxima are red-shifted as compared to the bandgap by 0.11 eV, 0.02 eV, 0.06 eV and 0.02 eV

for samples A, B, C and D, respectively. In literature, PL maxima red shifts of 110 meV are reported for solution-based methods, whereas vacuum methods can yield values as low as 10-20 meV.^[2,3,22] The rather broad shape in our case indicates the presence of tail states and/or potential fluctuations,^[8] which are responsible for the increased lifetime by several orders when performing low-temperature TR-PL measurements (not shown here). The decrease in red shift of the PL maxima in respect to the bandgap values of samples A, C to B and D suggests a reduction in tail states.

Figure 5 shows the properties of the champion device D_2, which was fabricated with an identical process as sample D but in another batch. The SEM cross-section image exhibits a similar structure as sample D with a large-grain upper crust, a rather narrow small-grain bottom layer and a distinct MoSe₂-layer. The *JV-T* curve yields a total-area efficiency of 11.2%, whereas 10 best cells had an average efficiency of $10.6 \pm 0.3\%$. The EQE measurement shows that the major part of additional current is stemming from the long-wavelength region, which is in line with the long TRPL decay in Figure 5 d). The decay curve is fitted with a single exponential function in the range 10 – 100 ns since the faster decay during first 10 ns originates from the charge separation in the device.^[22] The fitted long minority carrier lifetime of $\tau_2 = 8.1$ ns is responsible for the improved collection in the long-wavelength region, which is manifested by plotting the ratio of reversed bias EQE and zero bias EQE.

Further advanced characterization on sample D_2 was conducted using AS and *JV-T* measurements. **Figure 6** a) shows the *JV-T* curves in darkness and under illumination. The crossover of illuminated and dark curves is becoming more pronounced at lower temperatures, whereas the increasing rollover of the *J-V*-curves leads to a complete blocking of the current at the lowest temperature of 123K. Possible explanations for this blocking is a barrier at the

interface between absorber and the Mo back contact, which facilitates the minority carrier recombination,^[23] or an increase in bulk resistivity, due to the lack of shallow acceptor states and therefore a freeze out of deeper acceptor states rendering the device fully depleted and exhibiting high resistivity.^[7]

The temperature dependence of the V_{oc} extrapolated to $T = 0K$ provides an intercept of $E_A (V_{oc}-T) = 0.99$ eV, representing the activation energy for the dominant recombination mechanism. Since this value is very close to the derived bandgap of 1.05 eV, one can conclude that the dominant recombination paths are located within the bulk of the absorber rather than at the interface.^[24]

In Figure 6 b) the temperature dependence of the dark series resistance R_s is shown. Using the model for a Schottky barrier at the back contact^[25] the barrier height can be calculated from equation (1)

$$R_S = R_0 + \frac{k}{qA^*T} e^{\frac{-E_A}{kT}} \quad (1)$$

where A^* is the effective Richardson constant, R_0 is the background series resistance and E_A the activation energy due to the barrier. The Arrhenius plot in the inset yields an activation energy of $E_A (R_s-T) = 182$ meV. AS measurements in **Figure 7** show one freeze out in the frequency range from 200 Hz to 2 MHz. Assuming a point defect, one can utilize equation (2) in order to extract the activation energy:

$$\omega_0 = 2\xi_0 T^2 e^{\frac{-E_A}{kT}} \quad (2)$$

with $\omega_0 = 2\pi f$ the freeze out frequency and ξ_0 the temperature independent thermal emission pre-factor. This results in a thermal emission depth $E_A (Cf-T) = 108$ meV with $\xi_0 = 4694$ s⁻¹K⁻².

However the freeze out observed in the AS measurement could also be attributed to a Schottky barrier in the device and a corresponding activation Energy is derived by a change in the temperature dependence of the pre-factor from T^2 to $T^{3/2}$, yielding an activation energy of $E_{A,B} (Cf-T) = 115$ meV.^[26] From the $Cf-T$ measurements the dark series resistance can also be

calculated by employing an admittance circuit model of a depletion region in series with the undepleted quasi-neutral region.^[7] Comparing these values with the R_s derived from JV - T (Figure S2) shows one order of magnitude lower values for R_s obtained from AS, implying that the activation energies $E_A(Cf-T)$ and $E_A(R_s-T)$ are not attributed to the same effect.

In **Table 1** the current champion devices having efficiency $> 10\%$ for non-vacuum and vacuum deposition techniques are displayed. The record efficiency of 12.6% is obtained with a pure-solution approach utilizing hydrazine as the solvent.^[1] The highest FF with 69.8% is also observed for this sample. DMSO-processed cells reach efficiencies 11.2% (this study), 11.8% (active area measurement)^[11] and 10.3%.^[10] Vacuum-based pure selenide absorbers can deliver the highest photocurrents J_{sc} of 40.6^[2] and 39.7 mA cm⁻²^[3] because of their low bandgaps. The 10.8% mini-module from Solar Frontier features the lowest V_{oc} -deficit of 0.56 V (determined from a linear fit of the transformed EQE curve).^[27] The 11.2% device of this study exhibits the highest minority carrier lifetime of $\tau = 8.1$ ns indicating a low concentration of defects in the absorber bulk and interfaces and the lowest ideality factor of $A = 1.14$ suggesting that the dominant recombination paths are shifting from the space charge region (SCR) to the quasi neutral region (QNR),^[23] which is consistent with the fact that the V_{oc} - T fit intersects at $T = 0K$ very close to the bandgap value.

In summary, an 11.2%-efficient (total cell area measurement) CZTSSe solar cell is fabricated using the hydrazine-free DMSO solution approach. The best device features the V_{oc} -deficit of only 0.57 V which is amongst the lowest for solution processed CZTSSe devices. The open circuit voltage improvement was possible because of the 3-stage annealing process in a silica-coated closed reactor, which enabled an increased incorporation of selenium and large-grained microstructure. The reduced V_{oc} -deficit is attributed to an increased minority carrier lifetime, low diode saturation current and ideality factor, which are signatures of the semiconductor material with a low concentration of recombination centers.

Experimental Section

The CZTSSe precursor solution consisted of thiourea (99%+, Sigma-Aldrich), $\text{SnCl}_2 \cdot 2\text{H}_2\text{O}$ (98%, Sigma-Aldrich), ZnCl_2 (99.99%, Alfa Aesar), CuCl_2 (98%+, Alfa Aesar) and NaCl (99.99%, Alfa Aesar), dissolved in DMSO (99.9%, Alfa Aesar). The precursor solution contained 0.15 M NaCl and the molar ratios were $\text{Cu}/\text{Zn} = 1.28$, $\text{Cu}/\text{Sn} = 1.36$, and $\text{Zn}/\text{Sn} = 1.07$. The precursor solution was spin-coated onto a Mo coated soda-lime glass and dried on a hotplate with 320°C in air. The spin-coating and drying steps were repeated several times in order to obtain the desired precursor film thickness of 1.5–2 μm . The precursor composition for all samples was $\text{Cu}/\text{Zn} = 1.48$, $\text{Cu}/\text{Sn} = 1.62$ and $\text{Zn}/\text{Sn} = 1.10$. Sample A and B were annealed in an Annealsys AS ONE 150 RTP furnace inside a closed graphite box with selenium pellets (800 mg) and sample C and D were annealed in the same furnace but inside a SiO_x -coated graphite box with the equal amount of Se. The temperature gradient employed for annealing sample A and C was the 2-stage process with holding at 300°C and 500°C whereas sample B and D were annealed with the 3-stage process with holding at 300°C , 500°C and 550°C . Metal ratios of the selenized absorbers were for sample A and C: $\text{Cu}/\text{Zn} = 1.57$, $\text{Cu}/\text{Sn} = 1.96$, $\text{Zn}/\text{Sn} = 1.25$, for sample B and D: $\text{Cu}/\text{Zn} = 1.62$, $\text{Cu}/\text{Sn} = 2.11$, $\text{Zn}/\text{Sn} = 1.30$ and for sample D_2: $\text{Cu}/\text{Zn} = 1.52$, $\text{Cu}/\text{Sn} = 1.92$, and $\text{Zn}/\text{Sn} = 1.26$. All metal ratios were obtained by X-ray fluorescence (XRF) measurements calibrated by inductively coupled plasma mass spectrometry (ICP-MS). The temperature-time profiles for all samples are given in supplementary information (Figure S1).

After selenization the absorbers were immersed for 30 s in a 10 wt% KCN solution in order to remove copper-rich phases and clean the surface from contaminations and oxides. A 50-70 nm thick CdS buffer layer was deposited by chemical bath deposition, and 70 nm/350 nm i-ZnO/Al:ZnO bilayer was sputtered. A Ni/Al top grid and an AR coating of MgF_2 were deposited by e-beam evaporation. Individual solar cells were mechanically scribed to an area

of $0.30 \pm 0.02 \text{ cm}^2$. Finally, post-annealing of complete devices at 120°C for 60 minutes in air was performed.

SEM measurements were done on a Hitachi S-4800 electron microscope, XRD patterns were recorded in $2\theta \setminus \theta$ scan mode using a Bruker D8 diffractometer with $\text{CuK}\alpha$ radiation ($\lambda = 1.5418 \text{ \AA}$, beam voltage: 40kV, beam current: 40 mA, calibrated using Si100 and Si111 single crystals), a step size of 0.04° and a scan rate of 0.5 s/step. The J - V characterization was performed under standard test conditions (100 mWcm^{-2} , 25°C , AM1.5G) using a solar simulator calibrated with a certified Si diode. The EQE spectra were recorded using a chopped white light source (900W halogen lamp) with a LOT MSH-300 monochromator, which was calibrated with certified Si and Ge diodes. The illuminated area on the sample was 0.1 cm^2 including grid lines. AS measurements were carried out with a LCR-meter from Agilent (E4990A) with an AC-voltage of 50 mV in the temperature range from 123K to 323K. Room temperature TRPL and PL spectra were measured on a FT300 fluorescence lifetime spectrometer from PicoQuant with a 639 nm pulsed diode laser as excitation source (pulse width 90 ps, repetition rate 10 MHz) and a thermoelectric cooled Hamamatsu NIR-PMT module H10330A-45 (rise time 0.9 ns, transit time spread 0.4 ns).

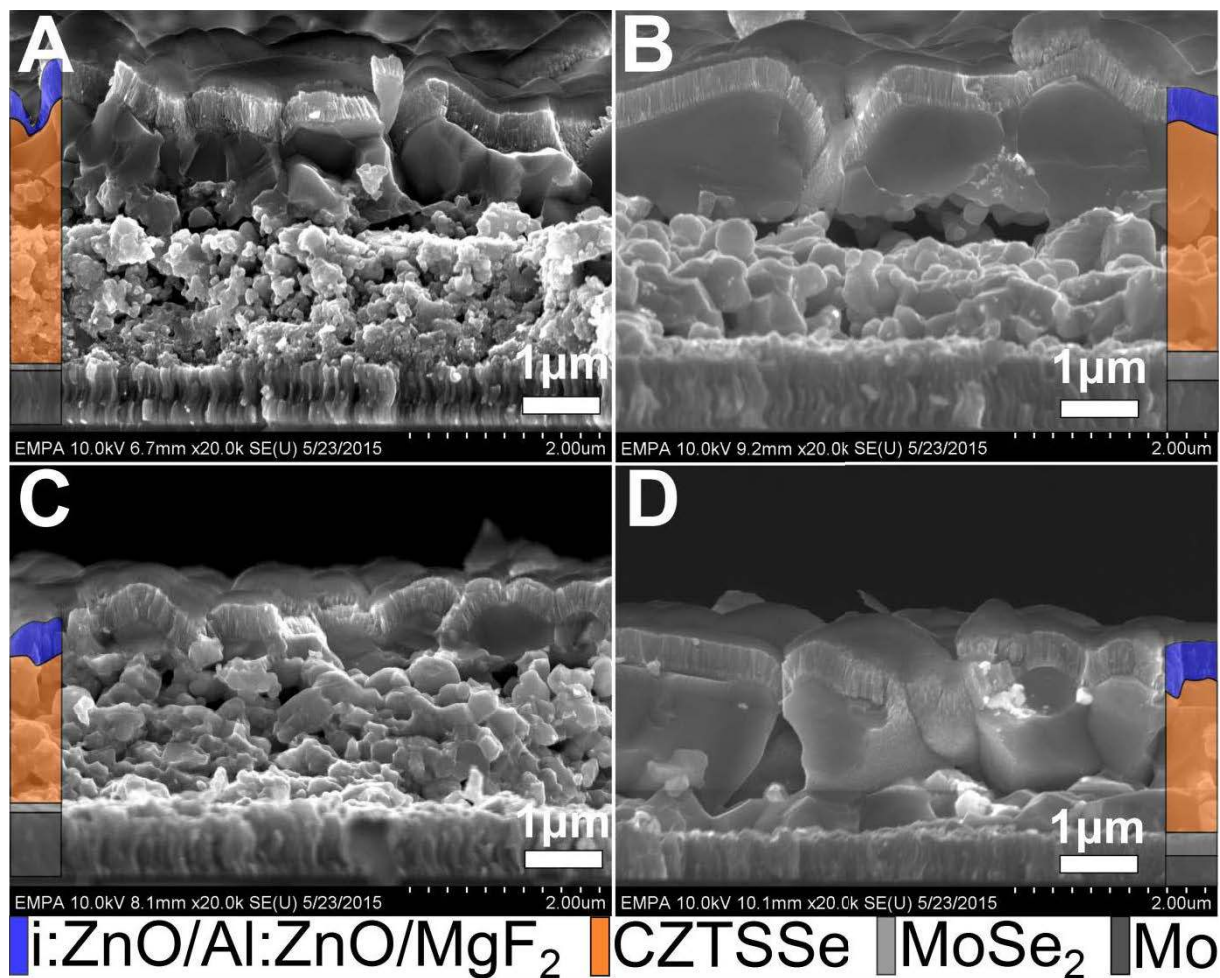


Figure 1. SEM cross-section image of samples A – D illustrating changes in the absorber morphology when switching the selenization process from the uncoated graphite box (A, B) to the SiO_x coated graphite box (C, D), and varying the temperature gradient from the 2-stage (A, C) to the optimized 3-stage process (B, D).

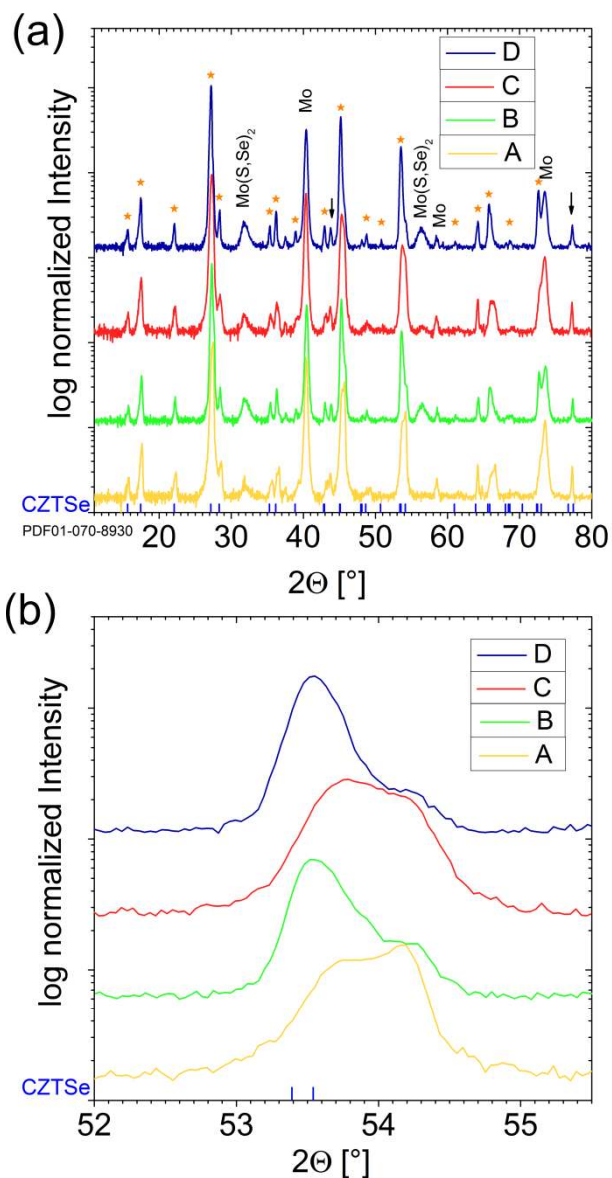


Figure 2. a) XRD pattern of samples A – D exhibiting reflexes of CZTSSe (marked with star *), Mo back contact, Mo(S,Se)₂, and the sample holder (marked with ↓). b) 312/116 reflex of the CZTSSe phase for samples A – D. The double peak alters depending on selenization conditions, indicating regions with different S/(S+Se) ratios.

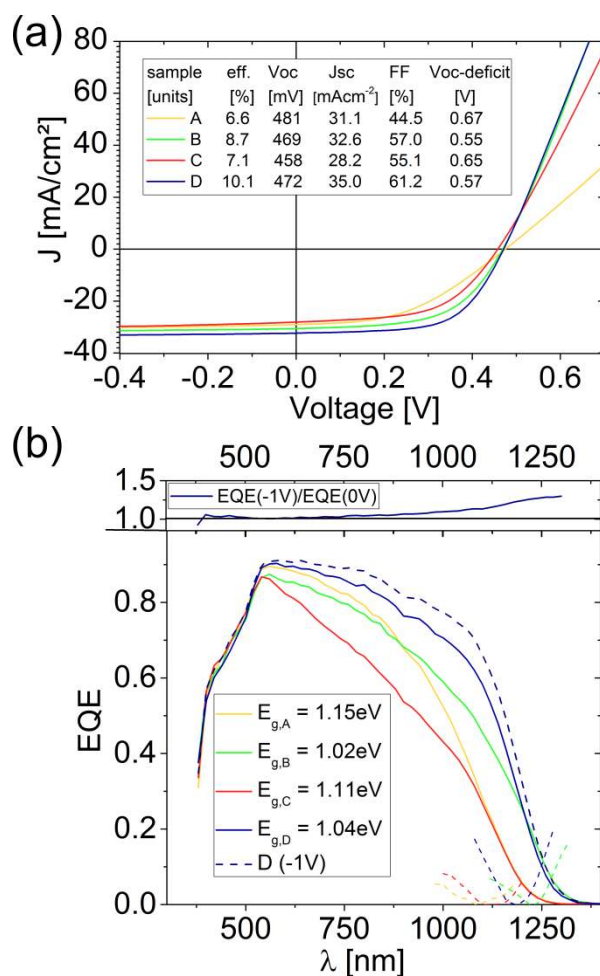


Figure 3. a) J - V characteristic of samples A – D. Photovoltaic parameters refer to total area measurements. b) EQE spectra for samples A – D as well as an EQE spectrum for sample D under a reversed bias of -1 V . The minimum in the derivative of the EQE curve from the long-wavelength range is used to estimate the absorber bandgap.

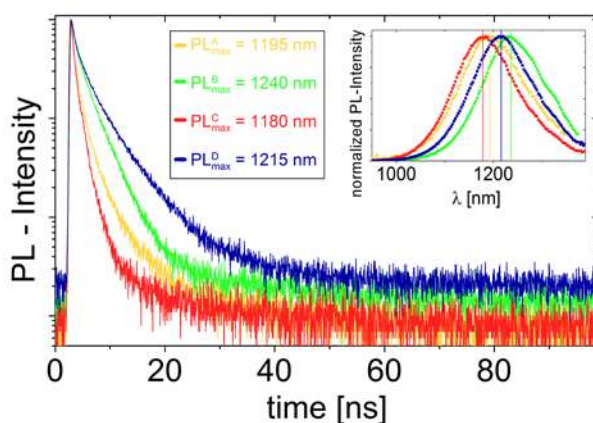


Figure 4. TRPL transient of samples A – D measured on complete cells measured at room temperature. The inset shows room temperature PL spectra of samples A – D.

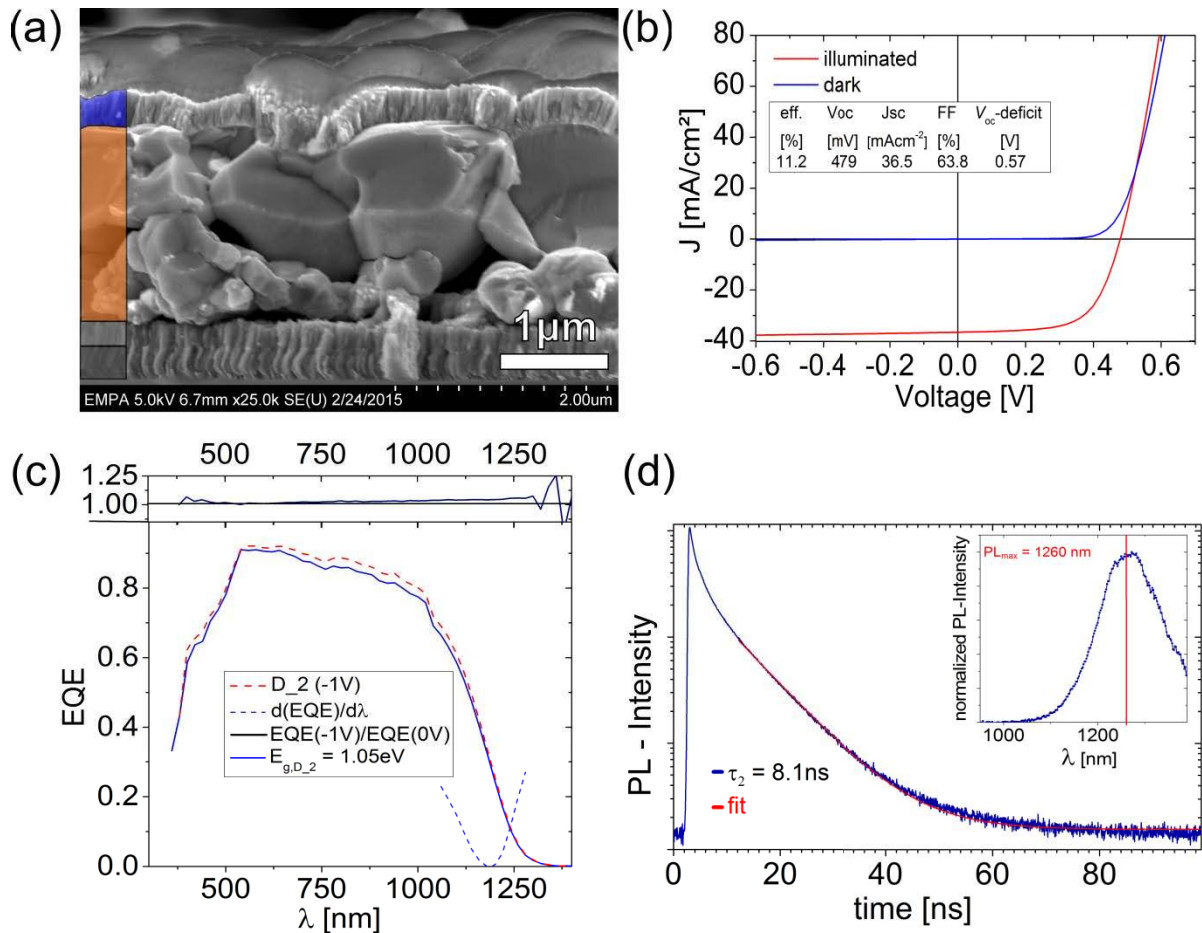


Figure 5. Characteristics of best device D₂ obtained with the identical fabrication process as sample D. a) SEM cross section exhibiting large grained morphology. b) Dark and illuminated *J-V*-measurement. c) EQE measured with 0 V and -1 V bias. The integrated EQE yield the current of 36.5 mAcm⁻². The bandgap is estimated from the minimum in the derivative in the long-wavelength range. In the upper part the ratio of EQE(-1V)/EQE(0V) is shown. d) TRPL transient at room temperature yields a minority carrier lifetime of 8.1 ns, and the PL maximum is located at 1260 nm.

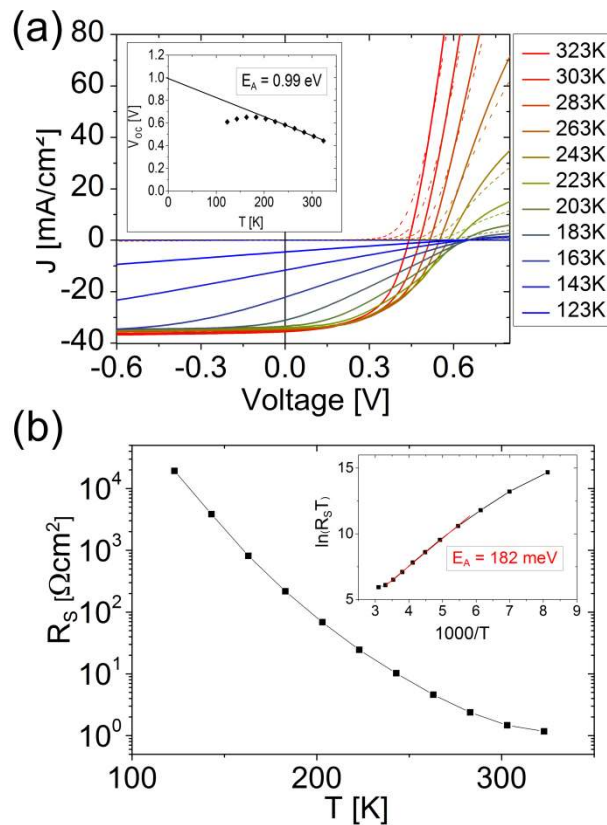


Figure 6. a) Temperature dependent J - V -measurement (dark curve – dotted line, light curve – solid line) of device D₂. The inset shows a linear fit of V_{oc} that can be extrapolated to an intersection value of $E_A = 0.99$ eV, which is close to the estimated bandgap of $E_g = 1.05$ eV. b) Temperature dependence of the series resistance R_s of sample D₂ obtained from the dark J - V curves, which is fitted with a thermal activation energy $E_A = 182$ meV.

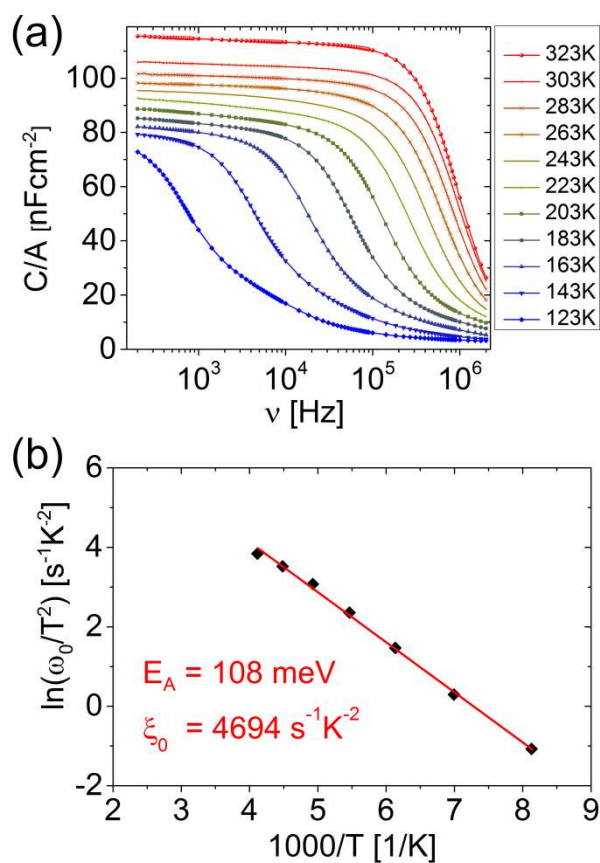


Figure 7. a) Temperature-dependent capacitance frequency measurements in the temperature range from 123 K to 323 K and frequencies from 200 Hz to 2 MHz. b) Arrhenius plot of the freeze out frequency yields an activation energy of $E_A = 108 \text{ meV}$ with $\xi_{\infty 0} = 4694 \text{ s}^{-1}\text{K}^{-2}$.

Table 1. Comparison of PV parameters of published kesterite solar cells with more than 10% conversion efficiency.

| Cell | Eff. [%] | FF [%] | V_{oc} [mV] | J_{sc} [mAcm ⁻²] | R_s [Ω cm ²] | G_s [mScm ⁻²] | A | J_0 [Acm ⁻²] | E_g [eV] | $E_g - V_{oc}$ [eV] | τ [ns] |
|--|---------------------|-------------|---------------|--------------------------------|------------------------------------|-----------------------------|---------------------|----------------------------|---------------------|---------------------------|--------------------|
| solution-processed | | | | | | | | | | | |
| Sample D 2 ^b | 11.2 | 63.8 | 479 | 36.5 | 1 | 0.9 | 1.14 | 3.16 E-06 | 1.05 | 0.57 | 8.1 |
| IBM ^[1] CZTSSe ^a | 12.6 | 69.8 | 513.4 | 35.2 | 0.72 ^[f] | 1.61 ^[f] | 1.24 | 7.00 E-08 | 1.13 | 0.617 | 6.7 ^[g] |
| UW ^[11] CZTSSe ^b | 11.8 ^[e] | 68.1 | 449 | 38.8 ^[e] | 0.43 | 0.19 | 1.6 | - | - | - | - |
| ZSW ^[10] CZTSSe ^b | 10.3 | 69.6 | 471 | 31.6 | 0.5 | - | - | - | 1.07 | 0.6 | - |
| vacuum-processed | | | | | | | | | | | |
| IBM ^[2] CZTSe ^c | 11.6 | 67.3 | 423 | 40.6 | 0.32 | 1.66 | 1.57 ^[h] | 1.38 E-03 ^[h] | 1.0 | 0.58 | 2-2.5 |
| Solar Frontier ^[27] CZTSSe ^c | 10.8 | 64 | 502 | 33.5 | 0.92 | 2.57 | 1.9 | 1.0 E-06 | 1.06 ^[i] | 0.56^[i] | - |
| IMEC ^[3] CZTSe ^d | 10.4 | 66.2 | 394.9 | 39.7 | 0.6 | 0.93 | - | - | 1.0 | 0.6 | 7 ^[k] |

All cells use an AR-coating; ^{a)} Pure-solution approach utilizing hydrazine as solvent; ^{b)} DMSO-based solution approach; ^{c)} Selenization of co-evaporated metal precursors; ^{d)} Selenization of sputtered metal precursors; ^[e] active area; ^[f] measured under illumination; ^[g] for a 11.1% device^[22]; ^[h] derived from J-V-characteristics; ^[i] determined from linear fitting the transformed EQE curve; ^[k] for a 9.7% device^[28]

Supporting Information

Supporting Information is available online from the Wiley Online Library or from the author.

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Supporting Information

11.2% - efficient solution processed kesterite solar cell with a low voltage deficit.

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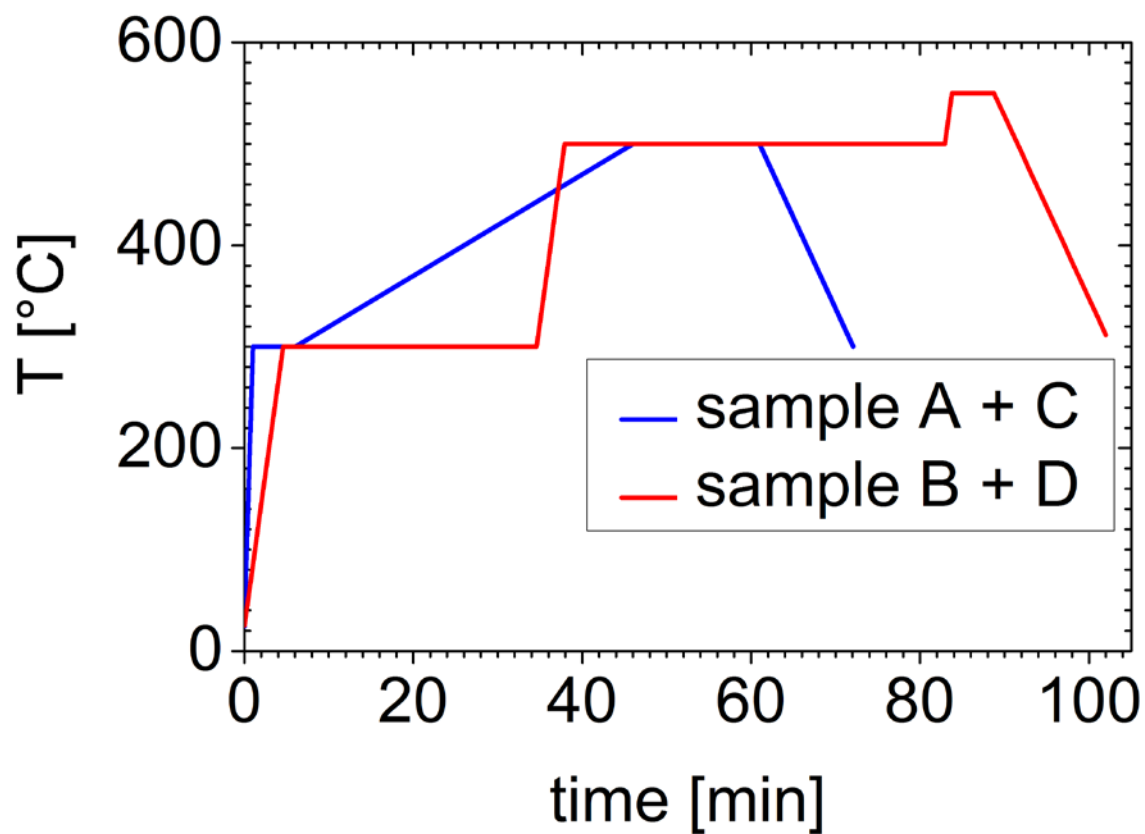


Figure S1. Temperature-time profile of the selenization run for precursors A, C and B, D. The holding temperatures are 300°C and 500°C for the 2-stage annealing (sample A + C) and 300°C, 500°C and 550°C for the 3-stage annealing (sample B + D).

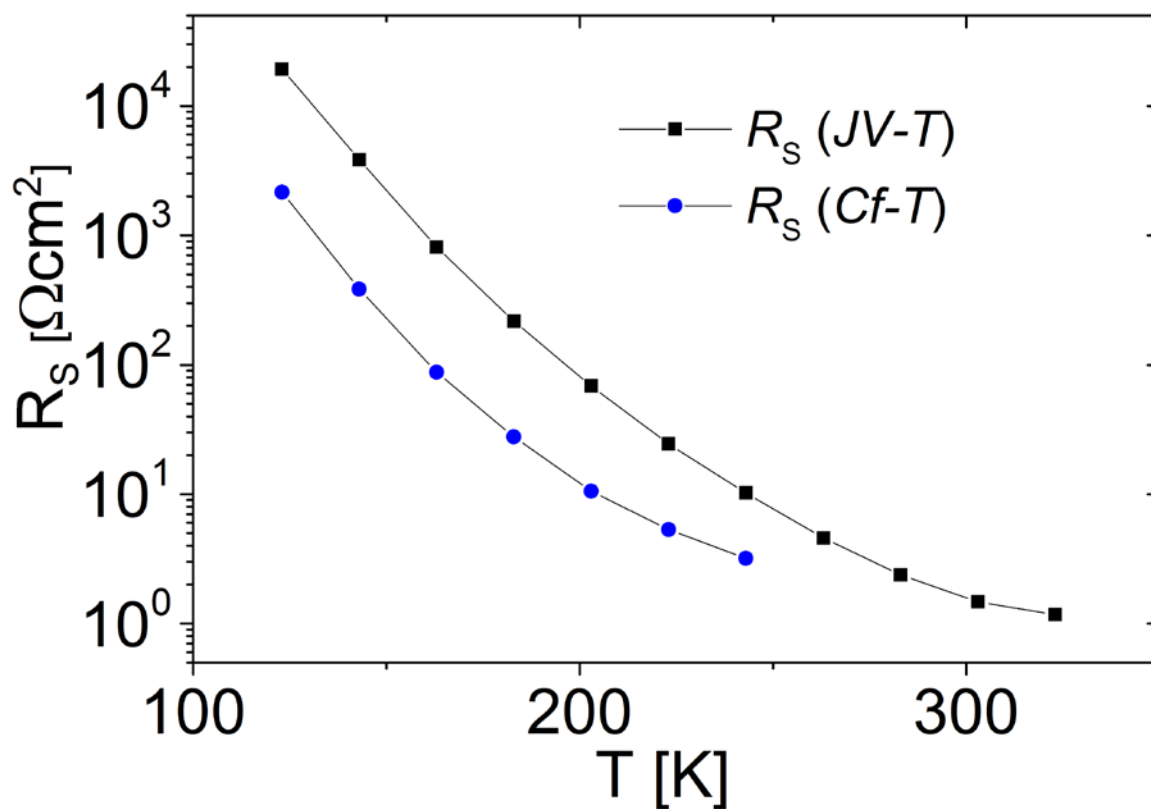


Figure S2. R_s from $JV-T$ in comparison to the calculated R_s from $Cf-T$ measurements. The obtained values differ by one order of magnitude and imply that the increase in R_s from $JV-T$ and the observed freeze out of the capacitance signal in $Cf-T$ measurements do not originate from the same source.