12.5 nm base pseudomorphic heterojunction bipolar transistors achieving f_T=710 GHz and f_{MAX}=340 GHz

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The pseudomorphic collector structure is known to allow enhanced collector transport, facilitating higher current cutoff frequencies at lower current densities and junction temperatures compared to traditional single heterojunction structures. The performance of a $0.25 \times 3\ \mu\text{m}^2$ pseudomorphic heteojunction bipolar transistors achieves peak f_T of 710 GHz (f_{MAX}=340 GHz) at a collector current density of 20 mA/μm^2. The same device achieves a f_T/f_{MAX} of 540/407 GHz at a reduced current density of 7.5 mA/μm^2. The epitaxial structure employs a 12.5 nm strained InGaAs base and 55 nm InGaAs collector, and exhibits a β of 115 and breakdown voltage of BV_{CEO}=1.75 V.
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Terahertz (THz) communication systems require the development of ultrafast transistor technologies. InP-based heterojunction bipolar transistors (HBTs) are currently the most promising technology for achieving THz operation based on the cutoff frequency versus breakdown voltage trend for various transistor technologies and material systems.[1] Single heterojunction bipolar transistors (SHBTs), type I InGaAs/InP double heterojunction bipolar transistors (DHBTs), and type II GaAsSb/InP DHBTs have significantly advanced high-frequency performance, with each technology achieving cutoff frequencies above 300 GHz.[2–6] Earlier work on InP/InGaAs SHBTs has demonstrated f_T values of 550 GHz with a current density of 20 mA/μm^2, corresponding to junction temperatures beyond 200 °C.[5] Further vertical scaling of the SHBT toward THz frequencies will require current densities exceeding 100 mA/μm^2, which is unacceptable as junction temperatures would surpass 500 °C. Recently, it was proposed and experimentally demonstrated that pseudomorphically grading the collector of an SHBT showed an increase in device speed, with a reported f_T=604 GHz at a reduced current density and junction temperature.[7] The increased cutoff frequency dependence on current density for the pseudomorphic HBT (PHBT) devices emphasizes the outstanding transport capabilities of the pseudomorphic-collector material system when parasitic capacitances are carefully controlled. In this work, we optimize the PHBT layer structure by implementing a 21% indium compositional grade from the base to the subcollector of the PHBT. A 25% increase in the effective electron velocity in the collector is estimated when compared to a lattice matched $In_{0.53}Ga_{0.47}As$ collector, resulting from the increased overshoot distances due to the larger Γ-L spacing in the graded collector and the increased mobility of the indium-rich crystal. The base thickness is reduced to 12.5 nm, implementing both compositional and dopant gradings, and aggressive lateral scaling is implemented to achieve cutoff frequencies above 700 GHz.

The epitaxial structure used in this work relies heavily on band gap engineering to lower resistances and to exploit the transport and grading capabilities of the ternary InGaAs material system. The emitter structure is composed of a 15 nm pseudomorphic InAs cap, enabling low contact resistance values from the smaller band gap semiconductor and higher n-type dopant incorporation capabilities ($n=8\times10^{19}$).[8] The InAs cap is then graded to lattice matched $In_{0.53}Ga_{0.47}As$, and a 40 nm partitioned InP emitter is implemented to lower the junction capacitance and emitter resistance. The pseudomorphic base consists of a 12.5 nm $In_xGa_{(1-x)}As$ layer, where x=0.47 at the emitter-base junction and x=0.53 at the base-collector junction. In addition, the carbon-doped base is linearly graded from 8×10^{19} cm^{-3} at the emitter-base junction to 5×10^{19} cm^{-3} at the base-collector interface and exhibits sheet resistance values of $R_{\text{SB}}\sim2800\ \Omega/\square$. The 55 nm $In_xGa_{(1-x)}As$ collector is uniformly Si doped to 6×10^{16} cm^{-3}, with the indium composition lattice-matched at the base-collector junction (x=0.53) and compositionally graded 15% to x=0.68 at the collector-subcollector interface. The composite subcollector consists of 10 nm of $In_{0.68}Ga_{0.32}As$ to form a low resistance collector contact, and is then graded to a thicker 350 nm InP subcollector to improve the device thermal resistance. An energy-band diagram

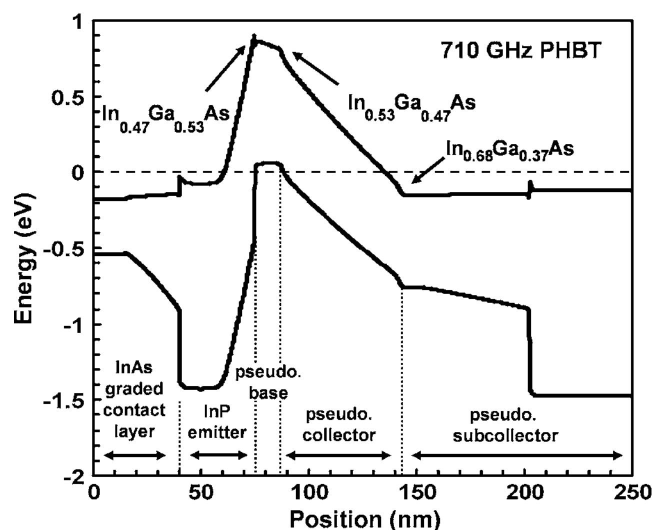

FIG. 1. Energy band diagram for PHBT implementing InAs emitter cap and an indium compositional grading across the base (6% indium grade), collector and subcollector layers (15% indium grade).

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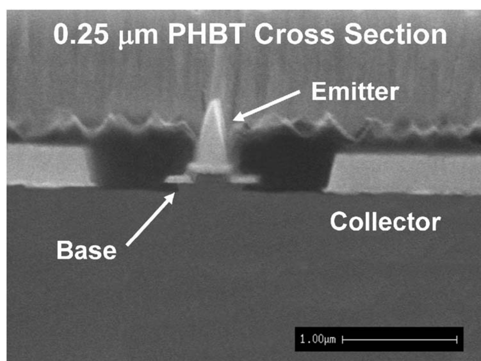

FIG. 2. Cross section of a vertically scaled pseudomorphic heterojunction bipolar transistor with a base-collector mesa width of 0.55 μm and an emitter width of 0.25 μm.

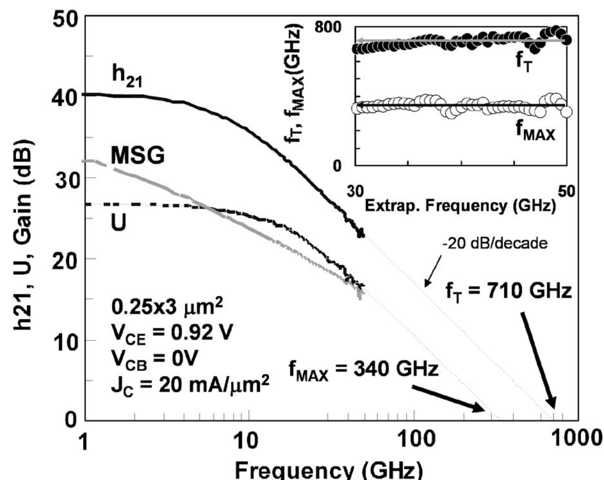

FIG. 4. Extrapolations of h_{21}, U, and MSG/MAG for a 0.25×3 μm^2 PHBT indicating a peak f_T=710 GHz with an associated f_{MAX}=340 GHz at J_C=20 mA/μm^2. The dashed lines represents a fit to ideal single-pole transfer functions for h_{21} and U.

illustrating the epitaxial structure is shown in Fig. 1.

Aggressive lateral scaling was employed to take advantage of the small transfer length of the base contact (L_T<0.1 μm) resulting from the high base sheet resistance of the 12.5 nm base and to minimize the large parasitic base-collector capacitance C_{BC} from the vertically scaled 55 nm collector. Due to the smaller transfer length, the base finger width can be significantly reduced without increasing the base resistance. Masking of the base-collector junction prior to etching was accomplished using a silicon nitride spacer process, with the fabricated mesa width of 0.55 μm achievable for a 0.25 μm^2 emitter. A scanning electron micrograph PHBT cross section is shown in Fig. 2. The base mesa scaling shows a 25% reduction in the extrinsic C_{BC} compared to the optically defined mesa formation technique reported in earlier works,[7,9] and is largely responsible for the high cutoff frequencies reported in this letter. Despite the thin base, no base-collector shorting was observed, as nonalloyed Ti/Pt/Au Ohmic base contacts and low-temperature nitrides were used to prevent contact diffusion though the base.

Gummel and common-emitter curves are shown in Fig. 3, with idealities of the Gummel curves of 1.1 and 1.8 for the collector and base, respectively. The knee voltage is 0.7 V at high current densities, and shows no effects from thermal collapse or current blocking. The collector-emitter breakdown, determined when I_C=50 μA, is measured at breakdown voltage $(BV)_{CEO}$=1.75 V, and the dc gain β is 115.

High frequency measurements were performed at room temperature using an off-wafer short-open-load-through calibration on an HP8510C vector network analyzer from dc to 50 GHz. Open and short on-wafer standards were subsequently de-embedded from the measured devices to remove capacitances and inductances associated with the pads. All high-frequency measurements were verified on an Agilent E8364A PNA with near-identical results. A plot showing h_{21}, Mason's U, and the maximum stable gain/maximum available gain (MSG/MAG) is shown in Fig. 4 for a 0.25×3 μm^2 PHBT. Cutoff frequencies f_T=710 GHz and f_{MAX}=340 GHz were determined by extrapolating the −20 db/decade roll-offs of h_{21} and U (inset), and are in excellent agreement with the single-pole transfer function represented by the dashed lines in the figure.[10] Peak f_T is achieved at I_C=15.3 mA(J_C=20 mA/μm^2) and a power dissipation of P_{diss}=14 mW(V_{CE}=0.92 V, ΔT_j=155 °C). Because of the high current density necessary to achieve peak f_T, the associated f_{MAX} is considerably lower than at

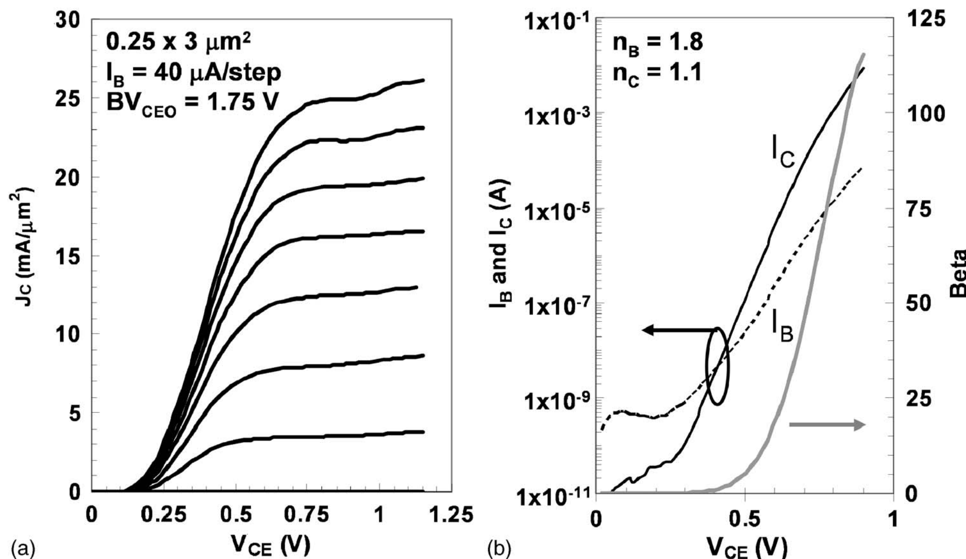

FIG. 3. Common emitter (left) and Gummel (right) curves for a 0.25×3 μm^2 PHBT. A BV_{CEO} of 1.75 V is determined at an I_C of 50 μA.

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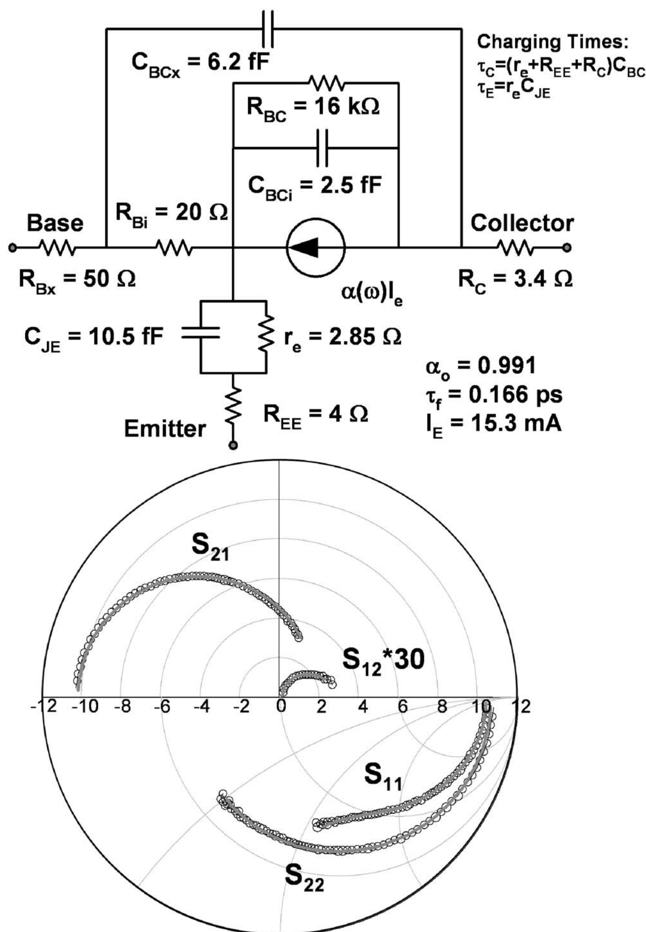

FIG. 5. (a) Small-signal equivalent circuit model and (b) modeled (solid lines) vs measured (open circles) S parameters on a hybrid polar/Smith chart for a $0.25\times 3\ \mu\mathrm{m}^2$ PHBT biased at peak f_T=710 GHz.

lesser current densities; operating the same device at I_C=5.5 mA(J_C=7.5 mA/μm^2, ΔT_j=55 °C), the cutoff frequencies are more balanced at 540/407 GHz for f_T/f_{MAX}. While this higher f_{MAX} value is more desirable for high-speed analog circuit design, the remainder of this letter will investigate the device operation at peak f_T with the intent of addressing issues to enable THz-bandwidth operation.

The small signal equivalent circuit elements for this device were extracted/optimized from measured S parameters, and are shown in Fig. 5(a). The measured and modeled S parameters show excellent agreement in Fig. 5(b), with the modeled parameters simulating an f_T of 720 GHz and an f_{MAX} of 320 GHz. The forward delay of the device, obtained by extrapolating $1/2\pi f_T$ vs $1/I_C$ to the y axis, is 166 fs. After removing the $(R_{\mathrm{EE}}+R_C)\times C_{\mathrm{BC}}$ component, the total base-to-collector transit delay is calculated to be 105 fs, illustrating the effectiveness of the vertically scaled epitaxial structure. Hot electron injection from the abrupt emitter-base junction plays an important role in reducing the transit time in the thin base structure. The transit time is reduced from 65 fs in a 20 nm PHBT structure[7] to approximately 40 fs in this work, which corresponds well with the theoretical and experimental calculations performed by Zokar *et al.*[11] This reduction in transit time is also confirmed by an increase in β from 65 in the 20 nm base device to 115 in the 12.5 nm base device. The extracted collector transit time estimates that the pseudomorphic collector is yielding electron velocities of 4.25×10^7 cm/s, significantly higher than the effective collector velocities of $3.3\times 10^7\ \mathrm{cm}^{-3}$ extracted from lattice-matched InGaAs collectors fabricated on earlier UIUC HBT structures. The emitter charging delay, calculated from $\tau_E=r_e\times C_{\mathrm{JE}}$, is determined to be 30 fs, and the collector charging delay is calculated to be $\tau_{\mathrm{CC}}=(R_{\mathrm{EE}}+r_e+R_C)\times C_{\mathrm{BC}}$ =89 fs. It is noteworthy to mention that, for the first time in a high-performance submicron HBT, the charging delays dominate the total device delay despite the aggressive lateral scaling of dimensions. As the charging delay is the dominant delay term, future efforts need to be focused on the reduction of parasitic capacitances and resistances, primarily C_{BC} and R_{EE}, through advanced processing techniques.

In conclusion, the pseudomorphic collector grading allows many benefits, such as increased mobility in the indium-rich material, as well as higher Γ-L separation, allowing velocity overshoot to occur over a larger portion of the collector region to effectively reduce the collector transit time. A $0.25\times 3\ \mu\mathrm{m}^2$ HBT was shown to exhibit a record performance f_T of 710 GHz from aggressive lateral scaling of the base mesa due to the narrow transfer length of the base contact. The lower operating current density and better thermal conductivity achieved with the PHBT structure is a critical step to enabling a THz-frequency HBT at realistic operating conditions.

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