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Abstract: A design method of low-pass (LP) negative group delay (NGD) integrated circuit (IC) implemented in 130-nm BiCMOS technology is investigated. The LP-NGD circuit is composed by RL-network with BiCMOS high Ohmic unsalicided N+poly resistor and symmetrical high current spiral inductor. The design methodology of the investigated LP-NGD circuit is explained by chip layout process. Then, the pre-simulation is performed with the design rule check (DRC) and 225 µm × 215 µm layout versus schematic (LVS) approaches. The LP-NGD design feasibility of the BiCMOS IC implementation is validated by AC frequency domain simulation with realistic component implementation constraints. As expected, the ideally calculated and simulated results show NGD of about -100 ps with 1.12 GHz cut-off frequency and -6 dB attenuation. Moreover, the LP-NGD function is also verified with transient analyses with Gaussian pulse and arbitrary waveform signals. As expected, despite the attenuation, the output signal leading and tailing edges appear in time-advance of about -100 ps compared to the input ones.

Keywords— 130-nm BiCMOS technology, Design method, Negative group delay (NGD), Low-pass (LP) NGD integrated circuit (IC), RL-network passive topology.

1. INTRODUCTION

The unfamiliar negative group delay (NGD) function is one of the most intriguing electronic functions. Because of its counterintuitive aspect, the design engineering of NGD electronic function remains a breakthrough for research designers. The initial experimentation highlighting the NGD effect existence was performed with negative group velocity (NGV) 3-D structures in 1980s [1-2]. The design feasibility of unfamiliar NGD electronic circuit becomes an attractive topic for curious RF and microwave engineering researchers. The NGD passive circuits were designed with NGV metamaterial 3-D periodical structures. The preliminary solutions were deployed in 2000s with the design of metamaterial inspired compact NGD microstrip circuits [3-5]. The 3-D to 1-D transfer function (TF) analogy leads to the implementation of metamaterial based NGD circuits [3-8]. The NGD function was verified in the microwave frequencies with more than 20-dB attenuation periodical artificial transmission line (TL) circuits [3-6]. Diverse NGD metamaterial-based circuits using tunable varactor diode [7] and resistive lossy left-handed TLs [8] were proposed.

Nevertheless, compared to the classical electronic functions as filters, amplifier, oscillator, antenna, etc., nowadays a lot of efforts must be accomplished about the NGD design technique. Indeed, the NGD design method is still not familiar to most of electronic design engineers. Furthermore, the NGD interpretation raises curious questions from academic and industrial researchers. Therefore, further research for easy to understand knowledges about the NGD function must be conducted. Accordingly, because of the similarity between the linear circuit magnitude and group delay (GD) responses, a basic theory based on the analogy between the filter and NGD behavior was initiated [9]. Emphatically, different classes of NGD circuits were proposed and expected to be commonly and conventionally used by the non-familiar and non-specialist engineers in the future. Following the innovative concept, a class of low-pass (LP) NGD function was approved by passive [10-14] and active [15-18] circuit studies.

In addition to the research work performed on the NGD understanding, several challenges are expected to be overcome on the NGD design method especially in term of circuit cumbersome and size reduction. Compact NGD circuits were designed in microstrip technology [19-20]. However, nowadays, the existing NGD electronic circuits [3-20] are generally designed with centimeter or decimeter size ranges. To overcome the size limitation bottleneck, we would like to develop a design method of NGD integrated circuit (IC) in CMOS technology similar to the classical electronic functions as frequency synthesizer [21] and transceiver devices [22-23].

Doing this, by inspiring from the inductor component CMOS design [24-25], an original design method of RL-network based LP-NGD passive circuit is initiated in the present paper. So far, the study of RL-network based NGD circuits are limited to the topologies implemented with lumped components [9-12,14]. The first design study of LP-NGD BiCMOS IC is introduced in the present paper which is organized in four main sections as follows:

- Section 2 describes the LP-NGD passive topology, circuit theory and the analytical characterization. By exploiting the voltage transfer function (VTF), the main LP-NGD specifications are expressed.
- Section 3 presents the synthesis and design methodology of the LP-NGD IC implemented in 130-nm BiCMOS technology is developed. The feasibility study of LP-NGD BiCMOS IC design is presented with a proof of concept (PoC). Comparisons between BiCMOS IC PoC frequency simulations from the Cadence® commercial tool, and analytical calculations are discussed.

- Section 4 is focused on the transient analyses of LP-NGD BiCMOS IC PoC. The time-domain signature of the LP-NGD function will be discussed based on the calculated and Cadence® simulated results.
- Then, Section 5 ends the paper with conclusion.

2. THEORETICAL DESIGN OF LP-NGD CIRCUIT UNDER STUDY

This section introduces the LP-NGD passive circuit theory. After the topological description, the design and synthesis equations in function of the desired LP-NGD specifications will be explored.

2.1 Description of the LP-NGD passive topology

Fig. 1 introduces the LP-NGD circuit composed by a series resistor R_a and shunted by series RL-network. The input and output voltages are denoted by $V_i(s)$ and $V_o(s)$ by taking $s=j\omega$ as the Laplace variable.

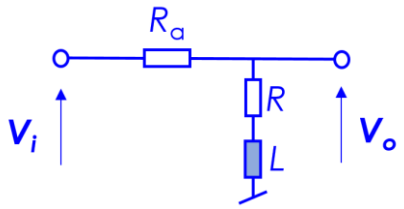

Fig. 1. RL-network circuit under study.

The NGD analysis is based on the RL-circuit VTF model defined by $N(s)=V_o(s)/V_i(s)$. Then, we have the transfer function:

$$N(s)=\frac{R+Ls}{R_a+R+Ls}. \tag{1}$$

The associated magnitude and phase are expressed by $N(\omega)=\left|N(j\omega)\right|$, and $\varphi(\omega)=\arg\left[N(j\omega)\right]$, respectively. The corresponding GD is given by:

$$GD(\omega)=\frac{-\partial\varphi(\omega)}{\partial\omega}. \tag{2}$$

Based on this preliminary mathematical definition, the LP-NGD particular specifications considered for the IC design methodology are introduced in the following subsection.

2.2 Analytical LP-NGD specifications of the passive circuit topology

The familiarization to the NGD analysis starts essentially by the characterization of VTF GD response. An electronic circuit can be assumed as a LP-NGD function if the GD at very low-frequencies (VLFs) satisfies the inequality $GD(\omega \approx 0) < 0$. The associated cut-off angular frequency, ω_n, is the root of equation $GD(\omega_n) = 0$. This means that the GD response should verify the condition:

$$\begin{cases} GD(\omega \le \omega_n) \le 0 \\ GD(\omega > \omega_n) > 0 \end{cases} \tag{3}$$

as explained by the ideal diagram of Fig. 2(a). In addition, to the GD response, the VTF magnitude response as shown in Fig. 2(b) must be specified. For example, the LP-NGD circuit can be designed by expecting a desired attenuation, $N(\omega \approx 0) = N_0 < 1$.

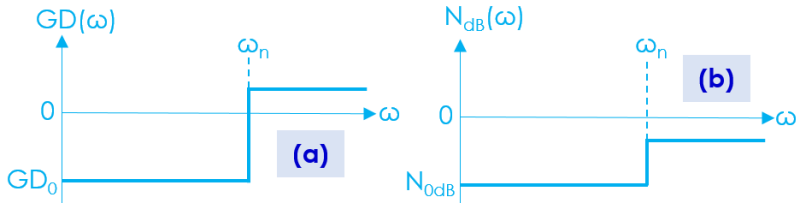

Fig. 2. Ideal LP-NGD VTF responses: (a) GD and (b) magnitude.

Based on the GD and magnitude ideal specifications, the analytical formulas are established in the following subsection.

2.3 LP-NGD analytical characterization

The LP-NGD characterization is developed from the VLF behavior where $\omega \approx 0$. Accordingly, the magnitude from VTF equation (1) at the VLFs is expressed as:

$$N_0 = \frac{R}{R_a + R} \tag{4}$$

Furthermore, the GD derived from equation (2) at the VLFs is equal to:

$$GD_0 = \frac{-R_a L}{R(R_a + R)}. \tag{5}$$

Then, the NGD cut-off frequency is written as:

$$\omega_n = \frac{\sqrt{R(R_a + R)}}{L}. \tag{6}$$

The NGD performance can be qualified by the figure-of-merit (FoM) defined as the product of VLF NGD value, NGD cut-off frequency and attenuation:

$$FoM = \omega_n N_0 |GD_0| \tag{7}$$

Substituting the magnitude, GD and cut-off frequency expressions given in equations (4), (5) and (6) into equation (7), the previously formulated FoM in function of resistive elements is expressed as:

$$FoM(R,R_a)=\frac{R_a\sqrt{R}}{(R_a+R)\sqrt{R_a+R}} \tag{8}$$

Based on these expressions, design formulas of resistor and inductor components are established in the following subsection.

2.4 Design formulas of the LP-NGD circuit components

The LP-NGD function main specifications is represented by the desired parameters, attenuation, N_0=A, power consumption, P, input signal amplitude, V_{max}, NGD value, GD_0<0, and NGD cut-off frequency, $\omega_n = 2\pi f_n$. Accordingly, knowing the desired specification values, the resistor components are given by the following design formulas:

$$R=\frac{V_{\max}^2 A}{P} \tag{9}$$

$$R_a=\frac{V_{\max}^2 (1-A)}{P}. \tag{10}$$

The inductor component can be calculated from:

$$L=\frac{-GD_0 R_a A}{(1-A)^2}. \tag{11}$$

Based on these resistor and inductor component expressions, we can demonstrate that the FoM defined by equation (8) can be simplified in function of the desired attenuation as follows:

$$FoM(A)=(1-A)\sqrt{A}. \tag{12}$$

By using these design formulas, we intend to design the smallest LP-NGD passive circuit by considering 130-nm BiCMOS technology.

The next section is focused on the design methodology and validation of the LP-NGD CMOS IC PoC.

3. LP-NGD CMOS IC POC DESIGN AND AC SIMULATION

The present section deals with the LP-NGD function chip design methodology. The PoC IC is designed in 130-nm BiCMOS technology. To validate the LP-NGD design, frequency or AC simulations were performed with Cadence® VIRTUOSO® simulator. Then, the calculated and simulated results are discussed.

3.1 Design methodology

Fig. 3 describes the RL-network LP-NGD CMOS design flow. The IC design can be organized in six consecutive different steps:

- Step 1 is the attribution of desired LP-NGD specifications aforementioned in the diagram shown by Figs. 2.
- The ideal circuit parameters are calculated in Step 2 via formulas (5), (6) and (7).
- Step 3 is the 130-nm CMOS design rule check (DRC) with high Ohmic unsalicided N+poly resistor and symmetrical high current spiral inductor. After the ideal electrical simulation from the designed schematic and preliminary drawing of the layout, the physical verification can be done with Mentor Graphics Calibre® DRC tool in flat configuration, allowing to check every design rule and IC layout consistency. The width and spacing of each wire constituting the layout must be correctly implemented and should not violate the specified minimum value.
- Step 4 is the layout versus schematic (LVS) simulation.
- Then, Steps 5 and 6 are the post-layout simulation and the LP-NGD specification validation.

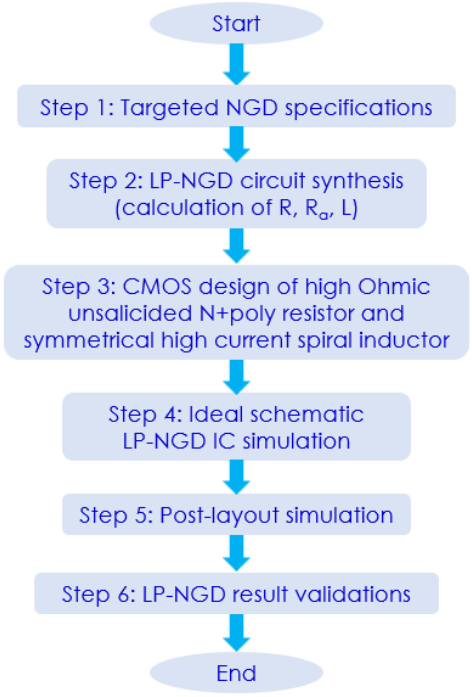

Fig. 3. Design flow of LP-NGD BiCMOS IC.

By applying the developed design flow, we obtain the LP-NGD IC PoC result investigated in the following subsection.

3.2 Description of the CMOS IC schematic and layout

The STMicroelectronics® BiCMOS-130 nm manufacturing technology was chosen for this study because of its component integration potential in the range of LP-NGD desired specification values. Due to the relatively large size of the components, expensive manufacturing processes such as 28 nm-FDSOI are not needed.

3.2.2 Design of schematic and layout

The passive LP-NGD structure PoC of the present feasibility study was designed in the Cadence® VIRTUOSO environment. Fig. 4 displays the LP-NGD IC chipset schematic. The circuit parameters were calculated from synthesis formulas (5), (6) and (7) with respect to the desired specifications indicated by Table I. The chosen specification corresponds to the LP-NGD FoM formulated by equation (12) equal to $FoM = 1/(2\sqrt{2})$.

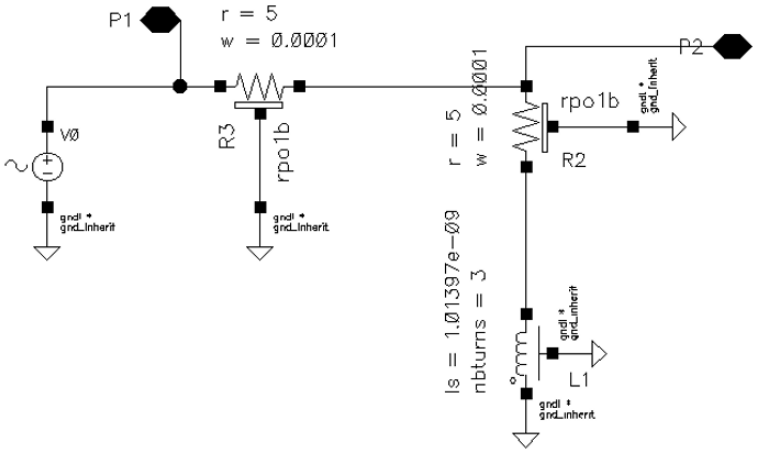

Fig. 4. VIRTUOSO® schematic of LP-NGD circuit chipset.

Objective	Parameter	Name	Chosen value
LP-NGD IC expected specifications	Center frequency	f_n	1.12 GHz
	NGD value	GD_0	-0.1 ns
	Attenuation	A	-6 dB
	Nominal power	P	625 mW
Component calculated value	Resistor	$R=R_a$	5 Ω
	Inductor	L	1 nH

Table I: LP-NGD specifications and PoC IC parameters

Fig. 5 displays the designed BiCMOS IC layout from the schematic of Fig. 4 with VIRTUOSO® platform. The chipset presents physical size, 225 µm × 215 µm or 0.04837 mm². It is interesting to underline that the chipset presents the smallest size design of LP-NGD passive circuit ever being made before. The designed PoC IC is expected to operate with input signal having maximal amplitude V_{max}=2.5 V.

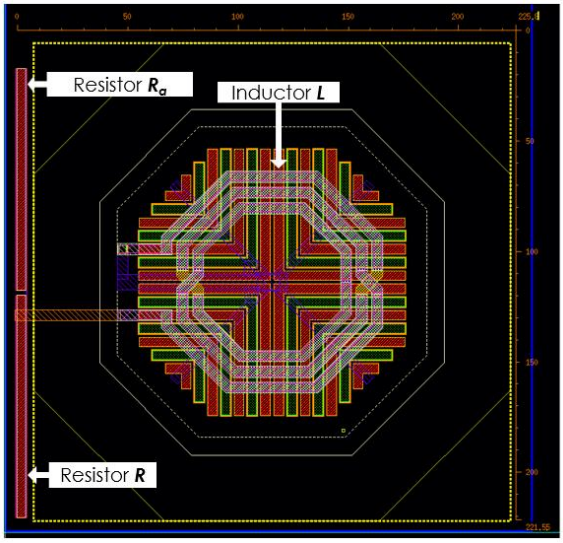

Fig. 5. VIRTUOSO® layout (physical size: 225 µm × 215 µm) of LP-NGD circuit chipset.

3.2.3 Die and interconnection description

The PoC IC is represented by single-input single output passive circuit. The whole layout area is occupied by the two resistors in left and the large spiral inductor. The resistor and inductor structure die are shown by Fig. 6(a) and Fig. 6(b), respectively. The chipset is expected to be implemented under the manufacturing process minimum square area.

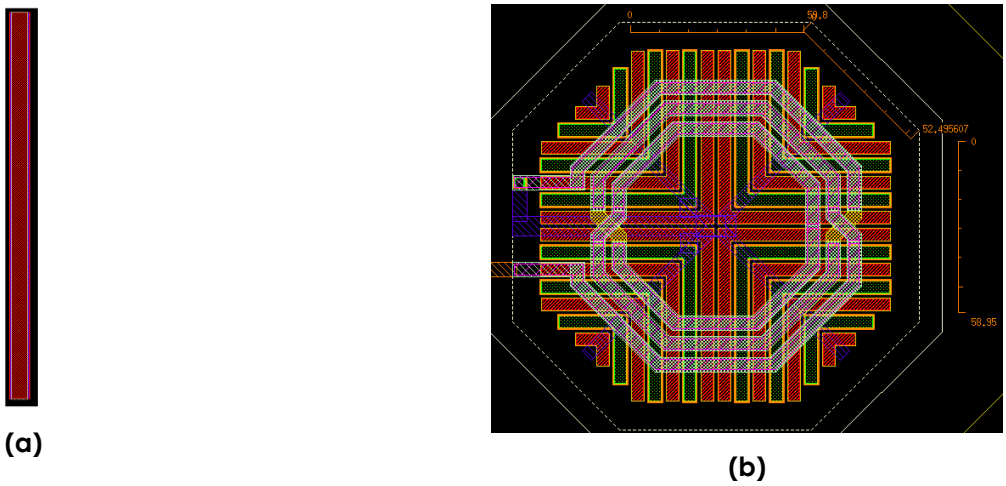

Fig. 6. LP-NGD circuit (a) resistor and (b) inductor die.

Each resistor is guard-ring surrounded in order to ensure their polarization and the ground plane connection through the dielectric substrate. The geometrical size and the structural implementation materials of the resistor depicted by Fig. 6(a) are addressed by Table II.

Role	Description	Parameter	Value
Resistor	Geometry	Shape	Rectangular
		Length	100 µm
		Width	4.9 µm
	Metallization	Cu	-
		Thickness	100 nm
Inductor	Geometry	Octagon	-
		Inner diameter	60 µm
		Outer diameter	105 µm
		Spiral TL width	4.9 µm
		Number of spires	3
		Surface	0.0145 mm²
	Metallization	Cu	-
		Thickness	100 nm
Substrate	Dielectric insulator	poly-Si	-
		Relative permittivity	4.5
		Thickness	100 nm
Interconnection	Metallization	Cu	-
		Thickness	100 nm

Table II: Chipset physical parameters

The inductor die is highlighted by Fig. 7(a). It is implemented in Al-metal spiral octagon with geometrical and physical parameters indicated in Table II. As illustrated by Fig. 7(b), all the die component interconnections are Cu-based interconnect metallization. All the chipset and interconnection structures are implemented on poly-Si dielectric insulator with characteristics shown by Table II.

Fig. 7. (a) Zoom in of inductor die and (b) interconnection metal pad of LP-NGD circuit chipset.

Knowing the chipset design, the LP-NGD function validation is examined in the following subsection.

3.2.4 CMOS IC AC calculated and simulation results

The MATLAB® calculated ("Calc.") from the VTF model expressed earlier by equation (1) and simulated ("Cadence") VTFs were compared from 0 Hz to 2 GHz. Figs. 8 reveal the AC pre-simulation results from VIRTUOSO® schematic diagram which does not involve the layout design. This AC simulation results validate the LP-NGD behavior with a good correlation between the calculated model and simulation in the frequency domain. Table III addresses the associated LP-NGD parameters.

Approach	f_n	GD_0	$T(f\approx 0)$	$T(f_n)$	*FoM*
Calculation	1.128 GHz	-100 ps	-6.02 dB	-3 dB	0.226
Cadence® simulation	1.26 GHz	-76 ps	-5.23 dB	-2.65 dB	0.173

Table III: Comparison of calculated and simulated LP-NGD IC responses

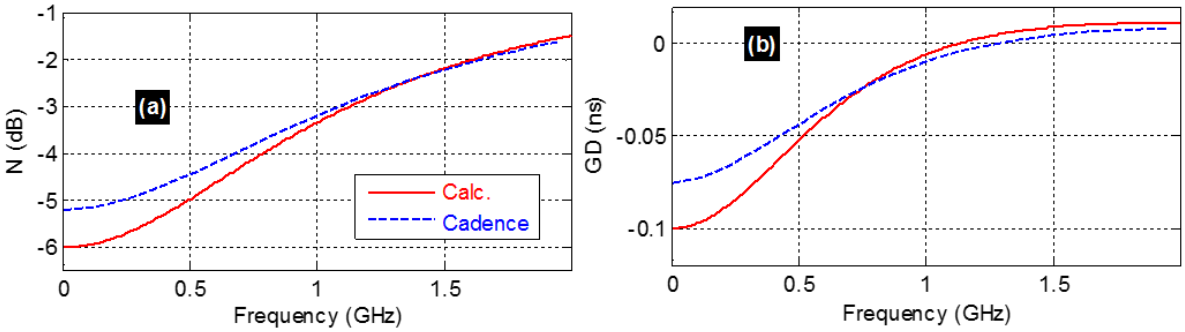

Fig. 8. Comparisons of calculated and simulated VTF (a) magnitude and (b) GD of the LP NGD circuit shown in Fig. 4 and Fig. 5.

Because of the BiCMOS inductance parasitic and chipset design imperfection, it can be found that the NGD absolute value and attenuation from BiCMOS IC present a 24-ps and 1-dB difference at very low frequencies. Due to the NGD specification results, we have around 23% relative difference of calculated and simulated FoMs.

3.2.5 Effect of resistor and inductor non-idealities

In more practical point of view, the main non-ideality effects can occur during the CMOS fabrication processes which is due to the component fabrication micrometric machining inaccuracies. The proposed non-ideality analysis depends on the physical size inaccuracies of BiCMOS high Ohmic unsalicided N+poly resistor and symmetrical high current spiral inductor. Therefore, a Monte-Carlo (MC) mismatch non-ideality analysis was performed with respect

to the resistor and inductor physical lengths and widths. All the lengths and withs are statistically varied around the nominal values over 300 samples. Consequently, during the MC analysis, R_a, R and L are varied of about +/-15%. As result, the histograms plotted in Figs. 9 are obtained. The statistical characteristics of NGD specifications GD_0 and f_n. are summarized in Table IV.

	Mean	Minimal	Maximal	Standard deviation
GD_0	-61.3 ps	-69.3 ps	-53.8 ps	3.4 ps
f_n	1.446 GHz	1.254 GHz	1.663 GHz	92 MHz

Table IV: Statistical characteristics of NGD specifications GD_0 and f_n from MC mismatch non-ideality analysis

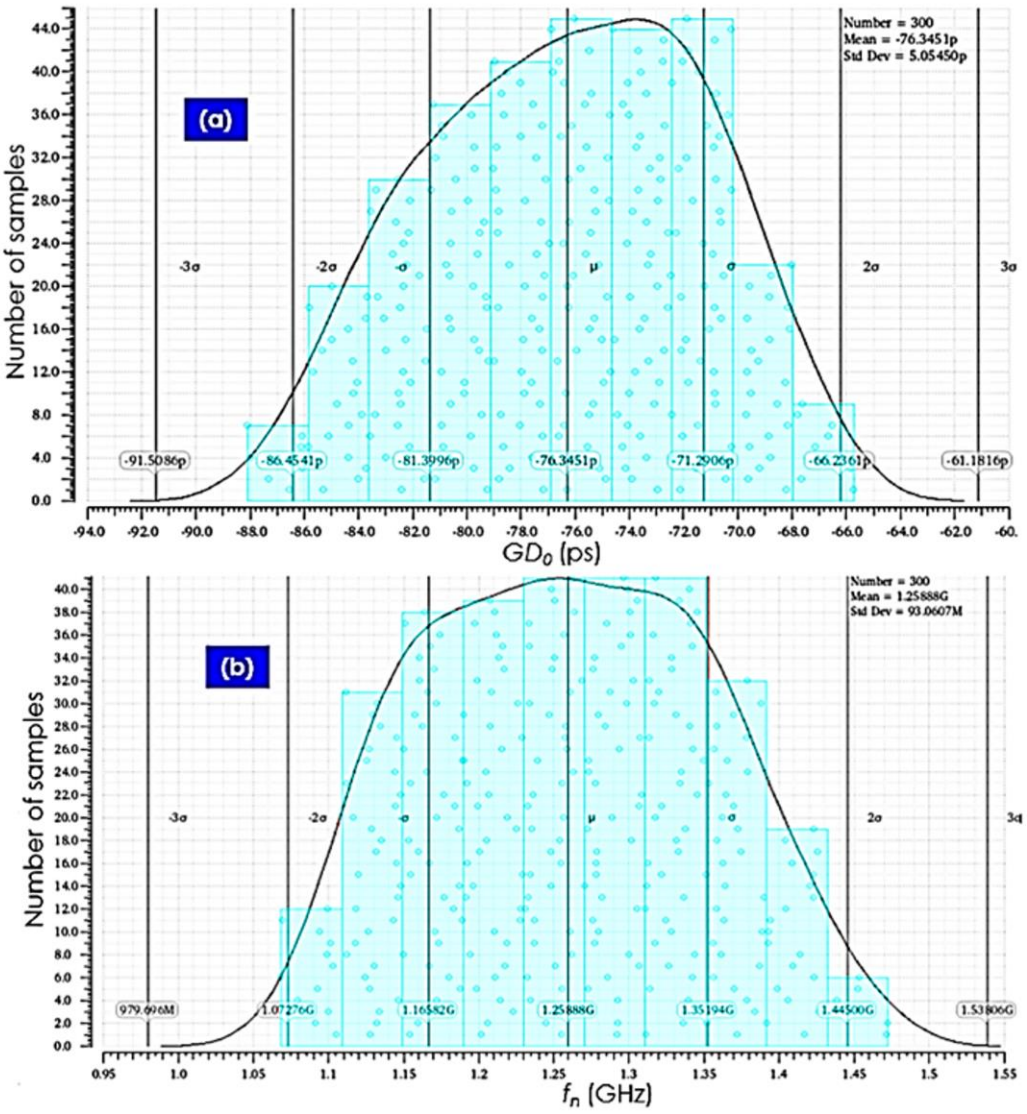

Fig. 9. Monte Carlos analysis histograms of (a) GD_0 and (b) f_n

3.2.6 Comparison with LP-NGD characteristics available in the literature

An additional state of the art about the LP-NGD characteristics and physical size from passive circuit available in the literature [10-14] was performed. Table V indicates the comparison results with the proposed and designed LP-NGD BiCMOS circuit.

References	Cut-off frequency	NGD value	LF attenuation	Size
[10]	13.78 MHz	-13.33 ns	-9.5 dB	-
[11]	1 kHz	-100 ns	-5 dB	10 mm x 17 mm
[12]	375 kHz	-0.3 ms	-6 dB	10 mm x 17 mm
[13]	490 MHz	-0.12 ns	-3.33 dB	-
[14]	8 MHz	-1.78 ns	-5.34 dB	50 mm x 40 mm
This work	1.26 GHz	-76 ps	-5.23 dB	225 µm × 215 µm

Table V: Comparison of LP-NGD characteristics

As aforementioned in the introduction of the present study, the LP-NGD IC PoC presents a clear advantage on two aspects:

- The possibility to operate with very high NGD cut-off frequency,
- And the design feasibility of especially the circuit physical size.

For more convenient illustration of the validation, the following section will examine the LP-NGD transient responses.

4. TRANSIENT VALIDATION RESULTS OF THE LP-NGD FUNCTION WITH THE CMOS IC POC

The present section is focused on the LP-NGD function transient characterization. The transient analysis is based on the comparison between the calculated and simulated results of the previously designed IC BiCMOS PoC.

4.1 Analytical method of LP-NGD transient characterization

The LP-NGD transient analysis must be performed with smoothed signal presenting spectrum belonging to the NGD frequency band. The analysis can be made by considering Gaussian waveform pulse input signal analytically defined by the expression:

$$v_{in}(t) = V_{\max}\, \mathrm{e}^{-(t-t_0)^2/\tau_a^2} \tag{13}$$

with maximal peak, $V_{\max} = v_{in}(t_0)$, at instant time, t_0, and depending the NGD bandwidth [28]:

$$\tau_a = \frac{\sqrt{a_{dB}\ln(10)/5}}{\pi f_n} \tag{14}$$

where a_{dB} is the expected attenuation in decibel of the Gaussian spectrum at f_n. Knowing the maximal instant time, t_0, the LP-NGD circuit transient characterization can be performed by the determination of rise- and fall-time advances. The leading-edge or rise-time advance is given by:

$$v_{in,out}(t_r^{in,out} < t_0) = \max\left[v_{in,out}(t)\right]/2 \tag{15}$$

The tailing-edge or fall-time advance is determined by the equation:

$$v_{in,out}(t_f^{in,out} < t_0) = \max\left[v_{in,out}(t)\right]/2\,. \tag{16}$$

In addition, the following voltage attenuation between the input and output signals is given by:

$$a = \frac{\max\left[v_{out}(t)\right]}{\max\left[v_{in}(t)\right]}\,. \tag{17}$$

The input and output relative cross-correlation can be assessed with discrete time parameters, minimum, t_{min}, maximum, t_{max} and step Δt. In this case, the discrete value of input and output samples at time instant $t=m\Delta t$ can be expressed as $v_{in}(m) = v_{in}(m\Delta t)$ and $v_{out}(m) = v_{out}(m\Delta t)$, respectively. The integer $m=\{1,\ldots,m_{max}\}$ varies up to $m_{\max} = Ent\left[t_{\max}/\Delta t\right]$ with $Ent(x)$ expresses the integer part of real x.

To verify the feasibility of the time-domain approach, two different test signals were used for this transient analysis of the LP-NGD characteristics from the designed BiCMOS IC. The following paragraphs examines the obtained results from the two cases of study.

4.2 BiCMOS IC transient response of Gaussian waveform pulse signal

The first transient simulation was carried out by considering Gaussian waveform pulse signal. The time-domain investigation was made in the time window presenting duration, t_{max}=4.43 ns. During the simulation, the Gaussian input signal was analytically defined by the different parameters indicated in Table VI.

Parameter	V_{max}	a	τ_a	t_0
Value	1 V	10 dB	610 ps	2.217 ns

Table VI: Specifications of the input Gaussian signal

Fig. 10(a) displays the Gaussian waveform pulse signal natural responses. The input signal is plotted in black solid line. Then, the transient responses from calculation and Cadence® simulated are plotted in red solid and dashed blue lines, respectively.

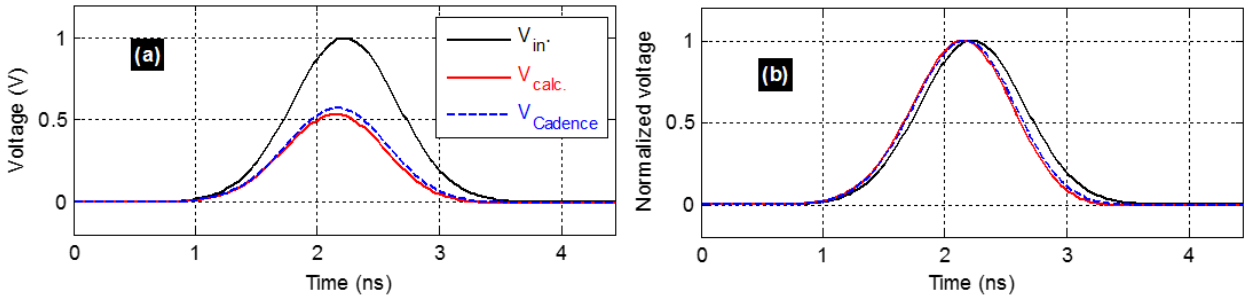

Fig. 10. (a) Natural and (b) normalized plots of calculated and simulated transient LP-NGD BiCMOS IC responses of Gaussian waveform pulse signal.

Acting as a passive circuit, the output is literally attenuated compared to the input. The corresponding normalized response is plotted by Fig. 9(b) to highlight the unfamiliar aspect of apparent time-advance related to the LP-NGD function without violating the causality. In all, the time-domain responses from calculation and simulation are in very good agreement and enable to verify obviously the LP-NGD signature. The extraordinary output Gaussian signal is literally observed in apparent time-advance compared to the input one.

4.3 BiCMOS IC transient response of arbitrary waveform pulse signal

Further confirmation of the LP-NGD signature in the time-domain is highlighted by arbitrary waveform input signal. Accordingly, Fig. 11(a) displays the natural plots of the obtained time-domain responses. The same as the previous case of study by means of Gaussian response, the input signal is plotted in black solid line, and the calculated and Cadence® simulated transient responses are plotted in red solid and dashed blue lines, respectively. In this case, the transient analysis was performed in the time duration, t_{max}=5.55 ns. To highlight the LP-NGD transient signature, the normalized plots of input and output signals are displayed by Fig. 11(b) display the natural and normalized plots of the time-domain responses. Once again, it can be seen that the normalized output is literally observed in apparent time-advance of the input signal.

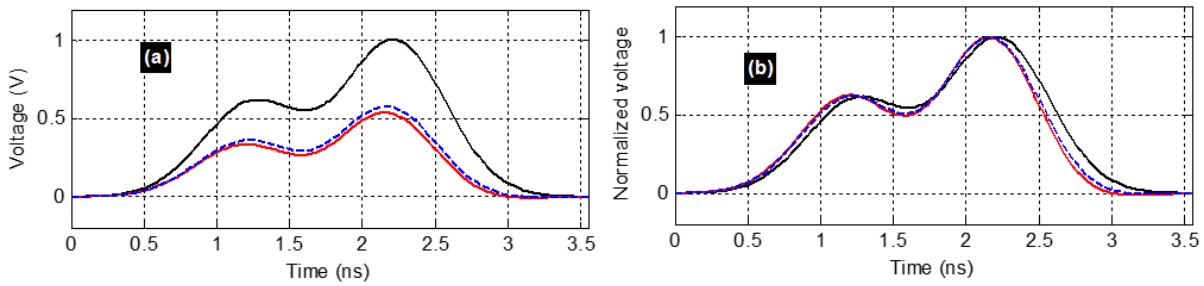

Fig. 11. (a) Natural and (b) normalized plots of calculated and simulated transient LP-NGD BiCMOS IC responses of arbitrary waveform signal.

4.4 Discussion on the transient characteristics of the LP-NGD BiCMOS IC response

Based on the two previous time-domain analysis, the comparison between the simulated and calculated LP-NGD specifications are discussed. Table VII summarizes the LP-NGD parameters from the BiCMOS IC transient characterization. For each cases of study, considerable output advances are obtained for both leading- and tailing-edges. The LP-NGD BiCMOS IC input and output signal cross correlations are higher than 97%.

Approach	Δt_{rise}	Δt_{fall}	a	ϖ_{Gauss}	$\varpi_{arbitrary}$
Calculation	-67 ps	-111 ps	0.533	98.34%	97.96%
Cadence® simulation	-44 ps	-133 ps	0.526	98.35%	97.97%

Table VII: Comparison of simulated and calculated LP-NGD transient characteristics

5. CONCLUSION

An innovative design method IC in 130-nm BiCMOS technology operating as a LP-NGD function is developed. After the synthesis equation formulation, the LP-NGD BiCMOS chip design methodology is described in function of the technological requirement. The different design steps including the DRC and LVS consideration are described.

A PoC of RL-network based LP-NGD BiCMOS IC was considered for the feasibility study. The PoC circuit was designed with the smallest size LP-NGD circuit ever being done before. Frequency and time domain investigations were explored to verify the LP-NGD function validation. The obtained results show a LP-NGD behavior with -100 ps NGD value over cut-off frequency more than 1 GHz. In addition, extraordinary results showing an apparent time-advance with two different waveform test signals were discussed. For all the cases of study, it was emphasized that the obtained calculated and Cadence® electrical simulation results are in very good agreement.

The manufacturing process and test are scheduled as the next step of the present study. Moreover, the differences between the calculation and simulations will be investigated more deeply via the effect of the interconnect and parasitic components after parasitic elements extraction.

This feasibility study promises the LP-NGD circuit applications especially for the NGD equalization interconnect delay compensation [19-20].

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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