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Abstract—This paper presents the design and test results of a fourth-order and sixth-order 14-bit 2.2-MS/s sigma–delta analog-to-digital converter (ADC). The analog modulator and digital decimator sections were implemented in a 0.35-mm CMOS double-poly triple-level metal 3.3-V process. The design objective for these ADC's was to achieve 85 dB signal-to-noise distortion ratio (SNDR) with less than 200 mW power dissipation. Both modulators employ a cascade sigma–delta topology. The fourth-order modulator consists of two cascaded second-order stages which include 1-bit and 5-bit quantizers, respectively. The sixth-order modulator has a 2-2-2 cascade structure and 1-bit quantizer at the end of each stage. An oversampling ratio of 24 was selected to give the best SNDR and power consumption with realizable gain-matching requirements between the analog and digital sections.

Index Terms—Analog circuits, cascaded ADC architectures, hybrid A/D converters, mash ADC architectures, sigma–delta modulators, switched-capacitor circuits.

I. INTRODUCTION

MIXED-SIGNAL VLSI trends for high-resolution, low-power, broadband A/D and D/A conversion are being driven by the emerging internet telecommunications marketplace. Broadband digital subscriber loop (DSL) transceivers require 12–14 bit accuracy for 2.2-MHz sampling with less than 200 mW power dissipation.

To achieve 85 dB signal-to-noise distortion ratio (SNDR) and 200 mW power dissipation at 2.2-MHz sampling rates, low voltage CMOS hybrid sigma–delta A/D architectures are required. As CMOS technologies continue to scale in gate length, higher oversampling rates (OSR's) can be implemented in the sigma–delta digital decimators. This will yield higher SNDR at broadband frequencies [1]. However, as OSR's increase, analog integrator and digital decimator power consumption also increases.

For applications where power consumption is crucial, higher order sigma–delta modulators are used. However, a single-loop structure of an order higher than second shows stability problems due to the inherently linear one-bit quantization [12]. Good stability can be achieved by cascading several lower order

single-loop modulators. In a cascaded sigma–delta modulator, there is no accumulation of signals at the later stages. This is simply because the correlated quantization error from the first stage and the error(s) from the later stage(s), except the last one, are cancelled by the digital correction [12]. There have been several studies on cascaded sigma–delta ADC's. In [13], the authors implemented a stereo audio sigma–delta ADC, in which the converter was realized by two identical cascaded fourth-order sigma–delta modulators. Williams and Wooley presented a cascaded third-order sigma–delta modulator in which a second-order stage is followed by a first-order stage. This is the so-called 2-1 architecture and is preferred by the authors to alternative cascaded third-order architectures because it is less sensitive to component mismatch [11]. Yin and Sansen proposed a three-stage fourth-order topology which was implemented with fully differential switch-capacitor circuits and was manufactured in a BiCMOS process [12]. Also, recently, Geerts *et al.* used a 2-1-1 cascade topology for a very similar application in which the ADC's in this paper are intended [14].

Section II will describe the trade-offs between OSR's, number of bits in quantizer, and sigma–delta order, which need to be optimized for 85 dB SNDR and minimum power consumption and realizable implementation requirements.

Section III describes the linear system analysis for the switched-capacitor integrator. The circuits for the integrator operational amplifier and voltage reference are described in Section IV. Section V will discuss the detail design and implementation issues of the fourth-order and sixth-order ADC's. The gain matching requirement between the analog and digital decimator macros is presented. In addition, the common centroid layout technique for the capacitor array is discussed. Layout plots of the fourth-order and sixth-order ADC are also given. Experimental results from chip testing including SNDR, analog, and digital I_{cc} measurements are reported in Section VI.

II. SYSTEM ARCHITECURE

High-order quantization noise shaping with good stability can be achieved with cascaded sigma–delta architectures [2], [4]. Higher order noise shaping will result in reduced sampling rates for a given SNDR design objective, thus reducing power consumption. However, since extra digital logic is needed for this error bandwidth correction, this power savings is slightly diminished. Increasing the number of bits in the quantizer can also reduce in band quantization noise power thus increasing SNDR. However, gain matching between analog integrators and error correction logic become more critical as OSR is reduced. Fig. 1

Fig. 1. SNDR and power estimation for OSR $= 24$.

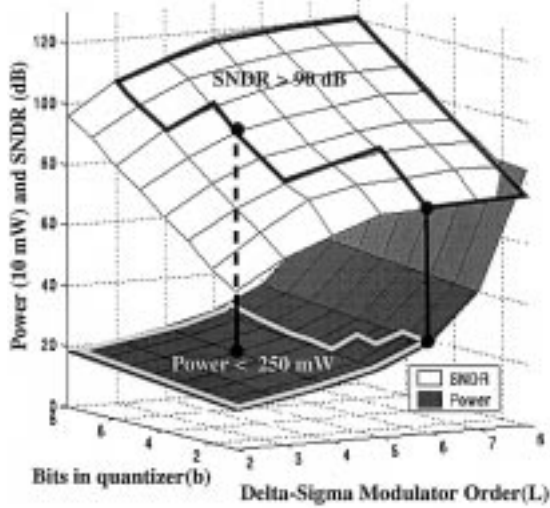

Fig. 2. Fourth-order modulator.

depicts a 3-D mesh plots showing SNDR and power dissipation for an OSR 24 ADC system. The power dissipation was estimated using separate analog and digital I_{cc} expressions. Analog I_{cc} was derived using scaled integrator gains and reduced capacitor sizes for a given integrator bandwidth. This is described below:

$$P_A \cong \sum L \times f(Int), \ g(comp_b), \ h(V_{\text{ref}}) \qquad (1)$$

where

L	modulator order which defines the number of integrator opamps;
$f(Int)$	estimate of the integrator opamp power consumption;
$g(compb)$	comparator power consumption;
$h(V_{\text{ref}})$	power.

Digital I_{cc} was derived using the CfV^2 expression [6] and is shown below:

$$P_D \cong \sum_{n=1,\,2,\,3} p_n C_n V^2 F_n. \qquad (2)$$

The load capacitance (C) is estimated based on the test results from a previous chip which utilized the same standard cell library for identical digital logic functions. Since there exist three clock domains, an OSR of 24 was selected to give the best SNDR with realizable gain matching requirements between the analog and digital sections which is described in more detail later on in this section.

The regions bounded by the 2-D contour plots for Power $<$ 200 mW and SNDR $>$ 90 dB will meet the design objectives of the ADC system. Hence, the 5-bit fourth-order ADC system and the 1-bit sixth-order ADC system were chosen as the topology to satisfy the SNDR and power consumption targets.

A. Cascaded Modulators with Error Correction

A cascaded sigma–delta modulators can achieve higher order noise shaping with reduced OSR. This is simply because, in cascaded structure, the sigma–delta modulator is not a single loop
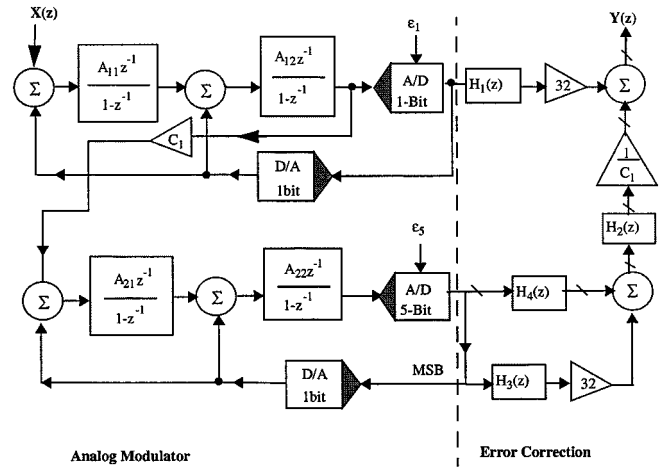
but a series of lower order single-loop modulators, each with its own quantizer. The output of the each single-loop is fed to the next stage where the quantization noise of the previous stage is corrected, hence at the final output we only have the quantization error of the last stage. However, due to integrator gain error, these corrections cannot be done 100%, which affects the resolution chosen for the quantizer in the next stage. In practical implementations, increasing the resolution of the multi-bit quantizer reduces the second-stage quantization error and increases the sensitivity to uncancelled quantization error from the first stage [5]. We adopted a similar approach for the fourth-order modulator and used a 5-bit quantizer in the second stage (see Fig. 2).

B. Fourth-Order 5-bit Analog Modulator

The fourth-order modulator shown in Fig. 2 consists of two cascaded second-order stages which include a 1-bit quantizer and 5-bit quantizer, respectively. This will result in fourth-order noise shaping with 5 bit quantization. The error correction stage will combine the 1-bit digital output from the first stage with 5-bit and 1-bit digital outputs from the second stage, to yield an output comprised of the input signal plus a fourth-order error term. Note that single bit feedback is used after the 5-bit quantizer, instead of 5-bit feedback which would require a precise 5-bit D/A converter. This scheme is also favored to avoid nonlinearity and gain matching issues related to higher bit D/A converters. Transfer functions for the error correction filters of the fourth-order system in Fig. 2 can be given as follows:

$$H_1(z) = k(A_1 A_2)z^{-2}\left(1 - k(1 - z^{-1})^2\right) \qquad (3)$$

$$H_2(z) = k(1 - z^{-1})^2 \qquad (4)$$

$$H_3(z) = 1 - k(1 - z^{-1})^2 \qquad (5)$$

$$H_4(z) = k(1 - z^{-1})^2 \qquad (6)$$

$$k = \frac{1}{1 + (A_2 - 2)z^{-1} + (A_1 A_2 - A_2 + 1)z^{-2}}. \qquad (7)$$

The overall system transfer function $Y(z)$ is below.

$$Y(z) = k^2 \left(X(z)(A_1 A_2)^2 z^{-4} + \frac{\varepsilon_5}{C_1}(1 - z^{-1})^4 \right). \qquad (8)$$
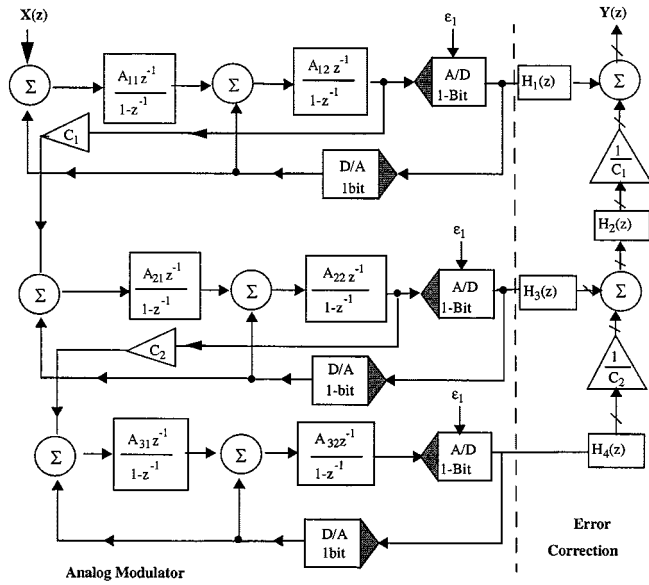
Fig. 3.   Sixth-order modulator.

Fig. 4.   SNDR versus amplitude plots.

Notice the 5-bit quantization noise error term, ε_5, with fourth-order noise shaping $(1 - z^{-1})^4$. This is the desired noise shaping required for this system transfer function. Following the error correction logic is a cascaded decimator section which includes a Sinc^5 filter and a 24-tap finite-impulse response (FIR) filter [4].

C. Sixth-Order 1-bit Analog Modulator

The sixth-order modulator consists of three cascaded second-order stages as shown in Fig. 3. This cascaded topology was chosen to take advantage of both the stability provided by its lower order sections and the sixth-order noise shaping of the overall system. The 1-bit digital outputs of each of the three stages are combined and digitally filtered to yield an output comprised of the input signal plus a sixth-order noise error term.

The sixth-order modulator structure is very similar to the fourth-order structure shown in Fig. 2. Likewise, the error correction filters in the sixth-order system have the same transfer functions as their counterparts in the fourth-order system with the exception of $H_1(z)$ and $H_3(z)$, which are modified as follows:

$$H_1(z) = k^2 (A_1 A_2)^2 z^{-4} \left(1 - k(1 - z^{-1})^2\right) \quad (9)$$

$$H_3(z) = k A_1 A_2 z^{-2} \left(1 - k(1 - z^{-1})^2\right). \quad (10)$$

The sixth-order system transfer function for $Y(z)$ is

$$Y(z) = k^3 \left(X(z)(A_1 A_2)^3 z^{-6} + \frac{\varepsilon_1}{C_1 C_2} (1 - z^{-1})^6 \right). \quad (11)$$

Notice the desired sixth-order noise shaping term for the 1 bit A/D quantization noise error, ε_1. Following the error correction logic is a cascaded decimator section which includes a Sinc^7 filter and a 24-tap FIR filter. Simulated ideal SNDR plots versus input amplitude for the ADC systems are shown in Fig. 4.

SNDR versus integrator gain error for fourth-order and sixth-order is shown in Fig. 7. An 84-dB SNDR target will require a
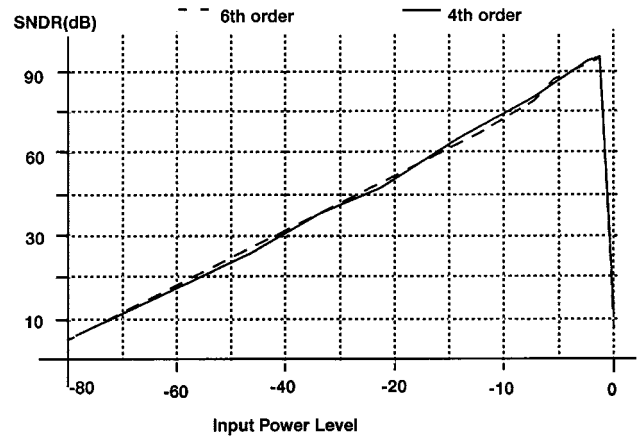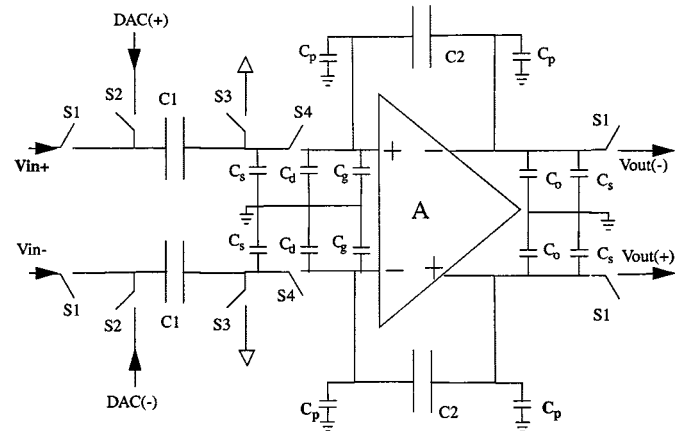
$\pm 0.8\%$ relative gain matching between analog integrators and the digital decimators which is physically realizable using the common centroid capacitor layout described in Section V.

Fig. 5.   Non-ideal switch capacitor integrator.

III. LINEAR MODEL OF INTEGRATOR

Switched-capacitor $\Sigma\Delta$ analog modulators use discrete time integrators to perform the integration of signal error required for noise shaping. The three key circuit components of the discrete time integrators are the electrical switches, gain capacitors and the operational transconductance amplifier (OTA). Due to the parasitics of the layout in a nonideal switch capacitor integrator system, the discrete time integrator contains a pole other than at the unit circle. When this occurs, the switch capacitor integrator becomes an digital filter rather than an integrator. Passive parasitics around the circuit integrator and nonideal circuit parameters of the OTA also make the ideal transfer function nonideal, hence, the name leaky integrator [6]. When we add the parasitics of wire capacitors to the common centroid layout, source drain capacitors of the switches and input and output capacitances of the OTA, our integrator model is shown in Fig. 5.

Using conservation of charge derivations in the time domain, system variables α, η, ν, and ρ can be derived as functions C_s, C_d, C_g, C_p, and C_o. Also, S1 and S3 are out of phase
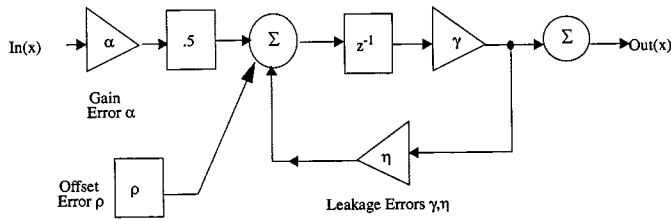
Fig. 6. Leaky integrator parasitic model.

clocks with respect to S2 and S4. These system variables for the leaky integrator are

$$\eta = 1 + \frac{C_g + C_d}{C_2(1+A)} \tag{12}$$

$$\gamma = \left(1 + \frac{(C_1 + C_s + C_g + C_d)}{C_2(1+A)}\right)^{-1} \tag{13}$$

$$\alpha = \frac{C_1}{C_2}\left(\frac{A}{1+A}\right) \tag{14}$$

$$\rho = \frac{C_1}{C_2}\left(\frac{A}{1+A}\right)\left(1 + \frac{C_s}{C_1}\right). \tag{15}$$

The γ and η feedforward and feedback parameters set the pole and zero of the switch capacitor integrator. Note η is >1 and $\gamma < 1$. The α parameter is considered the gain error of the switch capacitor integrator [5], [6]. The ρ parameter is analogous to a filtered dc offset. If this dc offset resides in the range of the OTA, it should not create a problem with respect to SNDR, only the input range. Thus, a sensitivity analysis with respect to the ρ parameter is not performed. In addition, all ADC gain parameters—namely A_{11}, through A_{33}, C_1, C_2—were set to 0.5 so that a unit capacitor based centroid capacitor layout could be used. Thus, the ratio of $C_2/C_1 = 0.5$. The linear model for the leaky integrator is shown in Fig. 6.

The transfer function of the leaky integrator is

$$H_{\text{Leaky}}(z) = \frac{\gamma z^{-1}(\alpha + 2\rho z)}{2(1 - \gamma\eta z^{-1})}. \tag{16}$$

The folded cascoded integrator used in the fourth-order and sixth-order ADC's had a slew rate of 475 V/μs, bandwidth of 1 GHz and dc gain of 58 dB. For the extracted layout of the integrator, $C_2 = 2.64\,\text{pF}$, $C_1 = 1.32\,\text{pF}$, $C_o = 8\,\text{pF}$, $C_g = 3.2\,\text{pF}$, $C_p = 0.01\,\text{pF}$, $C_s = C_d = 0.4\,\text{pF}$. Thus, $\eta = 1.00$, $\gamma = 0.99$, and $\alpha = 0.5$ and $\rho = 0.65$. These system parameters found in the $H_{\text{Leaky}}(z)$ transfer function were simulated in Matlab for the fourth-order and sixth-order systems. Each parameter was individually altered and SNDR was recalculated for each increment. Sensitivity of SNDR data with respect to each of the system parameters were empirically extracted from the SNDR curves. In Figs. 7 and 8, the SNDR data is presented for the fourth-order and sixth-order ADC simulations.

In Table I, the SNDR sensitivity is summarized with respect to the system parameters for a -6 and -12 dB attenuation from peak SNDR. This data was extracted from the graph data in Fig. 7. The system parameters α, γ, η are in percentages and the gain parameter A is in dB.

Thus, for the cascaded sixth-order ADC with OSR of 24, a 3% ($|-1.5|\% +1.5\%$) variation range of gain error (α) will re-
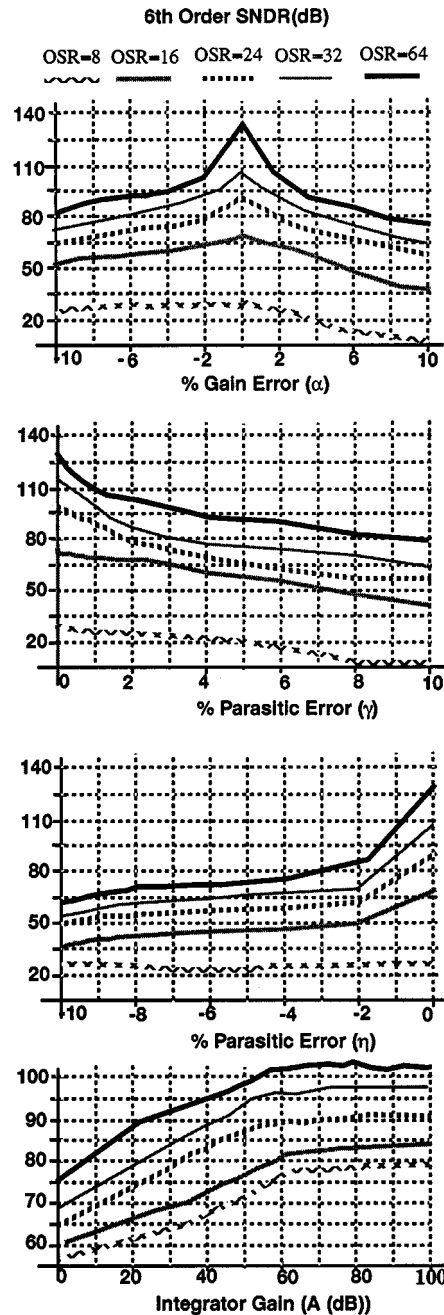
Fig. 7. SNDR sensitivity for sixth-order.

duce peak SNDR by -6 dB and a 5% ($|-3|\% +2\%$) variation range of gain error will reduce peak SNDR by -12 dB. Similarly, for the fourth-order ADC, 3 and 5% variation ranges of gain error will reduce peak SNDR -6 and -12 dB, respectively. This sensitivity data shows a trend that the smaller the OSR rate becomes, the more sensitive the modulator becomes with respect to the leaky integrator system parameters.

IV. ANALOG CIRCUIT IMPLEMENATION

Two important analog macros used in the fourth-order and sixth-order sigma–delta ADC's are the integrator OTA and the voltage reference circuits. The details of designing these circuits are described in Section IV-A and B, respectively.

Fig. 8.   SNDR sensitivity for fourth-order.

TABLE I
-6 dB$|-12$ dB SNDR Sensitivity

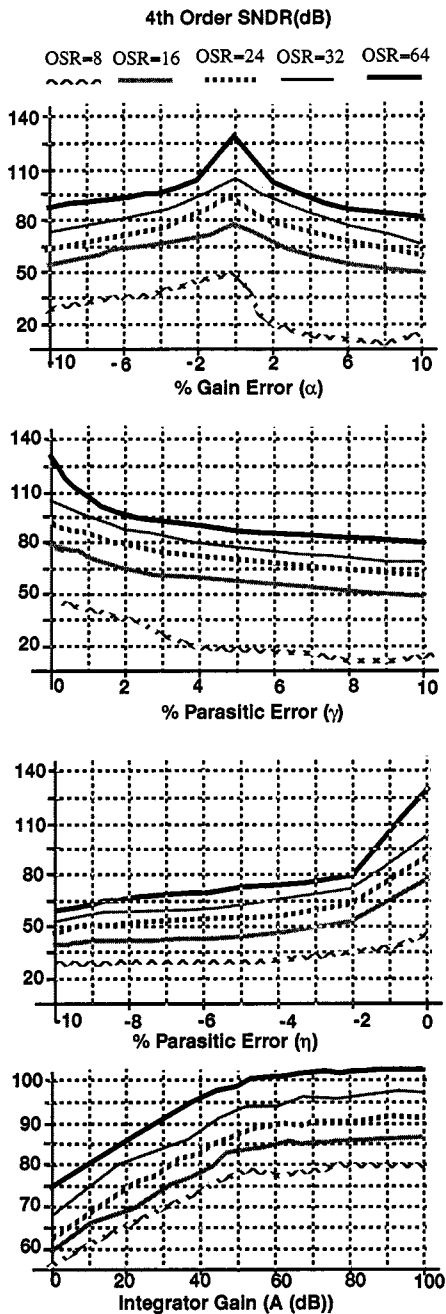| 6th Order, 1-Bit	OSR				
System Parameters	8	16	24	32	64
% α (Gain Error)	3|6	2|4	1|4	1|4	.5|1.5
% γ (Parasitic Error)	4|6	3|5	1.3|3	.7|1.5	.3|.8
% η (Parasitic Error)	5|20+	1|2	.8|1.6	.5|1	.4|1
A (OTA dc Gain)	1|16	2|18	2|18	2|19	4|10
4th Order, 5-Bit	OSR				
System Parameters	8	16	24	32	64
% α (Gain Error)	.1|.4	1|2	.4|1	.3|.9	.2|.7
% γ (Parasitic Error)	.4|1	.6|2	1.3|3	1.4|3	.4|1
% η (Parasitic Error)	.4|1	.6|.9	.6|.9	.6|.8	.2|.6
A (OTA dc Gain)	2|7	2|8	2|8	2|8	3|9
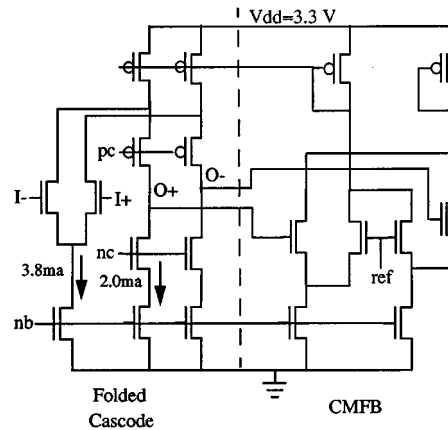
Fig. 9.   Folded cascode opamp.
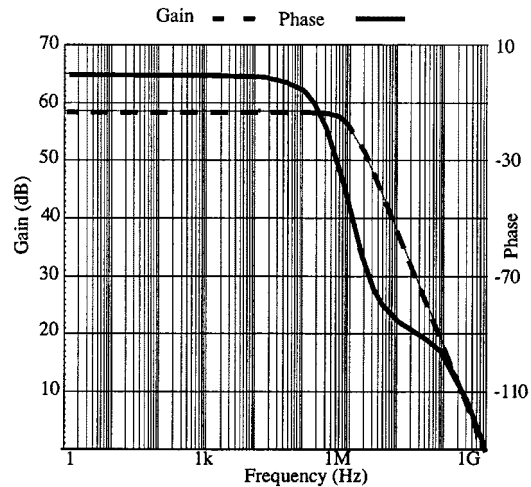
Fig. 10.   Bode plot for integrator OTA.

A. Integrator Amplifier

The switched-capacitor integrators in the sigma–delta ADC require very high switching speeds which presented a design challenge for the analog circuitry. To achieve the high speed necessary for the OTA, a fully differential folded cascode amplifier topology was implemented (see Fig. 9). Another requirement, due to the ADC architecture, was that the amplifiers had to be fully differential with a differential input signal swing of 1.1-V peak-to-peak. The OTA also featured a continuous-time common mode feedback (CMFB) circuit which is used to maintain the desired level at the output. To achieve the high speed needed, power consumption was sacrificed. The tail current through the differential pair was 3.8

mA while the currents through each leg of the cascodes was 2 mA. The total current for the amplifier circuit was about 8mA including the CMFB circuitry.

Simulation results show a dc gain of 60 dB with a unity gain frequency of 820 MHz. The phase margin measures 40° and the slew rate is 475 V/μs. Amplifier simulations were run using a 1.8-pF load.

The bode plot from Hspice simulations of the folded cascode amplifier is shown in Fig. 10.

Fig. 11. Common centroid capacitor layout for the switch cap integrator.

B. Voltage Reference Buffer

The critical design issue for the sigma–delta reference buffer amplifiers was the slew rate. Given the architecture, the amplifiers needed to account for digital switching current spikes of 850 μA every clock cycle on their outputs. In order to recover from these current spikes, the slew rate necessary for this particular application, was calculated to be 375 V/μs.

Using one amplifier topology for all three references was desired but proved unfeasible with the large difference in reference levels. The amplifier topology selected was the standard two-stage CMOS amplifier without an output stage. The amplifiers supplying the V_{ref} and $V_{\text{ref}}(-)$ levels were pMOS differential input pair OTA's while the reference amplifier supplying the $V_{\text{ref}}(+)$ level was an nMOS differential input pair OTA. Using these two amplifiers guaranteed all devices would remain in saturation given large voltage spikes feeding back into the outputs.

Both OTA's were designed with 400 μA tail currents and used simple frequency compensation. The dc gain of both amplifiers was 90 dB with a 72° phase margin. The slew rates were over 400 V/μ while driving a 10 pF load.

V. Layout Considerations

One important design criteria requires us to have a capacitance ratio of 2.0 with 0.8% accuracy between the feedback capacitor (O) and the input capacitor (X) in the switched-capacitor integrator circuit. To accomplish this requirement and to eradicate all fabrication inaccuracies up to 0.8%, the layout is drawn in a common centroid fashion [9]–[11]. The capacitors are split into four and two equal parts, respectively for the capacitor O and the capacitor X, that are connected in parallel. A unit capacitor size of 330 fF was selected so that the kT/C thermal noise was not an issue, and fabrication process variations are below the 0.8% tolerance. Hence, capacitor O has a capacitance of 4×330 fF $= 1320$ fF or 1.32 pF, and likewise capacitor X has a capacitance of 2×330 fF $= 660$ fF or 0.66 pF. To avoid coupling capacitances and preserve common mode rejection, connections are drawn in such away that the electrodes of the two capacitors are separated from each other. A portion of the layout of the integrator capacitor is shown in Fig. 11.

Two rings of dummy capacitors were placed around the periphery as recommended in [8] and [10]. This horizontal dimen-
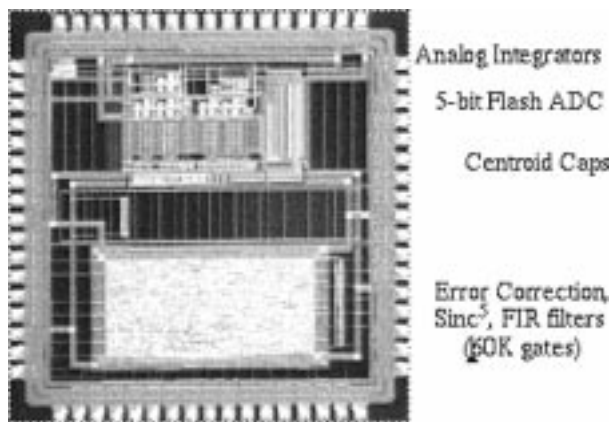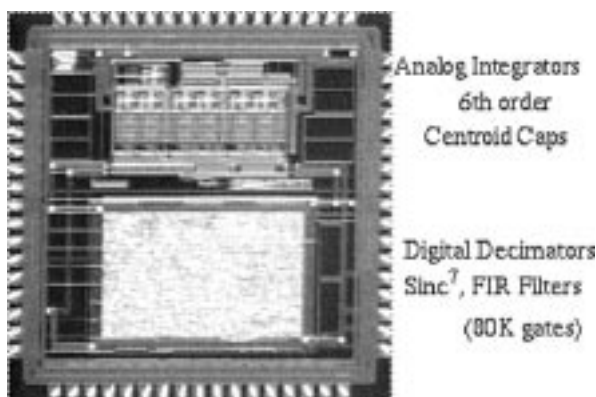

Fig. 12. Fourth-order die photo.

Fig. 13. Sixth-order die photo.

sion of this array of capacitors is 105 mm which matches the width dimension of single switch capacitor integrator.

This enabled the array to be placed directly above each switch capacitor integrator in the modulator floorplan. Also, differential signal routing between each unit capacitor was preserved which connected the analog signals from the OTA to the electrical switches. The layout of the electrical switches S1–S4 were place above the capacitor array.

The die photos for the fourth order and sixth order are shown in Figs. 12 and 13, respectively.

The digital area for the error correction and decimation filter for the fourth-order ADC is 2.3 mm^2 while the analog section area is 1.3 mm^2. The digital and analog area in the sixth order are 2.6 and 1.7 mm^2, respectively.

A. Evaluation Results

An eight-layer custom-printed circuit board was designed to evaluate the fourth-order and sixth-order devices. High Q bandpass filters tuned for 1.1 MHz, 500 kHz, and 110 kHz were used to enable the >95 dB SNDR required for input signal quality. The layout of this evaluation board was carefully designed for analog signal and power isolation with respect to digital signal and analog power. Termination and shielding of all digital clock I/O pins were implemented. Since the I/O signal names of the fourth order were identical to the sixth order, a single ZIF socket was needed for both ADC's, hence one board was required.
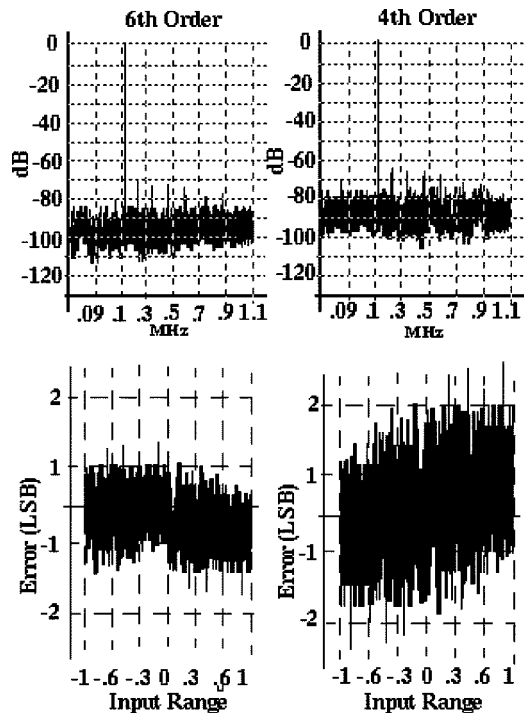
Fig. 14.   Spectral and DNL test data of fourth-order and sixth-order ADC's.

VI. CONCLUSION

In this paper we have presented the design and test results of a fourth-order and sixth-order 2.2-MS/s 14-bit sigma–delta ADC's. Both ADC's use a cascaded architecture consisting of second-order stages which employ 1-bit quantizers, except the second stage of the fourth order which has a 5-bit quantizer at the end. The SNDR sensitivity phenomenon for the fourth-order and sixth-order ADC's are also investigated. Circuit parameters of the switched-capacitor integrators such as amplifier open loop gain, integrator gain, amplifier offsets, and layout parasitics were quantified. Simulation data are presented and quantified to show percentage dependencies for that particular parameter. Measured test results show that the sixth-order ADC performs much better in terms of SNR with a tradeoff of more area and power consumption. Further power and area reductions of 15% and 20% respectively can be achieved in the digital section if a full custom design methodology is utilized to replace the standard cells for FIR memory and multiply/accumulate macros. Further reduction in digital logic of 10% can occur by reducing the output bit lengths of the Multiply and Accumulate (MAC) and FIR logic. Currently, data bus lengths in the FIR filter output stages were designed for 15 bits precision, which can be reduced to 14 bits.

TABLE II
MEASURED TEST RESULTS

Item	4th Order	6th Order
SNDR	72 dB	79 dB
SNR	81 dB	86 dB
DNL	+/.5 LSB	+/-.3 LSB
INL	+/-.66 LSB	+/-.5 LSB
THD	- 87 dB	- 89 dB
Differential Range	1.0 V	1.2 V
ENOB	12 Bits	13 Bits
Intermod Interference	- 75 dB	- 76 dB
Analog Icc @ 3.0v	33 ma	50 ma
Digital Icc @ 2.5v	35 ma	39 ma
Total Power Dissipation	187 mW	248 mW
Total Macro Area	3.6 mm^2	4.3 mm^2

Fig. 14 shows the spectral data output and DNL data across the input range for the sixth-order and the fourth-order ADC's.

Experimental measured results for each ADC system are summarized in Table II.

The digital and analog I_{cc} was measured at 52.5-MHz clock rate which is OSR of 24 multiplied by the 2.2-MHz Nyquist Rate. All other measurements were taken using a 2.2-MHz sampling rate for a 1.1-MHz band-limited input. The results in Table II are given for an input sine wave of 110 kHz. Peak-to-peak jitter on clock source is measured as less than 20 ps. A 240-mV correlated noise level is measured on the voltage reference signals, namely $V_{ref}(p)$, $V_{ref}(n)$ and V_{ref}—causing an estimated −8 dB degradation in the SNDR and signal-to-noise ratio (SNR). This noise is being triggered off the digital output clock and further characterization is still required to understand the substrate noise effects.

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