15 kV SiC MOSFET: An Enabling Technology for Medium Voltage Solid State Transformers

Alex Q. Huang, Qianlai Zhu, Li Wang, and Liqi Zhang

***Abstract*—Due to much higher achievable blocking voltage and faster switching speed, power devices based on wide bandgap (WBG) silicon carbide (SiC) material are ideal for medium voltage (MV) power electronics applications. For example, a 15 kV SiC MOSFET allows a simple and efficient two-level converter configuration for a 7.2 kV solid state transformer (SST) for smart grid applications. Compared with multilevel input series and output parallel (ISOP) solution, this approach offers higher efficiency and reliability, reduced system weight and cost by operating at medium to high switching frequency. However, the main concern is how to precisely implement this device in different MV applications, achieving highest switching frequency while maintaining good thermal performance. This paper reviews the characteristics of 15 kV SiC MOSFET and offers a comprehensive guideline of implementing this device in practical MV power conversion scenarios such as AC-DC, DC-DC and AC-AC in terms of topology selection, loss optimization and thermal management.**

***Index Terms*—15 kV SiC MOSFET, efficiency, medium voltage, medium voltage power electronics, reliability, solid state transformer, smart transformer.**

I. Introduction

As a new and emerging application of medium voltage (MV, 2 kV-35 kV) power electronics, the Solid State Transformer (SST) is very attractive in smart grid, traction drive and renewable energy systems [1]-[4] due to its benefits in size and weight reductions, as well as a number of smart functionalities such as reactive power compensation. The basic concept of the SST is to use a Medium Frequency (MF) (several kHz to tens of kHz) power converter to replace a traditional Line Frequency (LF) power transformers (LFT). Comparing to LFTs, SSTs can achieve higher power density while potentially offering many smart features such as Var compensations, voltage regulation, fault isolation and DC link [1]-[4].

The basic operational principle of the SST is as follows:

1) Change the 50/60 Hz MV ac voltage to a MF voltage.

2) Step up/down this MF voltage through a MF transformer.

3) Reshape the MF waveform back to 50/60 Hz voltage.

One grand challenge for the SST is to achieve MV input voltage such as 7.2 kVac in single phase smart grid application in United States. No commercial power devices are currently available to handle the associated peak voltage stress. Modular multilevel configurations based on input series and output parallel (ISOP) are widely used to address this issue in which low voltage converters are connected in series to share the voltage and power [5]-[13]. To avoid power and voltage balancing problems, additional balancing circuits and control strategies are needed [14]. The resulting SST is therefore typically very complex due to the complex system configuration, protection and control schemes, numerous gate drivers and isolated power supplies. System reliability is low if redundancy is not carefully considered.

Ultimate solutions for MV power electronics can be more elegantly achieved if MV power devices can be developed to cover the wide spectrum of MV voltages (2 kV-35 kV). Up to now, silicon power devices such as Si IGBT are the only available device for MV applications but the maximum blocking voltage of the IGBT is limited to 6.5 kV due to substantially increased losses if designed for even higher voltages. On the other hand, due to the significantly increased peak electric field strength in WBG materials such as SiC, SiC power devices with much higher blocking voltage have been developed and demonstrated. The blocking voltage demonstrated ranges from 10 kV to 24 kV with three terminal device concepts based on unipolar (i.e. SiC MOSFET) and bipolar (i.e. SiC IGBT/ETO) conduction mechanisms [15]-[18]. Although not yet commercially available, they can enable a simpler and robust two-level SST in 7.2 kV applications where the peak voltage stress is less than 12 kV. SST based on high voltage SiC power devices is therefore a very attractive technical approach. With two-level configuration, the system complexity and control scheme can be much simplified. Therefore, higher reliability and efficiency can be obtained. In addition to the improvements in voltage ratings, the switching speed of these devices is also significantly faster than commercially available 6.5 kV Si IGBTs hence allowing the SST to operate at higher switching frequency. Higher operation frequency enables volume reduction of the MF transformers, inductors and capacitors so that higher power density and light weight can be obtained.

Varies power conversion topologies and applications of the SST have been discussed in literatures [5]-[13]. Many well-known MV SST designs are depicted in Fig. 1, including designs by Alstom [5], Bombardier [6], UNIFLEX [7], ABB PETT [8], GE Global Research [10], EPRI [9], ETH [11] and the FREEDM System Center [12], [13], [19].

From power conversion point of view, there are basically

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The authors are with FREEDM Systems Center, North Carolina State University, Raleigh, US (e-mail: aqhuang@ncsu.edu).

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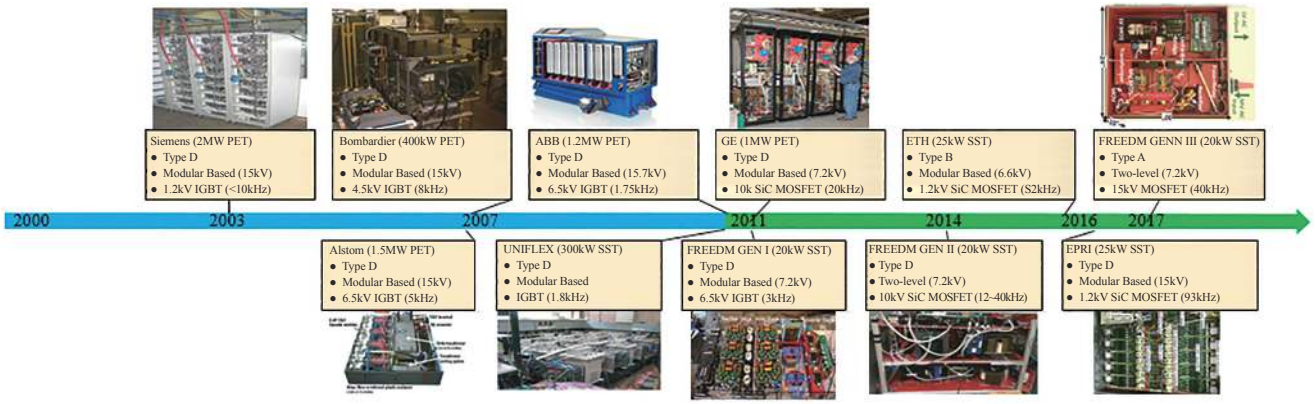

Fig. 1. MV prototypes developed by leading research groups.

four topology approaches to form a SST as shown in Fig. 2. Type D is the most widely used approach since it can achieve most of the smart features that a smart transformer desires. It contains three conversion stages: a rectifier stage that offers power factor correction and reactive power capability; a second DC-DC stage with galvanic isolation and voltage step-down and a third low voltage (LV) inverter stage that reshapes the DC voltage back into a desired AC voltage. The efficiency of Type D SSTs is lower because of the three stages of power conversion, and two of them are MV converters.

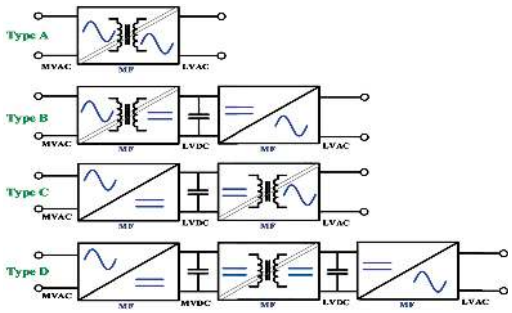

Fig. 2. SST topology classification.

Type A topology is very attractive since the power conversion stages are reduced, which enables better efficiency and higher reliability. Due to these benefits, several efforts on Type A SST have been carried out [11], [29], [34]. In Type A SST, the MV device will experience a wide voltage range, from 0 to 10 kV during one line frequency cycle in case of a 7.2 kVac input. Achieving ZVS under such wide voltage range and load conditions becomes very difficult.

In the SSTs, the MV devices may encounter totally different operation conditions. The AC-DC stage of the Type D SST normally operates under hard switching condition, which limits the switching frequency under 10 kHz due to the large amount of switching losses even if SiC MOSFET is used [13], [28]. While in the DC-DC stage, ZVS can be easily achieved and it enables a substantial reduction of the switching loss. Hence the switching frequency can be much higher [19], [20]. Type A SST is basically an isolated direct AC-AC converter and the MV devices may operate under hard switching condition. In this case, both switching and conduction losses exist, an optimal design that achieves minimum overall loss is needed. Transformer loss optimization must also be part of this optimization process. On the other hand, Type A SST with ZVS capability will be very desirable to reduce or eliminate the switching loss hence the switching frequency can be substantially increased.

Many previous papers focus on topology, passive components and control design. Only a few papers focus on the MV device utilization issue in MV and MF applications. This paper provides a comprehensive review of the 15 kV SiC MOSFET characteristics as well as a comprehensive design guideline for utilizing its full switching frequency and power potential in MV AC-DC, DC-DC, AC-AC applications.

The paper is structured into five sections. Section II gives a comprehensive overview of the salient characteristics of 15 kV SiC MOSFET. In the Section III, the frequency vs. power handling capability of the 15 kV SiC MOSFET in AC-DC, DC-DC and AC-AC are fully investigated. Some of the experimental results from the author's group are presented to verify the design. Some conclusions will be drawn in the final section.

II. 15 kV SiC MOSFETs

Due to almost ten times higher peak electric field strength in SiC when compared to Si, SiC power devices with much higher blocking voltages such as the 15 kV SiC MOSFETs have been developed and demonstrated [13], [14]. Since the device operates as a unipolar conduction device, its switching speed is also very fast. As a comparison, Si power MOSFETs are typically designed with a blocking voltage less than 1200 V. So achieving ultra high blocking voltage is a direct benefit of SiC power devices.

The 15 kV SiC MOSFET prototype developed by Wolfspeed uses a DMOS device structure and the device is packaged with a single side cooling capability as shown in Fig. 3 [35]. The chip size has a dimension of 8.1 mm×8.1 mm in which 5.95 mm×5.95 mm is the active area that conducts current. To Implement this device in MV applications, ac-

curate device conduction loss, switching loss and thermal models need to be developed.

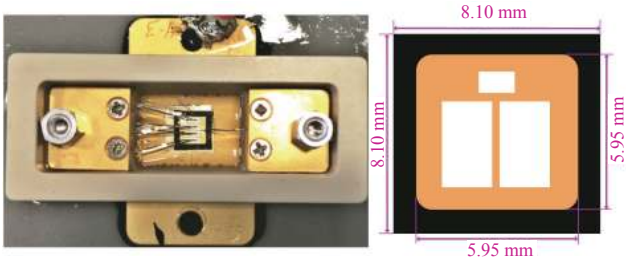

Fig. 3. 15 kV SiC MOSFET (a) packaged module (b) die dimension [35].

A. On-Resistance Model

The measured and modeled conduction resistance of the device at 20V gate to source voltage are shown in Fig. 4. The room temperature on-resistance is around 0.875 Ω, and the corresponding specific on-resistance is 309 mohm-cm^2. This value is very close to the theoretical capability of 15 kV SiC MOSFET. In the future, superjunction SiC MOSFET can be developed that can lower this resistance substantially.

SiC MOSFET on-resistance increases quickly with the increase of the junction temperature as shown in Fig. 4. The measured result can be represent by a Ron model [19]

$$R_{on} = R_0(\frac{T_j}{T_0})^{3.5} \tag{1}$$

where R_0=0.875 Ω, T_0=348.16 K.

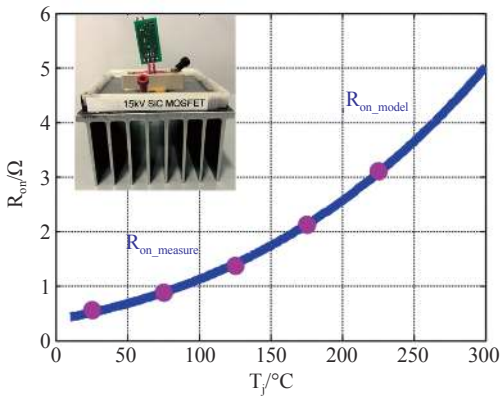

Fig. 4. On-state resistance of the 15 kV SiC MOSFET modules [19].

Increased Ron at high temperature is a typical behavior of all unipolar power devices such as the MOSFET, but the rate of increase for the 15 kV device is substantially higher than 1200 V SiC MOSFET. This is due to the fact that the 15 kV device on resistance is dominated by the drift layer resistance. Due to the large on resistance, a single chip MOSFET is only capable to operate under relative low current conditions due to the high conduction loss. Ideal applications will be those requiring high voltage and low current, such as a single phase SST in the range of 10 to 50 kVA. For high power applications, many MOSFET chips can be paralleled to form a MOSFET module. In paper [10], 12 dies of 10 kV/10 A MOSFETs are paralleled to form a single 10 kV 120 A switch.

B. Switching Loss Model

The SiC MOSFET has very fast switching speed because it is a unipolar switch with no current tail. The switching time is determined by load condition and the device parasitic capacitance. The switching time is typically less than 500 ns as shown in Fig. 6, in which the dynamic turn-on and turn-off waveforms under 8 kV/8 A conditions are shown. However, this high switching speed does not directly translate to high switching frequency. In MV applications, the energies stored in the output capacitance of the devices is extremely high, which will result in large turn-on loss if the stored energies are not carefully recovered. An accurate Q_{oss} and E_{oss} model is critical for converter design.

Turn-on Loss: In a typical bridge configuration, the minimum turn on energy under hard switching condition is the energy stored in the output capacitance of the device as well as that in the freewheeling diode. Additional turn-on loss occurs due to the controlled dI/dt and dV/dt which results in a large voltage and current overlap during the turn-on, as shown in Fig. 5.

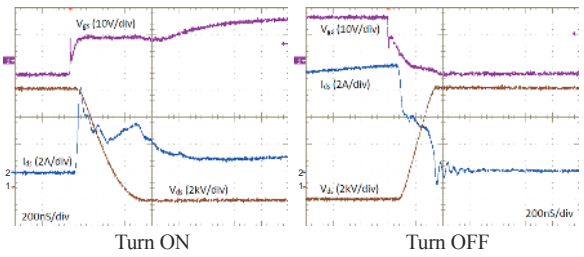

Fig. 5. Turn on and turn off waveforms under 8 kV /8 A condition.

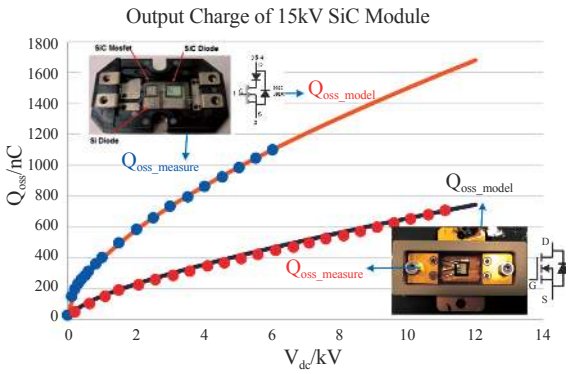

Fig. 6. Output charge of 15 kV SiC MOSFET modules.

The output charge Q_{oss} of the 15 kV MOSFET, hence the associated loss E_{oss}, can be accurately measured with a novel method proposed in [23]. The measured and modeled output charge of the 15 kV MOSFET in two different package are plotted in Fig. 6.

The Q_{oss} model equation is expressed as

$$Q_{oss\_single}(V_{ds}) = 4.08\sqrt{V_{ds}} + 24.8 \cdot V_{ds} \quad (2)$$

for the packaged 15 kV SiC MOSFET prototype device. If the associated energy E_{oss} is directly released to the device during the hard turn on, it will result in a substantial turn on loss. The measured E_{on} loss, which include E_{oss} as well as the voltage and current overlap loss, is shown in Fig. 7.

Turn-off Loss: Since the load current for the 15 kV MOSFET is low, the turn-off process is dominated by the charging of the output capacitance of the MOSFET as well as the discharge of the associated freewheeling diode and load parasitic capacitance. This is clearly shown in Fig. 5. This process is almost lossless (E_{off}=0) since the energy is simply stored in the output capacitance and stored energy is E_{oss}. Hence the turn-off loss of the 15 kV SiC MOSFET can be modeled as zero. Similar situation can also happen in lower voltage SiC MOSFETs if the turn-off process is dominated by the load current determined charging of C_{oss} of the switch, the freewheeling diode and the load parasitic capacitance [38].

The measured E_{on} and E_{off} at 4 kV condition are shown in Fig. 7 when compared with a 6.5 kV Si IGBT under similar test condition. The E_{on} loss shown includes the E_{oss} loss as well as the voltage and current overlap loss which has a strong dependence on the gate driving condition or R_g value.

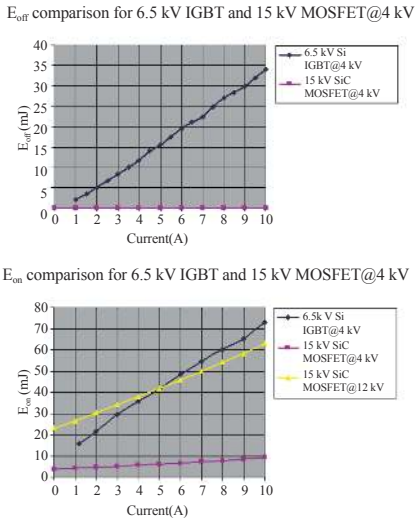

Fig. 7. The E_{on} and E_{off} of the 15 kV SiC MOSFET [22].

Compared with the IGBT, the SiC MOSFET shows a much lower total loss. This overall lower switching loss enables higher switching frequency in MV converters under hard switching conditions, leading to smaller system volume and higher power density. Hard switching based AC-DC converter based the 15 kV MOSFET has been reported in [28] which has a switching frequency of 6 kHz and a DC link voltage of 6 kV.

If the DC link voltage increases to 12 kV, the E_{off} loss remains close to zero while the E_{on} loss increases substantially, as shown in Fig. 7. This will limit the maximum switching frequency if the MOSFET operates in hard switching condition.

ZVS Turn-on: The switching frequency can be increased by recycling the output charge energy E_{oss} back to the load and/or source through the well-known zero voltage switching (ZVS) technique. The basic idea is to use the inductive energy stored in an inductor to discharge the C_{oss} of the device during the deadtime. A minimum amount of current is needed in the inductor and a typical ZVS criteria is shown in (3) where $Q_{oss}(V_{ds})$ corresponds to the charge in the C_{oss} of the device prior to the discharge.

$$I_{off}(\mathrm{V}_{ds})t_{dead} \geq Q_{oss}(V_{ds}) \quad (3)$$

If ZVS can be achieved, then the total switching loss of the device is almost zero. Theoretically then no switching frequency limitation exists. In practice, the switching frequency will be limited by the performance of the magnetic components, as well as the timing required to discharge the C_{oss}. In summary, with a combination of intrinsic capability (unipolar device vs. bipolar device) and circuit technique (ZVS vs. hard switching), the unique opportunity with the 15 SiC MOSFET can be summarized as a significantly increased operational Voltage×Frequency figure of merit (FOM) when compared with Si IGBT. This FOM is directly related to the MV converter performance. The higher the FOM, the better. The 15 kV SiC MOSFET device can achieve a FOM several hundred times higher than MV Si IGBT power devices. For example, the author's group have already achieved steady operation of the 15 kV SiC MOSFET at 40 kHz under 10 kV/ 20 kW condition [39] hence the FOM number is 400 MHz-Volt. Additional analysis shown in this paper (see Fig. 23) suggest that operation beyond 100 kHz is also feasible hence the FOM can reach more than 1 GHz-Volt, which is 200 times higher than the typical 5 MHz-Volt capability of a Si IGBT device. Fig. 8 shows the achieved FOMs for a number of power devices.

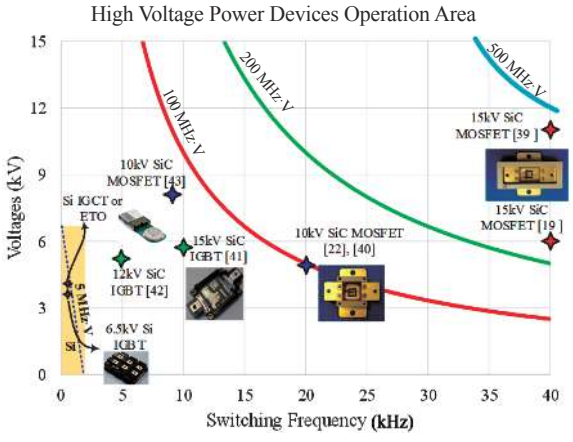

Fig. 8. The MV SiC MOSFET's Voltage×Frequency capability in comparison with Si high power devices such as IGBT/IGCT/ETO.

C. Paralleled JBS Diode

The 15 kV SiC MOSFET has an integrated body diode

that can be used as the freewheeling diode in converter applications. Applying a positive gate voltage will enable the MOSFET to operate as a synchronous rectifier. This capability is a directly advantage of the MOSFET when compared with an IGBT which must have a paralleled freewheeling diode.

However, there may be a need to connect a separate SiC JBS diode with the 15 kV SiC MOSFET for several reasons. The body diode of the 15 kV SiC MOSFET does not turn on until a forward voltage higher than 3.2 V. This higher forward drop will result in higher conduction loss. Applying a gate voltage to operate it as a synchronous rectifier can lower the conduction loss to the same level as that of the forward direction with a resistance shown in Fig. 4. This strategy can only happen after the deadtime period. Another important reason is the poorer diode reverse recovery performance associated with the SiC PN junction diode if substantial carriers are injected by the PN junction. The forward conduction of the PN junction may also cause significantly device degradation (loss of the forward blocking capability and/or increase of the R_{on}) [24], [25]. Many research on this degradation has been conducted with several literatures indicate that the issue has been largely solved in 1200V SiC MOSFET. For the tested 15 kV SiC MOSFET, however, there is a significantly degradation observed if the body diode conducts.

For above reasons, the 15 kV SiC MOSFET prototype device should be used without the body diode conduction. One strategy is to have low voltage silicon diode connected in series with the MOSFET to prevent the body diode from conducting, while a 15 kV SiC JBS diode is placed in parallel to conduct the reverse current (see Fig. 9). These two add-on devices may affect the device performance as well as system designs. The upper curve in Fig. 6 shows the output charge of the device up to 12 kV with a paralleled JBS diode, which has a significantly higher Q_{oss} than the MOSFET alone (lower curve). The Q_{oss} model for the MOSFET+JBS is derived as

$$Q_{oss\_combine}(V_{ds}) = 11.43\sqrt{V_{ds}} + 36 \cdot V_{ds} \qquad (4)$$

At 11 kV, the Q_{oss} of the SiC MOSFET alone is around 700 nC, while the output charge of the JBS diode is around 900 nC at this point. The test result indicates that the output charge in the JBS diode is even larger than that in MOSFET. In hard switching conditions, the added output charge will increase the hard switching E_{on} loss. In ZVS converter, larger output charge requires higher turn off current or longer deadtime, either way it will result in higher conduction loss for the system.

However, in a well-designed ZVS DC-DC or AC-AC converter, as will be mentioned in this paper, body diode conduction of the MOSFET can be avoided. So that the anti-paralleled SiC JBS diode can be eliminated. This will lower the semiconductor cost and improve the system power density.

D. Thermal Model

In this paper, the 15 kV SiC module is mounted on a heatsink without fan (see Fig. 4), which has a measured junction to air thermal resistance of 1.5 °C/W. Junction temperature is calculated based on this thermal resistance to predict the converter capability. If a better cooling system such as forced air or forced water is adopted, the thermal resistance will be much lower and even higher power handling capability can be obtained in the discussed converters.

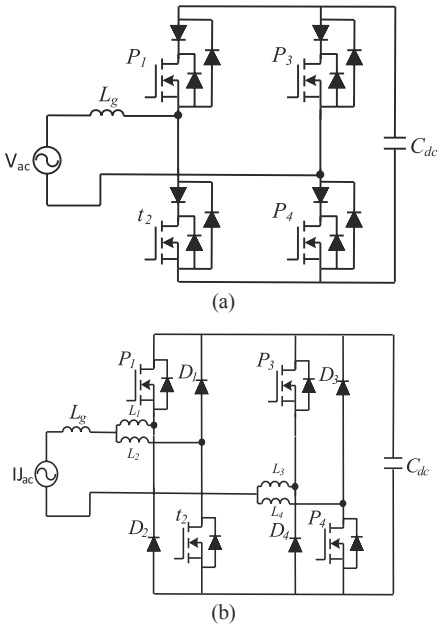

Fig. 9. AC-DC topologies: (a) Full bridge based (b) Dual buck based.

III. MV Converter Implementation Using 15 kV SiC MOSFETs

In different implementations, the MV devices may encounter totally different operation scenarios. Therefore it is important to understand the MV device's capability in terms of power handling capability in practical MV applications according to the unique applications features and requirements. AC-DC, DC-DC and AC-AC are the three main conditions the 15 kV SiC MOSFETs will encounter in MV applications.

A. AC-DC Applications

AC-DC stage normally acts as the input stage for a Type D SST and offers power factor correction and reactive power functionalities. Fig. 9(a) shows a typical bridge type AC-DC circuit that is widely adopted in MV applications. The MV devices operate under hard switching condition in this stage. As mentioned previously, a series connected Si diode and a SiC JBS diode are used with the MOSFET to prevent the body diode conduction [21], [22]. In hard switching conditions, the output charge of the device is directly released to the device during turn on. These amount of energy is large in MV applications, which will therefore limit the switching frequency of this stage. A design example of a MV AC-DC converter based on the 15 kV SiC MOSFET is shown in

[13] and the switching frequency is 6 kHz at 3.6 kV input voltage/V_{dc}=6 kV. The measured efficiency and calculated efficiency are shown in Fig. 10. Loss breakdown at V_{dc}= 6 kVdc and 12 kVdc are also shown in Fig. 10 to highlight the significantly increased switching loss at higher DC link voltages. Fig. 11 shows the predicted junction temperature of the 15 kV SiC MOSFET versus dc voltage and switching frequency in hard switching AC-DC converters. The results indicate that the switching frequency and power handling capability of the device in hard switching conditions. The results show that switching loss dominant the total loss and increases significantly as DC link voltages increases. At V_{dc}=12 kV, the switching frequency has to be lowered to keep the junction temperature below 150 ℃.

To reduce the switching loss of the AC-DC stage, critical conduction mode (CRM) is normally implemented in LV PFC applications [39] to achieve ZVS turn-on at the expense of increased control complexity and large conduction loss. However, there is currently no publications that discussed the CRM mode operation of a MV AC-DC converter. The main concerns may include: 1) a current zero crossing detection circuit is required in CRM, which is not easy to implement in MV applications. 2) Switching frequency varies in CRM, which makes it difficult to design input filter and create additional EMI problems. 3) The current ripple is two times of the average current, resulting in larger input filters. Nevertheless, CRM based MV AC-DC is worth exploring since it will completely eliminate the switching loss (E_{on}=0, E_{off}=0) and the conduction loss can always be reduced by paralleling more devices. Multiphase CRM AC-DC can be used to reduce the input side current ripples.

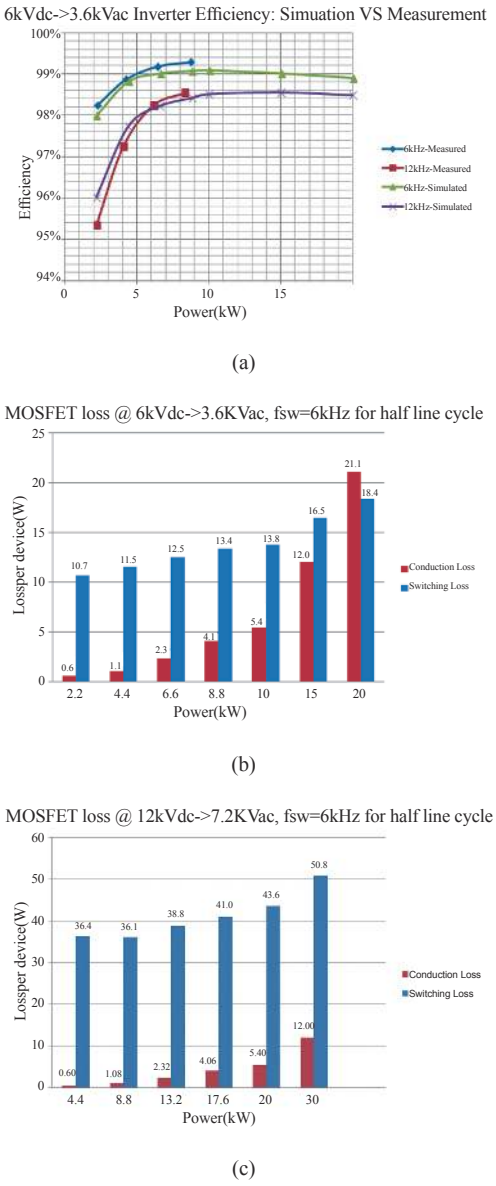

Fig. 10. (a) Measured and calculated AC-DC converter efficiency at V_{dc} =6kV and f_s=6 kHz and 12 kHz. (b) Loss breakdown at V_{dc}=6 kV, f_s=6 kHz; (c) Loss breakdown at V_{dc} =12 kV and f_s=6 kHz.

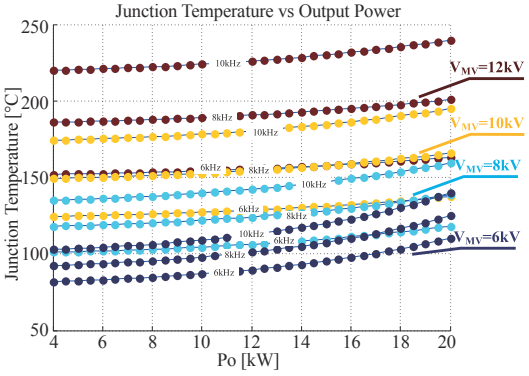

Fig. 11. Minimum 15 kV SiC MOSFET junction temperature versus processed power with different f_s and V_{MV} in AC-DC application. Natural cooling.

The integrated silicon diode in Fig. 9(a) may experience an abnormal avalanche breakdown in every switching cycle and the circuit has potential shoot-through problem [28]. An improved AC-DC as shown in Fig. 9(b) is presented in [28] to solve the shoot-through and avalanche of silicon diode problems. In the improved topology, the SiC MOSFET body diode never conducts and there is no shoot through problem that threatens the safe operation of the circuit.

B. DC-DC Applications

MV MF isolated DC-DC converter is an essential device functioning as a DC transformer in future MV DC grid as well as a key stage in a Type D SST. Its conversion efficiency is crucial to the overall system power efficiency. In addition, it needs to step down the MV DC to LV DC and provides system galvanic insulation. Its operation frequency directly determines the MF transformer's size. SiC MOSFETs with fast switching speed enables the realization of MV MF transformation. However, due to the significant amount of energy store in the output capacitance, even with zero load current, hard turn-on loss is still high enough to limit the operation frequency below 10 kHz [13], [28]. To increase the switching frequency and conversion efficiency, full ZVS DC-DC converter is therefore required.

Dual Active Bridge (DAB) or Dual Half Bridge (DHB, Fig. 12) are classical solutions for MV isolated DC-DC converter with ZVS capability. Only two MV switches are needed in the DHB. It has simple and symmetrical structure, easy to start up and to implement over current protection. With the 15 kV SiC MOSFETs, a 6 kV-400 V, 10 kW DHB DC-DC converter running at 20 kHz has been developed and reported [19]. The steady state waveforms at 6 kV/ 6.5 kW is shown in Fig. 14(a). ZVS of the switch is obtained in this condition. However, ZVS may be lost under light load condition and the high turn off current may result in non-zero turn-off loss (introduce additional voltage-current overlap during device turn-off) hence deteriorates the overall efficiency [13], [20]. Additional control methods such as extended-phase-shift (EPS) and dual-phase-shift (DPS) can be applied to extend the ZVS operation range of this converter [36], [37].

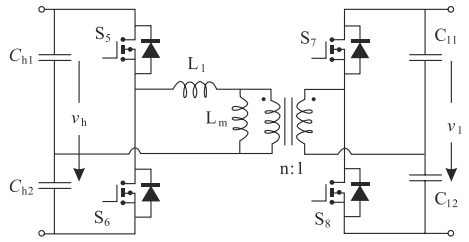

Fig. 12. DHB based DC/DC converter circuit used in [13] .

Novel MV DC-DC converter (see Fig. 13) that combines a DAB and a series resonant converter has been demonstrated by the authors in [19]. Operating at 40 kHz, it can realize ZVS at any load condition [19]. From zero to full load, the converter is designed to operate at the resonant frequency. Magnetizing current charges and discharges the MOSFETs' output capacitors during the switching interlock time. According to (5), complete soft turn-on is realized by carefully chosen magnetizing inductance and dead-time t_d. Fig. 14(b) and (c) shows the steady state waveforms of the converter with a V_{dc}=10 kV at light and heavy loads. V_{ds} waveforms in orange indicate that ZVS is fully achieved in both load conditions.

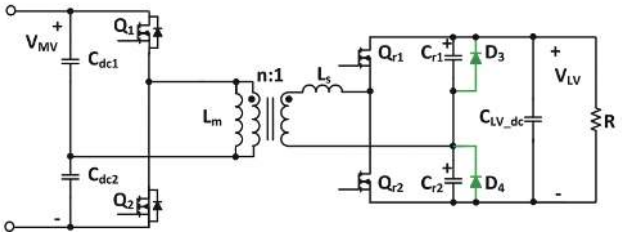

Fig. 13. Novel resonant and DAB hybrid DC-DC converter in [19].

$$Q_{oss}(V_{ds}) \le V_{MV}\, T_r\, t_d / 8 L_m \tag{5}$$

In order to have an optimized L_m and t_d, understanding the MOSFETs' output charge is crucial. [23] proposed a new test circuit that not only reflects the realistic ZVS scenario, but also achieves high accuracy (<1% error). High voltage measurement of the MOSFETs' output charge was measured up to 12 kV without resorting to special equipment or complex configuration. The result is shown in Fig. 6.

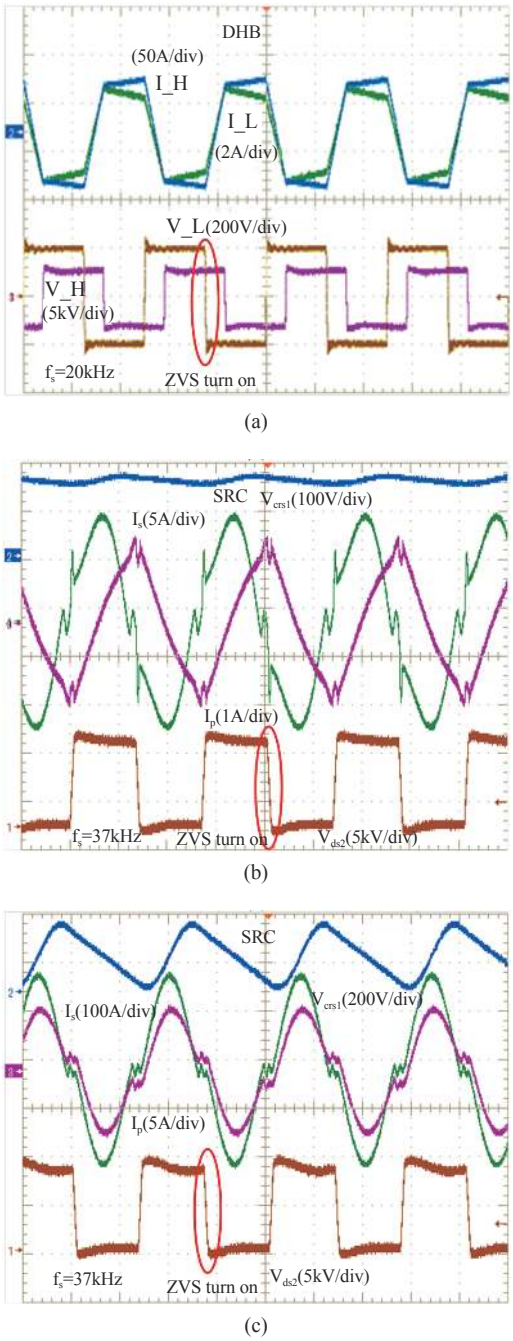

Fig. 14. DC-DC Operation waveforms (a) DHB at 6 kV/ 6.5 kW/20 kHz (b) SRC at 10 kV /1 kW/ 40 kHz (b) SRC at 10 kV /17 kW/ 40 kHz.

The Q_{oss} model, together with the on-resistance model as well as the thermal model, is used to calculate the maximum power handling capability of the 15 kV SiC MOSFET in the Fig. 13 DC-DC topology. The results are summarized in Fig. 15. The results indicate the amazing capability of the 15 kV

SiC MOSFET if soft switching is achieved. With less than 2 cm^2 total chip area for the two MV switches, the converter can deliver greater than 30 kW when operates at 12 kV with 100 kHz switching frequency. In a well-designed ZVS DC-DC converter, body diode conduction of MOSFET can also be avoided. The anti-paralleled SiC JBS diode is not necessary, which further lowers the semiconductor cost.

Fig. 16 provides the measured efficiency curves at both 6 kV and 10 kV conditions over a wide load range. The achieved efficiency is higher than 97% at most load conditions and the peak efficiency is up to 98%.

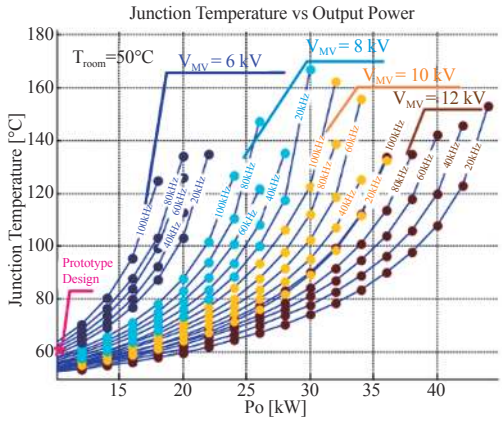

Fig. 15. Optimized (minimum)15 kV SiC MOSFET junction temperature versus processed power with different f_s and V_{MV} in DC-DC application. Natural convection cooling [19].

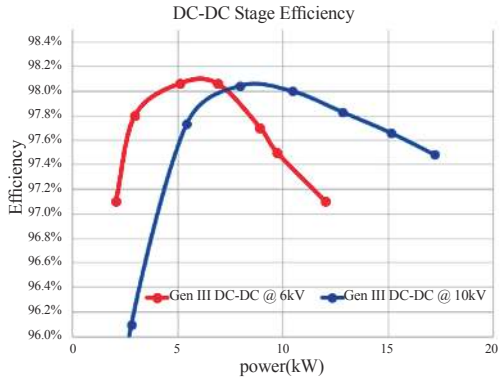

Fig. 16. Efficiency curves of the MV DC-DC converter at 6 kV and 10 kV.

C. AC-AC Applications

Type A SST shown in Fig. 2 is also attractive since the power conversion stages are reduced. The reduced power stages and simplified system configuration enables higher efficiency and reliability. The main challenges to implement MV Type A SST is the ZVS design under wide input voltage range. The input voltage changes from 0 to 10 kV every line frequency cycle. Achieving ZVS under such wide voltage range and load conditions is very difficult. The ZVS constraint is still represented by equation (6).

$$I_{off}(V_{ds}, P_o)t_{dead} \geq Q_{oss}(V_{ds}) \tag{6}$$

However, The Q_{oss} of the MOSFET is nonlinear with the V_{ds} voltage, while turn off current at left hand side of the equation has a linear relatioship with voltage, which makes the ZVS design more complicated.

Fig. 17 shows a Type A topology based on DAB and four-quadrant switch cells [34]. The converter can operate at high frequency and efficiency due to its ZVS capability. This circuit also shows a good capability in bidirectional power flow and voltage regulation. The turn off current of a normal SPS controlled DAB can be expressed in as [31]

$$I_{off} = \frac{T_S}{4L}[nV_{in}(2d-1) + V_o] \tag{7}$$

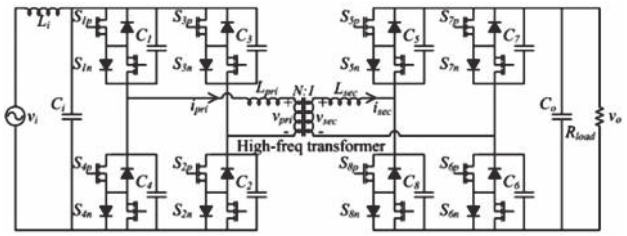

Fig. 17. Direct AC-AC converter based on DAB in [34].

The turn-off current in (7) not only depends on the load condition but also on the input voltage. If not well designed, ZVS may be lost at light load and low voltage conditions due to insufficient turn off current [31]. Additional control methods such as extended-phase-shift (EPS) and dual-phase-shift (DPS) can be applied to extend the ZVS operation range [36]-[37]. The converter in [34] also contains eight MF MV device, which is not cost effective.

Fig. 18 shows another Type-A SST configuration which uses an ISOP configuration of low voltage AC-AC converters [11]. Series resonant converter (SRC) is used as the AC-AC topology that operates in half cycle discontinuous conduction mode. [11] provides an analysis of the ZVS behavior under wide input voltage range. A time-dependent variation of deadtime control is adopted to achieve ZVS over the entire grid period. The SST is based on modular structure with voltage on each module less than 1200 V. Many modules are needed to achieve MV and there are no experimental results reported so far.

The authors of the paper have proposed a Type-A SST using a two-level SRC circuit based on the 15 kV SiC MOSFETs, as shown in Fig. 19 [39]. The circuit is proposed to operate at constant resonant switching frequency for high efficiency. The achieved gain is unity and is independent of load conditions. Only two MV switches are used.

In Fig. 19 circuit, the turn off current can be derived as

$$I_{Lm}(V_{ds}) = \frac{V_{ds}T_s}{8L_m} \tag{8}$$

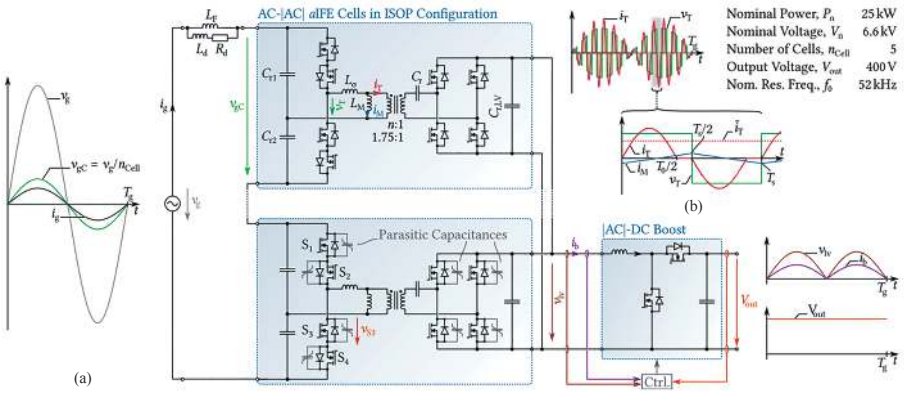

Fig. 18. Type A SST based on the ISOP Configuration of AC-AC converters [11].

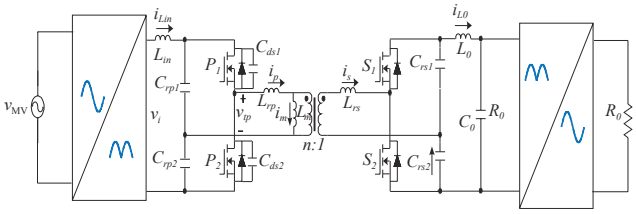

Fig. 19. Direct AC-AC converter based on SRC proposed by the author's group [39].

This turn off current is only associated with the input voltage, the magnetizing current and the deadtime and is idependent of the load condition, which means that if ZVS is obtained at a certain voltage level, this ZVS is maintained over wide load range. The ZVS constraint is still same as shown equation (5). The orange and blue curves in Fig. 20 shows the minimum deadtime required to realize ZVS over the half line cycle for two different L_m cases. These curves represent the adaptive deadtime strategy that is also mentioned in paper [11]. Long deadtime is needed at low input voltage range to maintain ZVS operation.

On the other hand, the turn-on loss of the SiC MOSFET decreases rapidly as V_{ds} decreases even if it has partial hard switching. In practical design, it is possible for the MOSFETs to experience hard switching at low voltage conditions if the turn on loss is controlled within a low level.

To simplify the deadtime control complexity, a constant deadtime scheme can be used and is drawn in pink curve in Fig. 20. The value of this deadtime is designed to guarantee

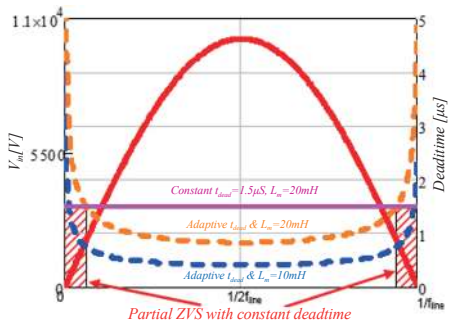

Fig. 20. Required and proposed deadtime versus input voltage.

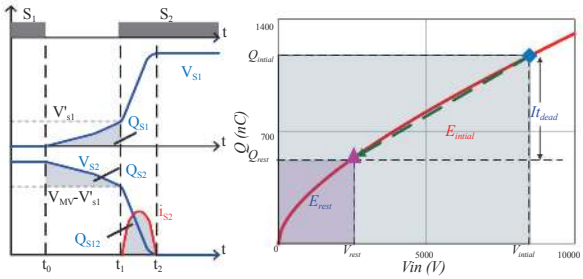

Fig. 21. Partial discharge theory.

the ZVS operation of the MOSFETs under most high voltage conditions. At low voltage conditions, the deadtime is not long enough to fully discharge the Q_{oss} of the devices and some turn on loss is generated. Such a partial discharge condition is shown in Fig. 21. When partial discharge happens, the residual Q_{oss} can be calculated as Q_{res}=Q_{oss}-It_{dead}.

The corresponding residual voltage at that moment can be derived based on equation (9)

$$V_{res} = \left(\frac{-4.08 + \sqrt{4.08^2 + 4 \cdot 0.0248 \frac{Q_{rest}}{2} 10^9}}{2 \cdot 0.0248}\right)^2 \tag{9}$$

The turn on power loss can be obtained with (10)

$$P_{on} = {f_{sw}}^2 \cdot f_{line} \int_0^{\frac{1}{2 \cdot f_{line}}} V_{res} Q_{res} \tag{10}$$

Fig. 22(a) shows the residual charge Q_{res} and voltage V_{res} versus the input voltage under different deadtime conditions. Fig. 22(b) shows the results of turn on loss versus deadtime under different L_m conditions with a switching frequency of 40 kHz. The curves indicate that the turn on loss decreases dramatically as the deadtime increases or L_m decreases. If the deadtime and L_m values are properly selected, the turn on loss will be small even if partial discharge happens.

Increasing deadtime or decreasing magnetizing inductance both help reduce the turn on loss. However, smaller magnetizing inductance leads to larger circulating and RMS current in the circuit. Longer deadtime also leads to higher RMS current and more distortion. Both methods will cause larger

conduction loss in the circuit. The L_m and t_{dead} selection is actually a trade-off between switching loss and conduction loss.

RMS current on MV side can be calculated with equations from (11) to (13) [32], [33].

$$i_{r\_p}(t) = \sqrt{2} I_{RMS\_P} \sin(\omega_0 t + \varphi) \tag{11}$$

$$i_{Lm\_p}(t) = -\frac{V_{in} T_0}{8 L_m} + \frac{V_{in}}{2 L_m} T \tag{12}$$

$$I_{RMS\_P} = \sqrt{\frac{\pi^2 I_o^2}{2n^2} \left(\frac{T_s}{T_s - 2t_d}\right)^2 + \frac{\left(\frac{V_{in} T_0}{8 L_m}\right)^2}{2}} \tag{13}$$

Using the on-state resistance R_{on} and thermal models of the 15 kV SiC MOSFET, the overall semiconductor loss versus magnetizing inductance and deadtime in the proposed AC-AC converter are calculated and shown in Fig. 23. This figure is based on 7.2 kV, 13 kW and 40 kHz switching frequency conditions. When t_{dead} is short and L_m is large, overall loss increases as turn on loss increases. While when t_{dead} is long and L_m is small, overall loss is also high due to the increasing of conduction loss. Optimized parameters can be chosen based on Fig. 22 and Fig. 23. L_m and t_{dead} values are chosen as 20 mH and 1.5 μs in actual hardware implementation.

Fig. 24(a) and (b) show the system operation waveforms at 7.2 kVac, 12 kW condition, with an output voltage of 230 Vac. Fig. 24(b) is the zoom-in switching cycle waveforms

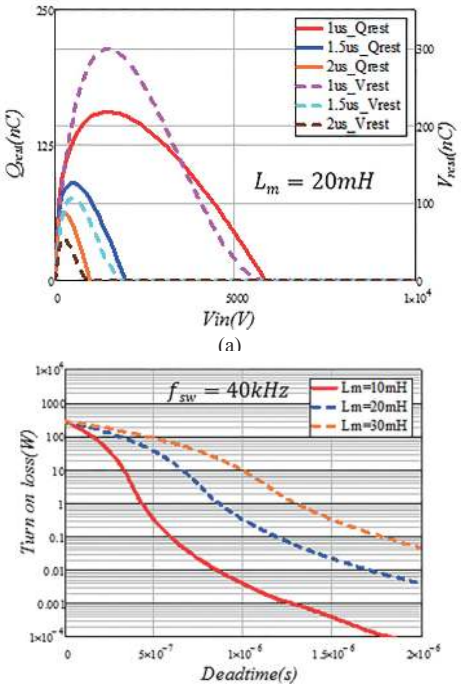

Fig. 22. (a) Residual output charge Q_{oss} and voltage vs input voltage (b) turn on loss vs deadtime.

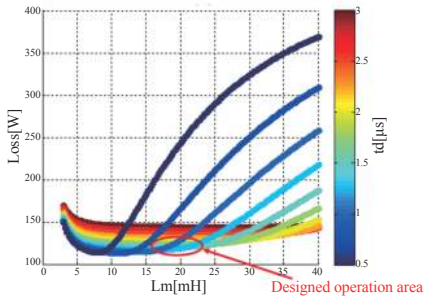

Fig. 23. Total semiconductor loss vs magnetizing inductance and deadtime. Vin=7.2kV, P=13 kW, f=40 kHz.

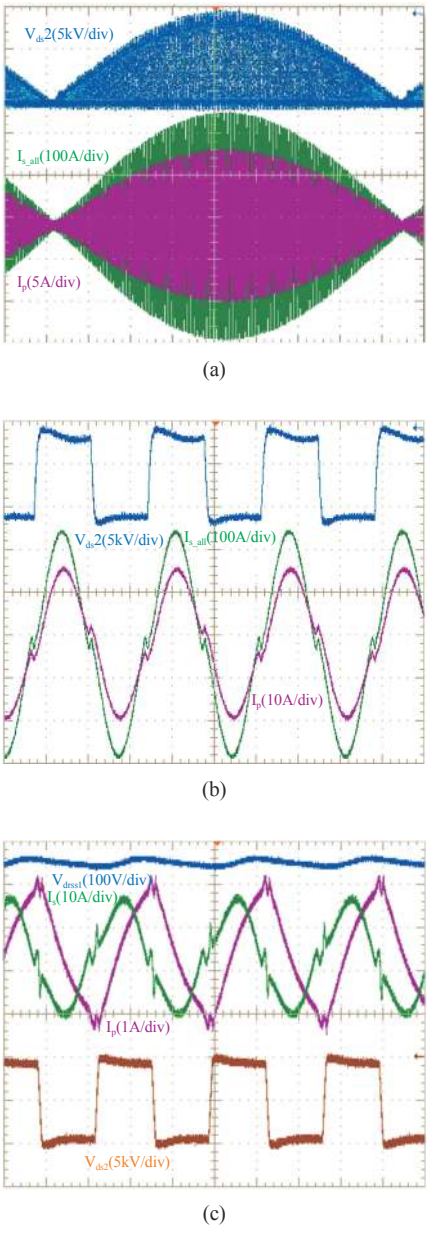

Fig. 24. Steady operation waveforms (a) and (b) V_{MV}=7.2 kV, P_o=12 kW; (c) V_{MV}=7.2 kV, P_o=600 W.

with a switching frequency of 37 kHz. The blue waveform is

the V_{ds} voltage of the MOSFET, which verifies the ZVS operation at 7.2 kV. Fig. 24(c) shows the operation waveforms at 7.2 kV / 600 W condition, which verifies the ZVS operation under at light load.

Efficiency of the developed prototype tested under 3.6 kV and 7.2 kV input voltage conditions are shown in Fig. 25. An efficiency curve of a Type D SST using the same MOSFETs is also added for comparison [13]. The efficiency for the developed Type A SST at 7.2 kV is shown in red curve and is higher than 97% under most load conditions. This figure shows an obvious improvement in efficiency compared with a Type D SST.

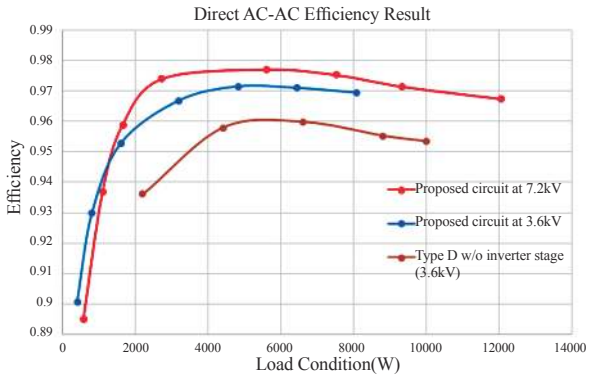

Fig. 25. Measured MV TLSS-SST efficiency, V_{MV}=3.6 & 7.2 kV, P_o from 600 W to 12 kW.

To fully utilize the 15 kV SiC MOSFETs in the direct AC-AC application, a series of optimized designs are presented in Fig. 26 with V_{MV} ranging from 3.6 to 7.2 kVac and switching frequency f_s from 20 to 100 kHz. One can observe from the results that if ZVS is well secured, a potential switching frequency of 100kHz and power over 20 kW can be achieved based on this device at 7.2 kV condition. Since the chip area of the MV switch is less than 2 cm^2, this resprents a remarkable power handling capability of more than 10 kW/cm^2 for the 15 kV SiC power MOSFET in natural convection condition. This can be increased further if forced air and water coolings are used.

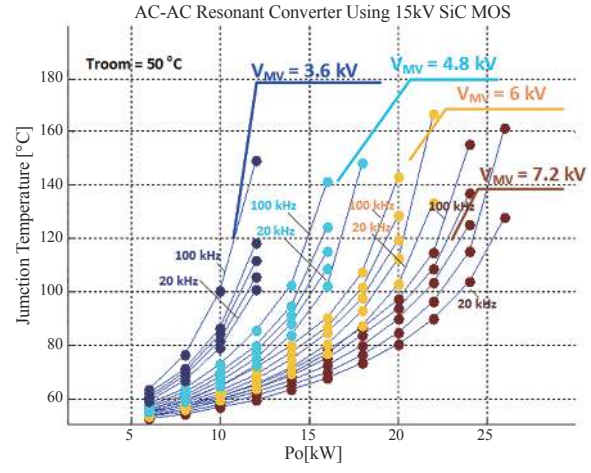

Fig. 26. 15kV SiC MOSFET junction temperature versus power with different f_s and V_{MV} in AC-AC application. Cooling=Natural convection.

IV. Conclusions

This paper reviews the characteristics of 15 kV SiC MOSFET in terms of conduction, switching and thermal performance. Comprehensive guidelines of implementing this device in practical MV applications such as AC-DC, DC-DC, AC-AC are elaborated in detail with an emphasis on device power and frequency handling capability. In hard switching MV AC-DC converters, switching loss dominates which limits the switching frequency to less than 10 kHz or even lower if DC link voltage reaches 12 kV. CRM AC-DC can be used to expand the switching frequency range. In isolated DC-DC and AC-AC applications, ZVS is extremely important and there are well studied topologies to achieve this. With the ZVS technique, the 15 kV SiC MOSFET can operate at frequencies up to 100 kHz and process an amazing amount of power in a small chip area. These results clearly demonstrate that the 15 kV SiC MOSFET is a disruptive and enabling device for a wide range of MV applications.

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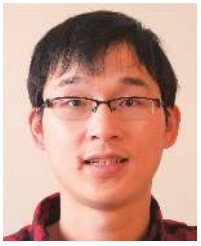
Alex Q. Huang received his B.Sc. degree from Zhejiang University, China in 1983 and his M.Sc. degree from Chengdu Institute of Radio Engineering, China in 1986, and his Ph.D. from Cambridge University, UK in 1992. From 1994 to 2004, he was a professor at CPES Virginia Tech. From 2004 to 2017, he has been with NC State University as the Progress Energy Distinguished Professor of Electrical and Computer Engineering. From September 2017, he will join University of Texas at Austin as the Dula D. Cockrell Centential Chair in Engineering. At NC State, he established the FREEDM Systems Center in 2008 and the PowerAmerica Institute in 2014. He has mentored more than 80 Ph.D. and master students to graduation, and has published more than 500 papers in journals and conferences. He is also the recipient of more than twenty U.S. patents. He is the recipient of the NSF CAREER award, the prestigious R & D 100 Award and the MIT Technology Review's 2011 Technology of the Year award. His current research interests are WBG power semiconductor devices, high density power converters, medium voltage power converters and renewable energy systems.



Qianlai Zhu was born in Wenzhou, China, in 1988. He received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010. From 2010 to 2013, he was an Electrical Engineer with the Delta Electronics Co., Shanghai China, where he was engaged in design and implement of server power supply and automotive onboard charger.

Currently he is pursuing the Ph.D. degree in the Department of Electronic and Electrical Engineering at the North Carolina State University. His current research interests include medium voltage Solid State Transformer design and implementation.

Li Wang received the Bachelor's and Master's degrees in electrical engineering from Zhejiang University, Hangzhou, China in 2009 and 2012 respectively. She received her Ph.D. degree from the NFS FREEDM Systems Center at North Carolina State University, Raleigh, NC, USA. She is now a senior engineer at Tesla, Inc. Her research interests include medium-voltage medium-frequency solid-state transformer, resonant converter with advanced control, and magnetics design.

Liqi Zhang was born in Ma'anshan, Anhui, P.R.China in 1991. He obtained bachelor's degree of Electrical Engineering and Automation from Chongqing University, Chongqing, P.R.China in 2013 and master's degrees in Electrical Engineering from North Carolina State University in 2015. He is currently pursuing the Ph.D. degree with the NFS FREEDM Systems Center, North Carolina State University, Raleigh, NC, USA. His current research interests include power module packaging, medium voltage circuit breaker and medium voltage solid-state transformer.