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# 160-Gb/s Silicon All-Optical Packet Switch for Buffer-less Optical Burst Switching

Hao Hu, Hua Ji, Minhao Pu, Michael Galili, Kresten Yvind, and Leif Katsuo Oxenløwe

***Abstract*—We experimentally demonstrate a 160-Gb/s Ethernet packet switch using an 8.6-mm-long silicon nanowire for optical burst switching, based on cross phase modulation in silicon. One of the four packets at the bit rate of 160 Gb/s is switched by an optical control signal using a silicon based $1 \times 1$ all-optical packet switch. Error free performance (BER $<$ 1E-9) is achieved for the switched packet. The use of optical burst switching protocols could eliminate the need for optical buffering in silicon packet switch based optical burst switching, which might be desirable for high-speed interconnects within a short-reach and small-scale network, such as board-to-board interconnects, chip-to-chip interconnects, and on-chip interconnects.**

***Index Terms*—All-optical signal processing, cross phase modulation, optical burst switching (OBS), optical packet switching (OPS), optical time division multiplexing (OTDM), photonic switching, silicon photonics.**

## I. Introduction

THE data traffic within Internet data centers and high-performance computing systems have been consistently growing over the past two decades [1]. The very high aggregate bandwidth demands of these systems have opened up opportunities for optics to compete with electronic interconnects, from rack-to-rack interconnects, chip-to-chip interconnects to on-chip interconnects [2]. In order to meet network bandwidth demands, 100 Gb Ethernet has been adopted by the new IEEE 802.3ba standards [3], however it is quite likely that network traffic will push it even further [4]. Silicon nanophotonics is a promising technology for low-power and cost-effective optical interconnects, due to its ultra-compactness, broad working bandwidth, high-speed operation, integration potential with electronics and complementary metal–oxide–semiconductor (CMOS) compatibility allowing cheap mass production [5]–[10]. In addition, silicon based optical signal processing functionalities where many bits are processed in a compact and integrated device without optical-electrical-optical (OEO) conversion has been identified as a potentially energy-efficient solution [11].

Current networks use optical circuit switching (OCS) for optical cross-connect, where a lightpath needs to be established from a source node to a destination node using a physical path. The OCS is suitable for large, stable and long duration traffic flows, where the lightpath setup time is much less than the data duration. However, the internet traffic has been recognized as consisting of a small number of large and long duration traffic flows and many small traffic flows, and exhibits a bursty nature [12]. The OCS is not ideal for bursty traffic, where the data transmission might not have a long duration relative to the setup time of the lightpath. To address the bursty internet traffic, optical packet switching (OPS) and optical burst switching (OBS) have been proposed as excellent candidates for high-speed interconnects, due to their better flexibility, resource utilization, functionality and granularity [13]–[18]. In an OPS network, an optical packet is sent along with its header. While the header is processed by a switching node, the packet needs to be buffered in the optical domain. The main challenge of OPS is lack of a practical optical buffer. In an OBS network, the burst header cell (BHC) is transmitted separately ahead of the transmission of a data burst to control the switching fabric and establish a path for the burst. The BHC contains the usual header information and the burst length. The data burst usually contains multiple packets. OBS can eliminate the need for a data burst to be buffered at the switching node by just waiting for the BHC to be processed. A major challenge of OBS is the data channel reservation protocol. Several protocols have been proposed to schedule bursts efficiently while achieving a high lightpath or bandwidth utilization at the same time, such as tell-and-go (TAG) and just-enough-time [14], [16].

Combination of silicon photonics and optical packet or burst switching might be a desirable technique for high-speed interconnects. Especially, memory devices (such as electronic random access memories (RAM)) are envisioned to be CMOS-integrated in a single silicon photonic chip [7]. Therefore, high speed ($>$100 Gb/s) silicon chips based OPS/OBS are very promising.

Using a silicon nanowire, we have demonstrated a 160 Gb/s packet switch, which can be used in OPS [18]. In this paper, we show that a silicon-based 160 Gb/s packet switch can also be used for OBS, and optical buffering could be avoided if a tell-and-wait (TAW) or TAG protocol is applied. In section II, we describe the working principle of the TAW or TAG protocol and compare the silicon based OBS with the $\mathrm{N} \times \mathrm{N}$ silicon based switch matrix. In section III, the design and the characteristics of the silicon nanowire are presented. In section IV, we describe the working principle of cross phase modulation (XPM) in silicon and its application for packet switching. In addition, we show that the silicon-based $1 \times 1$ all-optical packet switch could be upgraded to $1 \times \mathrm{N}$ all-optical packet switch if a fast tuning laser is used. In Sections V and VI, we show the experimental

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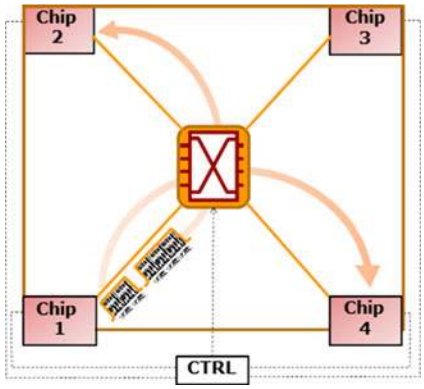


Fig. 1. Short-reach and small-scale network scenario using silicon based OBS.

setup and results of the 160 Gb/s all-optical packet switch for OBS. We experimentally demonstrate a 160 Gb/s packet switch using an 8.6-mm long silicon nanowire based on XPM. One of four packets at the bit rate of 160 Gb/s is switched by an optical control signal. Error free performance (BER < 1E-9) is achieved for the switched packet.

## II. TAW and TAG

In the scenario of short-reach and small-scale interconnects (as shown in Fig. 1), such as interconnections among servers, boards and even chips, optical packets could be stored in the electronic domain using electronic RAM and will not be converted into the optical domain and transmitted until the switching node is ready for the packet. In this case, a two-way reservation protocol such as TAW can be applied [19], [20]. Since the end nodes are close to each other, both BHC and confirmation from the switching node can be sent in the electronic domain with negligible latency and avoiding OEO conversion, which is different in the case of conventional OBS. Another different feature is that the data payload of a burst could be either a short packet or several accumulated long packets, which makes the switching more flexible but requires faster switching speed. In comparison with conventional OPS, which can be used in the large-scale interconnects but requires label processor and packet buffer [21]–[23], our proposed scheme addresses the scenario of short-reach interconnects, and no label is transmitted together with the packet and packet buffer can be avoided.

As shown in Fig. 1, when an ingress end node (EN, e.g., Chip 1) needs to transfer a packet, it first sends a *setup* message (i.e., BHC) to the control plane. When the control plane receives the *setup* message, a virtual path will be established towards its egress EN (e.g., Chip 2 or Chip 4) during the data payload transmission if the switching node is free, and then the control plane will send a *confirmation* message to the ingress EN. Once the ingress EN receives the *confirmation* message, the data payload stored at the electronic RAM of the ingress EN will be immediately converted into an optical burst and then sent to the egress EN. The virtual path will be automatically released according to the BHC. If more than one ingress EN need to transfer data payload at the same time or the switching node is busy, the data payload at the ingress ENs is still stored

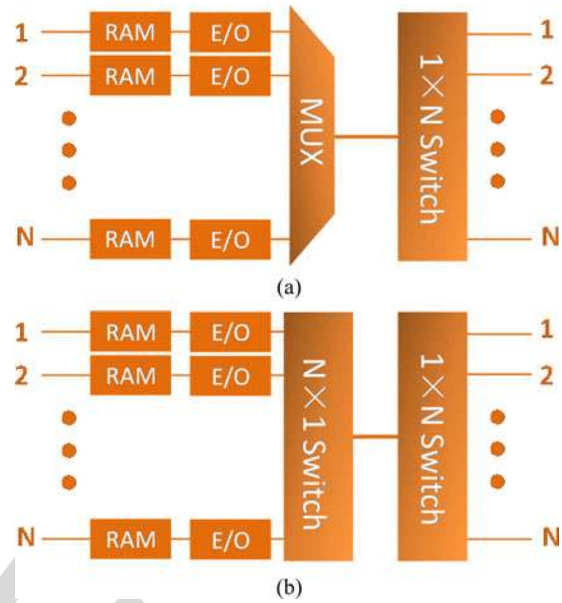


Fig. 2. Schematic architecture of silicon packet switch based OBS using (a) TAW and (b) TAG.

in the electronic RAM and a waiting list will be established in the control plane. The data payload will wait for the transfer according to the sequence of the list. The sequence of the list depends on the priority based class-of-service. Even if the packet blocking probability rises with higher data load, higher class services experience relatively lower blocking probability compared to lower class services [15]. Fig. 2(a) shows a possible architecture of a silicon packet switch based optical burst switch using TAW protocol. Only one of N ingress ENs will receive the *confirmation* message at a time and send data payload to the $1 \times N$ switch through a multiplexer, which could be a coupler. The $1 \times N$ switch will switch the data payload to its egress EN according to the BHC.

Another scheme is TAG, which is a one-way reservation protocol and requires no acknowledgement from the switching node before sending the data payload. When an ingress EN has a data payload to transfer, it sequentially sends a *setup* message to the control plane and an optical burst to the optical switch with a guard time in between. The guard time is at least equal to or more than the time interval needed for setup of a virtual path inside the switching node. This allows the optical switch to be set before the packet arrives. If the switching node is free when it receives the *setup* message, a virtual path will be set up for the packet transfer and a *successful* message will be sent back to the ingress EN. If the switching node is busy when it receives the *setup* message, the optical packet sent from the ingress EN will be discarded and a *fail* message will be sent back to the ingress EN. If the ingress EN receives the *successful* message, the electronic RAM storing the data payload will be released. If the ingress EN receives the *fail* message, it will send the *setup* message and the optical burst again. Fig. 2(b) shows a possible architecture of silicon packet switch based OBS using TAG protocol. If the control plane receives a *setup* message from an ingress EN and the switching node is free at the time, the first

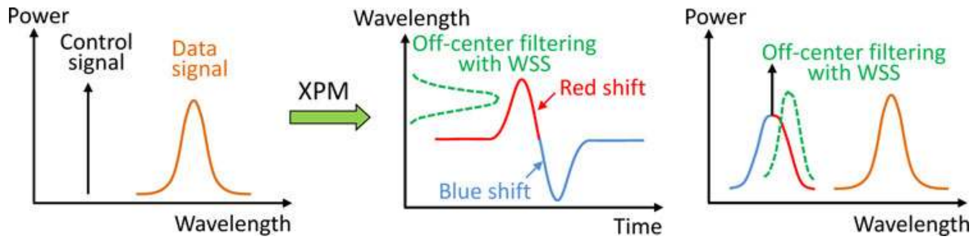


Fig. 3. Operation principle of the XPM in a silicon nanowire with subsequent off-center filtering.

$N \times 1$ switch will connect to the ingress EN and allow the data payload to enter, and the second $1 \times N$ switch will switch to its egress EN according to the BHC. If the switching node is busy when the control plane receives the *setup* message, the first $1 \times N$ switch will not connect to the ingress EN and the data payload sent from the ingress EN will be discarded.

Compared to an $N \times N (N \in 2^n,\ n = 1, 2, 3, \ldots)$ silicon based switch matrix with a granularity of the optical paths, silicon based OBS with a granularity of optical packets is more flexible and could have smaller footprint and less power consumption. For the $N \times N$ switch matrix based on path-independent insertion loss and "switch-and-select" topology, the total number of Mach–Zehnder interferometer (MZI) switches is $2 \times N \times N$ and $2 \times N \times (N–1)$, respectively [24], [25]. Assuming MZI switches are also used in the $1 \times N$ switch, as shown in Fig. 2, the total number of MZI switches for the TAW and TAG are N–1 and $2 \times (N–1)$, respectively. In addition, no intersections are needed for the $1 \times N$ switch, and therefore there will be no crosstalk.

A main requirement for the silicon packet switch is that the switching speed of the optical switches should be fast enough in order to introduce less latency and lower blocking probability, and therefore the switching time should preferably be no more than a few nanoseconds.

## III. Silicon Nanowire

The key device for the silicon all-optical packet switch is a dispersion engineered 8.6-mm long silicon straight waveguide, which includes tapering sections for low loss interfacing with optical fiber [26]. The main waveguide section is ~8 mm long and has a cross-sectional dimension of 240 nm × 450 nm while the tapering sections are ~0.3 mm long each. The width at the end of the silicon nanowire is tapered from 450 nm to a tiny tip end of 40 nm so that the guided mode will expand into a polymer waveguide, surrounding the silicon-on-insulator (SOI) waveguide and the taper. The device has an SOI structure, with the silicon waveguide placed on a $SiO_2$/Si substrate. The measured propagation loss is 4.3 dB/cm and the fiber-to-fiber loss of the device is 6.8 dB.

## IV. XPM in a Silicon Nanowire for Packet Switch

XPM is an ultrafast optical Kerr effect, with a response time of a few fs. Fig. 3 shows the operation principle of XPM in a silicon nanowire with subsequent off-center filtering. The pump pulse can modulate the refractive index of the silicon waveguide, which results in phase modulation on the co-propagating continuous wave (CW) probe [27]. The phase modulation will then result in transient chirp on the CW probe. The leading edges of the pump pulse will generate red-shift chirp, whereas the trailing edge of the pump pulse will generate blue-shift chirp. The blue shifted and red shifted sidebands are generated as a result of the chirp. If an off-center filter is used to extract either the blue shifted sideband or the red shifted sideband, the XPM-induced phase modulation can be converted into amplitude modulation. When an RZ-OOK data signal is used as the pump, the generated sideband can pass through the off-center filter in the presence of a "1" bit of the pump, whereas no generated sideband results in no transmission through the off-center filter in the presence of a "0" bit of the pump. Using a CW probe, the XPM in silicon with subsequent off-center filtering has been used for forward error correction supported 150 Gb/s wavelength conversion, 10 Gb/s tuneable wavelength conversion, 40 Gb/s regenerative wavelength conversion and 160 Gb/s all-optical data modulator [27]–[30]. If the probe is gated in time (with a gating time slightly larger than the packet duration), XPM in silicon with subsequent off-center filtering, can be used for packet switching with ultrafast response time. Fig. 4 shows an illustration of packet switch based on the XPM in silicon with subsequent off-center filtering using gated probe light. For the $1 \times 1$ packet switch, 1 out of 4 data packets ($\lambda_D$) is switched out at the wavelength of $\lambda_C + \Delta\lambda$ when the control signal ($\lambda_C$) is set to be on. When the control signal is off, no light is generated at the wavelength of $\lambda_C + \Delta\lambda$. For the $1 \times N$ packet switch, a wavelength selective switch (WSS) with different wavelengths at different outputs should be used. When the wavelength of the control signal is fast tuned, the incoming packet could be switched to different outputs of the WSS. The tuning speed of the tunable laser depends on the guard band between packets, which is typically on the order of several nanoseconds to several microseconds. This requirement of tuning speed could be relaxed if the granularity of the packet becomes large, i.e., introducing large enough guard band (~$\mu$s) by switching a long packet or several aggregated short packets. If the first packet of four data packets needs to be switched to port 1 of the WSS, the wavelength of the control signal should be tuned to be $\lambda_{C1}$; if the second packet of four data packets needs to be switched to port 4 of the WSS, the wavelength of the control signal should be tuned to be $\lambda_{C4}$. Compared to the $1 \times N$ packet switch based on cascaded MZI switches, which needs N–1 active switch, the XPM based $1 \times N$ packet switch only needs an active fast tunable laser followed by passive filtering. Based on the $1 \times N$ packet switch, the TAW and TAG protocol can be realized, as shown in Fig. 2.

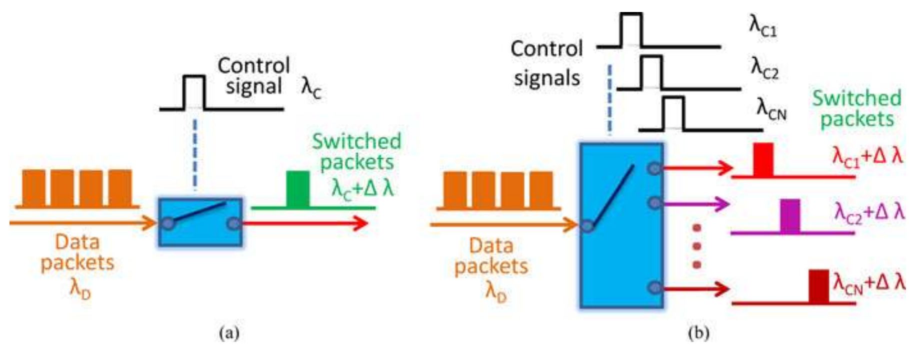


Fig. 4. Illustration of packet switch. (a) One out of four data packets is switched out using $1 \times 1$ packet switch when the control signal is set to be on; (b) One of the input data packets is switched to different path using $1 \times$ N packet switch when the wavelength of the control signal is tuned. Blue box: WSS with different wavelengths at different outputs.

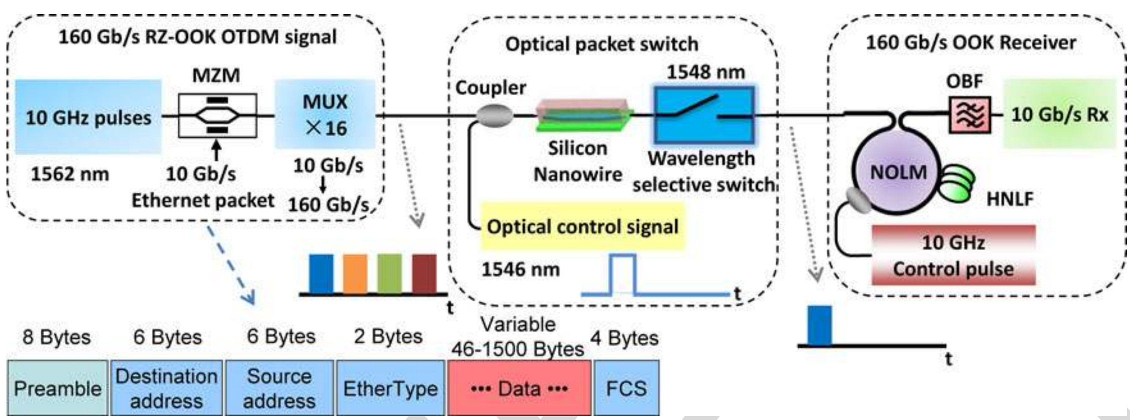


Fig. 5. Experimental setup for the 160 Gb/s all-optical packet switch using a silicon nanowire followed by a WSS.

## V. Experimental Setup

The experimental setup for the 160 Gb/s silicon packet switch is shown in Fig. 5. It mainly includes a 160 Gb/s RZ-OOK transmitter, a $1 \times 1$ silicon based packet switch and a 160 Gb/s on–off keying (OOK) receiver. The erbium-glass oscillating pulse-generating laser produces 10 GHz pulses at 1542 nm with a 1.5-ps full-width at half-maximum pulse width. The spectrum of the pulses is broadened in a 400-m dispersion-flattened highly nonlinear fibre (DF-HNLF, dispersion coefficient $D = -0.45$ ps/nm/km and dispersion slope $S = 0.006$ ps/nm$^2$/km at 1550 nm, nonlinear coefficient $\gamma = 10.5$ W$^{-1}$km$^{-1}$) due to self-phase modulation [31], [32]. The broadened spectrum is filtered at 1562 nm with a 5-nm optical bandpass filter (OBF) to generate the 10 GHz pulses for the data signal and is also filtered at 1538 nm using a 1 nm OBF to obtain the 10 GHz control pulses used in the OTDM demultiplexing. The generated 10 GHz pulses at 1562 nm are OOK modulated in a Mach–Zehnder modulator (MZM) using a software defined pattern to generate 10 Gb/s Ethernet packets. As shown in Fig. 5, the Ethernet packet with a maximum standardized size of 1518 bytes consists of a preamble, a destination address, a source address, an Ethertype, payload data and a frame check sequence [33]. The packets have duration of 2.19 $\mu$s, consisting of 1.22 $\mu$s of data payload separated by a 0.97 $\mu$s guard band. The generated 10 Gb/s Ethernet packet is multiplexed in time using a passive fiber-delay multiplexer (MUX $\times$ 16) to generate the 160 Gb/s signal.

In the $(1 \times 1)$ silicon based optical packet switch, the generated 160 Gb/s optical packet is amplified by an EDFA, then filtered by a 5 nm OBF and finally launched into the silicon nanowire through a 3-dB optical coupler. The optical control signal is generated from a CW light at 1546 nm, which is modulated by an electrical control signal in a MZM. The electrical control signal is generated according to the BHC of the burst, which has duration of 1.5 $\mu$s and repetition rate of $\sim$114 kHz in order to switch one of the four packets. The optical control signal is also launched into the silicon nanowire through the second input of the 3-dB coupler. Fig. 6 shows the waveforms of the packets and the control signal. The launched average power for the data and the control are 13.5 and 8.5 dBm, respectively, which corresponds to the energy consumption of 140 and 44 fJ/bit. Since the total launched power is well below the two photon absorption (TPA) threshold [6], the TPA and resulting carrier effects are negligible. The polarizations of the data signal and control signal are both aligned to transverse-electric polarizations into the silicon waveguide. The optical packets modulate the refractive index of the silicon waveguide and generate XPM on the control signal. Only if the control signal presents "1" level and aligned in time with a packet, the control signal will be phase modulated by the optical packet and be converted into an amplitude modulated signal by passing through an off-center filter. Note that the refractive index of the silicon waveguide could also be modulated by an electrical signal [8], therefore,

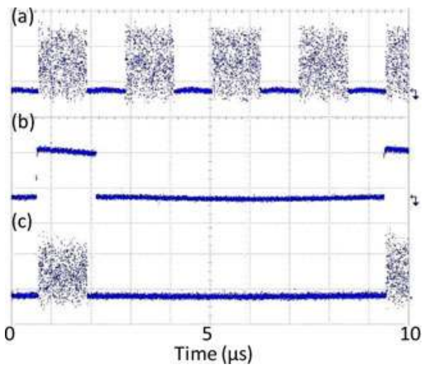


Fig. 6. Oscilloscope traces (a) 160 Gb/s optical packets at the input of the silicon nanowire; (b) optical control signal; (c) one out of four packets switched at the output of the silicon nanowire and WSS.

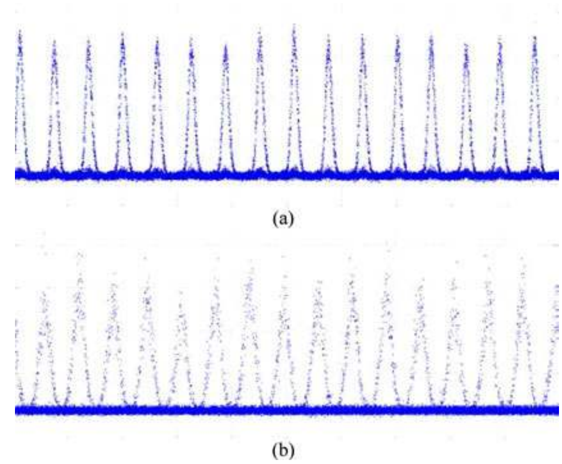


Fig. 7. (a) OSO eye diagrams of 160 Gb/s original packets (b) and 1-of-4 switched packet.

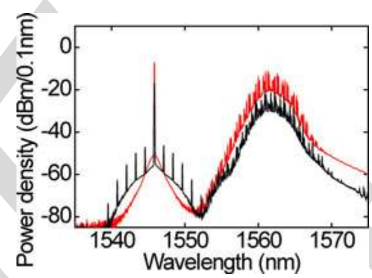


Fig. 8. Optical spectra at the input of the silicon chip (red) and output of the silicon nanowire (black).

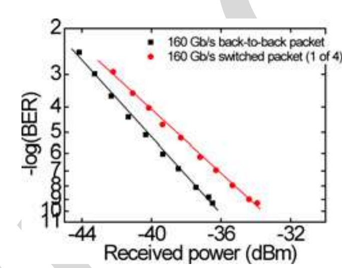


Fig. 9. BER measurements after demultiplexing to 10 Gb/s for the 160 Gb/s back-to-back packet and for the 160 Gb/s 4-to-1 switched packet.

in principle the scheme could also work if the electrical signal is directly employed on the silicon chip. At the output of the silicon nanowire, a WSS with the center wavelength of 1548 nm is used to filter out the red-shifted sideband of the control signal and select the switched packet.

The 4-to-1 switched 160 Gb/s packet was detected using a 160 Gb/s OOK receiver, which consists of a nonlinear optical loop mirror (NOLM) based OTDM demultiplexer, a 0.9-nm filter, a photo detector (PD) and an error analyzer. The NOLM is used to OTDM demultiplex the 160 Gb/s packet down to 10 Gb/s packets based on the XPM in a 50 m long HNLF. Finally, the demultiplexed 10 Gb/s optical packet was detected using a PD and the performance was evaluated using an error analyzer.

## VI. Experimental Results

Fig. 6 shows the dynamic operation of 160 Gb/s silicon packet switch. When the control plane receives BHC information, a control signal was generated to drive the silicon based all-optical switch. In this case, one of four packets needs to be switched; therefore, the targeted packet was aligned in time with the optical control signal, as shown in Fig. 6(a) and (b). At the output of the packet switch, the targeted packet was successfully switched with an extinction ratio of ~18 dB, as shown in Fig. 6(c). Fig. 7 shows optical sampling oscilloscope (OSO) eye diagrams of 160 Gb/s original packets and 1-of-4 switched packet. The switched packet has an open and clear eye diagram after the packet switch. Actually, some “0” level noise on the original packets was also removed after the $1 \times 1$ packet switch, resulting from the regenerative characteristics of the off-center filtering [29].

The spectra at the input and the output of the silicon nanowire are shown in Fig. 8. XPM on the control signal can be clearly seen (modulation peaks around the control signal) at the output of the silicon nanowire. The blue and red shifted sidebands on the optical control signal were generated from the leading edge and trailing edge of the 160 Gb/s optical packets with the modulation format of RZ-OOK, respectively. A WSS centered at 1548 nm is used to filter out the red-shifted probe light to obtain an amplitude modulated 160 Gb/s signal and separate the switched packet at 1548 nm from the original packet at 1562 nm.

The performance of the silicon based $1 \times 1$ all-optical packet switch for the 160 Gb/s Ethernet packet was evaluated using BER measurements, as shown in Fig. 9. BER curves are plotted for the 160 Gb/s back-to-back packets and for the 160 Gb/s 4-to-1 switched packets. The 4-to-1 switched 160 Gb/s packets achieve an error-free performance (BER $< 10^{-9}$) with a power penalty of ~2.5 dB compared to the back-to-back case. The measured penalty is partly attributed to the pulse broadening due to the filtering effect induced by the WSS, and partly attributed to the OSNR degradation after the packet switch due to the limited phase modulation on the control signal.

## VII. Discussion and Conclusion

We have successfully demonstrated a 160 Gb/s silicon based $1 \times 1$ all-optical packet switch, based on XPM in a silicon nanowire. This scheme could be upgraded to a $1 \times N$ all-optical packet switch if a fast tunable laser is used. The silicon packet switch could be used either for OPS or OBS without optical buffering if the TAW or TAG protocol is used. The 4-to-1 switched 160 Gb/s Ethernet packet shows error free performance (BER $<$ 1E-9), and holds great promise for future photonic switching of ultra-fast data signals.

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# 160-Gb/s Silicon All-Optical Packet Switch for Buffer-less Optical Burst Switching

Hao Hu, Hua Ji, Minhao Pu, Michael Galili, Kresten Yvind, and Leif Katsuo Oxenløwe

***Abstract*—We experimentally demonstrate a 160-Gb/s Ethernet packet switch using an 8.6-mm-long silicon nanowire for optical burst switching, based on cross phase modulation in silicon. One of the four packets at the bit rate of 160 Gb/s is switched by an optical control signal using a silicon based $1 \times 1$ all-optical packet switch. Error free performance (BER $<$ 1E-9) is achieved for the switched packet. The use of optical burst switching protocols could eliminate the need for optical buffering in silicon packet switch based optical burst switching, which might be desirable for high-speed interconnects within a short-reach and small-scale network, such as board-to-board interconnects, chip-to-chip interconnects, and on-chip interconnects.**

***Index Terms*—All-optical signal processing, cross phase modulation, optical burst switching (OBS), optical packet switching (OPS), optical time division multiplexing (OTDM), photonic switching, silicon photonics.**

## I. Introduction

THE data traffic within Internet data centers and high-performance computing systems have been consistently growing over the past two decades [1]. The very high aggregate bandwidth demands of these systems have opened up opportunities for optics to compete with electronic interconnects, from rack-to-rack interconnects, chip-to-chip interconnects to on-chip interconnects [2]. In order to meet network bandwidth demands, 100 Gb Ethernet has been adopted by the new IEEE 802.3ba standards [3], however it is quite likely that network traffic will push it even further [4]. Silicon nanophotonics is a promising technology for low-power and cost-effective optical interconnects, due to its ultra-compactness, broad working bandwidth, high-speed operation, integration potential with electronics and complementary metal–oxide–semiconductor (CMOS) compatibility allowing cheap mass production [5]–[10]. In addition, silicon based optical signal processing functionalities where many bits are processed in a compact and integrated device without optical-electrical-optical (OEO) conversion has been identified as a potentially energy-efficient solution [11].

Current networks use optical circuit switching (OCS) for optical cross-connect, where a lightpath needs to be established from a source node to a destination node using a physical path. The OCS is suitable for large, stable and long duration traffic flows, where the lightpath setup time is much less than the data duration. However, the internet traffic has been recognized as consisting of a small number of large and long duration traffic flows and many small traffic flows, and exhibits a bursty nature [12]. The OCS is not ideal for bursty traffic, where the data transmission might not have a long duration relative to the setup time of the lightpath. To address the bursty internet traffic, optical packet switching (OPS) and optical burst switching (OBS) have been proposed as excellent candidates for high-speed interconnects, due to their better flexibility, resource utilization, functionality and granularity [13]–[18]. In an OPS network, an optical packet is sent along with its header. While the header is processed by a switching node, the packet needs to be buffered in the optical domain. The main challenge of OPS is lack of a practical optical buffer. In an OBS network, the burst header cell (BHC) is transmitted separately ahead of the transmission of a data burst to control the switching fabric and establish a path for the burst. The BHC contains the usual header information and the burst length. The data burst usually contains multiple packets. OBS can eliminate the need for a data burst to be buffered at the switching node by just waiting for the BHC to be processed. A major challenge of OBS is the data channel reservation protocol. Several protocols have been proposed to schedule bursts efficiently while achieving a high lightpath or bandwidth utilization at the same time, such as tell-and-go (TAG) and just-enough-time [14], [16].

Combination of silicon photonics and optical packet or burst switching might be a desirable technique for high-speed interconnects. Especially, memory devices (such as electronic random access memories (RAM)) are envisioned to be CMOS-integrated in a single silicon photonic chip [7]. Therefore, high speed ($>$100 Gb/s) silicon chips based OPS/OBS are very promising.

Using a silicon nanowire, we have demonstrated a 160 Gb/s packet switch, which can be used in OPS [18]. In this paper, we show that a silicon-based 160 Gb/s packet switch can also be used for OBS, and optical buffering could be avoided if a tell-and-wait (TAW) or TAG protocol is applied. In section II, we describe the working principle of the TAW or TAG protocol and compare the silicon based OBS with the $\mathrm{N} \times \mathrm{N}$ silicon based switch matrix. In section III, the design and the characteristics of the silicon nanowire are presented. In section IV, we describe the working principle of cross phase modulation (XPM) in silicon and its application for packet switching. In addition, we show that the silicon-based $1 \times 1$ all-optical packet switch could be upgraded to $1 \times \mathrm{N}$ all-optical packet switch if a fast tuning laser is used. In Sections V and VI, we show the experimental

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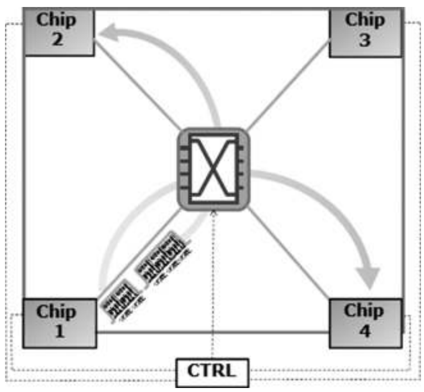


Fig. 1. Short-reach and small-scale network scenario using silicon based OBS.

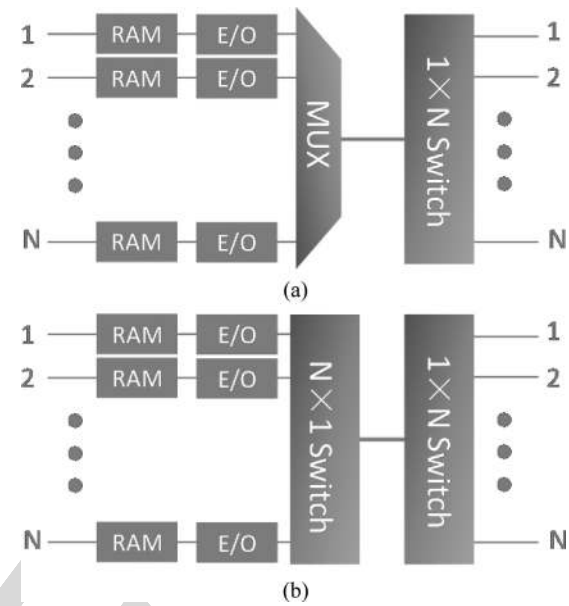


Fig. 2. Schematic architecture of silicon packet switch based OBS using (a) TAW and (b) TAG.

setup and results of the 160 Gb/s all-optical packet switch for OBS. We experimentally demonstrate a 160 Gb/s packet switch using an 8.6-mm long silicon nanowire based on XPM. One of four packets at the bit rate of 160 Gb/s is switched by an optical control signal. Error free performance (BER $<$ 1E-9) is achieved for the switched packet.

## II. TAW and TAG

In the scenario of short-reach and small-scale interconnects (as shown in Fig. 1), such as interconnections among servers, boards and even chips, optical packets could be stored in the electronic domain using electronic RAM and will not be converted into the optical domain and transmitted until the switching node is ready for the packet. In this case, a two-way reservation protocol such as TAW can be applied [19], [20]. Since the end nodes are close to each other, both BHC and confirmation from the switching node can be sent in the electronic domain with negligible latency and avoiding OEO conversion, which is different in the case of conventional OBS. Another different feature is that the data payload of a burst could be either a short packet or several accumulated long packets, which makes the switching more flexible but requires faster switching speed. In comparison with conventional OPS, which can be used in the large-scale interconnects but requires label processor and packet buffer [21]–[23], our proposed scheme addresses the scenario of short-reach interconnects, and no label is transmitted together with the packet and packet buffer can be avoided.

As shown in Fig. 1, when an ingress end node (EN, e.g., Chip 1) needs to transfer a packet, it first sends a *setup* message (i.e., BHC) to the control plane. When the control plane receives the *setup* message, a virtual path will be established towards its egress EN (e.g., Chip 2 or Chip 4) during the data payload transmission if the switching node is free, and then the control plane will send a *confirmation* message to the ingress EN. Once the ingress EN receives the *confirmation* message, the data payload stored at the electronic RAM of the ingress EN will be immediately converted into an optical burst and then sent to the egress EN. The virtual path will be automatically released according to the BHC. If more than one ingress EN need to transfer data payload at the same time or the switching node is busy, the data payload at the ingress ENs is still stored in the electronic RAM and a waiting list will be established in the control plane. The data payload will wait for the transfer according to the sequence of the list. The sequence of the list depends on the priority based class-of-service. Even if the packet blocking probability rises with higher data load, higher class services experience relatively lower blocking probability compared to lower class services [15]. Fig. 2(a) shows a possible architecture of a silicon packet switch based optical burst switch using TAW protocol. Only one of N ingress ENs will receive the *confirmation* message at a time and send data payload to the $1 \times N$ switch through a multiplexer, which could be a coupler. The $1 \times N$ switch will switch the data payload to its egress EN according to the BHC.

Another scheme is TAG, which is a one-way reservation protocol and requires no acknowledgement from the switching node before sending the data payload. When an ingress EN has a data payload to transfer, it sequentially sends a *setup* message to the control plane and an optical burst to the optical switch with a guard time in between. The guard time is at least equal to or more than the time interval needed for setup of a virtual path inside the switching node. This allows the optical switch to be set before the packet arrives. If the switching node is free when it receives the *setup* message, a virtual path will be set up for the packet transfer and a *successful* message will be sent back to the ingress EN. If the switching node is busy when it receives the *setup* message, the optical packet sent from the ingress EN will be discarded and a *fail* message will be sent back to the ingress EN. If the ingress EN receives the *successful* message, the electronic RAM storing the data payload will be released. If the ingress EN receives the *fail* message, it will send the *setup* message and the optical burst again. Fig. 2(b) shows a possible architecture of silicon packet switch based OBS using TAG protocol. If the control plane receives a *setup* message from an ingress EN and the switching node is free at the time, the first

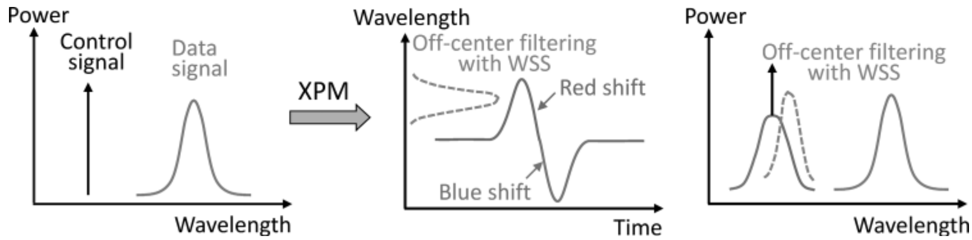


Fig. 3. Operation principle of the XPM in a silicon nanowire with subsequent off-center filtering.

$N \times 1$ switch will connect to the ingress EN and allow the data payload to enter, and the second $1 \times N$ switch will switch to its egress EN according to the BHC. If the switching node is busy when the control plane receives the *setup* message, the first $1 \times N$ switch will not connect to the ingress EN and the data payload sent from the ingress EN will be discarded.

Compared to an $N \times N (N \in 2^n,\ n = 1, 2, 3, \ldots)$ silicon based switch matrix with a granularity of the optical paths, silicon based OBS with a granularity of optical packets is more flexible and could have smaller footprint and less power consumption. For the $N \times N$ switch matrix based on path-independent insertion loss and "switch-and-select" topology, the total number of Mach–Zehnder interferometer (MZI) switches is $2 \times N \times N$ and $2 \times N \times (N–1)$, respectively [24], [25]. Assuming MZI switches are also used in the $1 \times N$ switch, as shown in Fig. 2, the total number of MZI switches for the TAW and TAG are N–1 and $2 \times (N–1)$, respectively. In addition, no intersections are needed for the $1 \times N$ switch, and therefore there will be no crosstalk.

A main requirement for the silicon packet switch is that the switching speed of the optical switches should be fast enough in order to introduce less latency and lower blocking probability, and therefore the switching time should preferably be no more than a few nanoseconds.

## III. Silicon Nanowire

The key device for the silicon all-optical packet switch is a dispersion engineered 8.6-mm long silicon straight waveguide, which includes tapering sections for low loss interfacing with optical fiber [26]. The main waveguide section is ~8 mm long and has a cross-sectional dimension of 240 nm × 450 nm while the tapering sections are ~0.3 mm long each. The width at the end of the silicon nanowire is tapered from 450 nm to a tiny tip end of 40 nm so that the guided mode will expand into a polymer waveguide, surrounding the silicon-on-insulator (SOI) waveguide and the taper. The device has an SOI structure, with the silicon waveguide placed on a $SiO_2$/Si substrate. The measured propagation loss is 4.3 dB/cm and the fiber-to-fiber loss of the device is 6.8 dB.

## IV. XPM in a Silicon Nanowire for Packet Switch

XPM is an ultrafast optical Kerr effect, with a response time of a few fs. Fig. 3 shows the operation principle of XPM in a silicon nanowire with subsequent off-center filtering. The pump pulse can modulate the refractive index of the silicon waveguide, which results in phase modulation on the co-propagating continuous wave (CW) probe [27]. The phase modulation will then result in transient chirp on the CW probe. The leading edges of the pump pulse will generate red-shift chirp, whereas the trailing edge of the pump pulse will generate blue-shift chirp. The blue shifted and red shifted sidebands are generated as a result of the chirp. If an off-center filter is used to extract either the blue shifted sideband or the red shifted sideband, the XPM-induced phase modulation can be converted into amplitude modulation. When an RZ-OOK data signal is used as the pump, the generated sideband can pass through the off-center filter in the presence of a "1" bit of the pump, whereas no generated sideband results in no transmission through the off-center filter in the presence of a "0" bit of the pump. Using a CW probe, the XPM in silicon with subsequent off-center filtering has been used for forward error correction supported 150 Gb/s wavelength conversion, 10 Gb/s tuneable wavelength conversion, 40 Gb/s regenerative wavelength conversion and 160 Gb/s all-optical data modulator [27]–[30]. If the probe is gated in time (with a gating time slightly larger than the packet duration), XPM in silicon with subsequent off-center filtering, can be used for packet switching with ultrafast response time. Fig. 4 shows an illustration of packet switch based on the XPM in silicon with subsequent off-center filtering using gated probe light. For the $1 \times 1$ packet switch, 1 out of 4 data packets ($\lambda_D$) is switched out at the wavelength of $\lambda_C + \Delta\lambda$ when the control signal ($\lambda_C$) is set to be on. When the control signal is off, no light is generated at the wavelength of $\lambda_C + \Delta\lambda$. For the $1 \times N$ packet switch, a wavelength selective switch (WSS) with different wavelengths at different outputs should be used. When the wavelength of the control signal is fast tuned, the incoming packet could be switched to different outputs of the WSS. The tuning speed of the tunable laser depends on the guard band between packets, which is typically on the order of several nanoseconds to several microseconds. This requirement of tuning speed could be relaxed if the granularity of the packet becomes large, i.e., introducing large enough guard band (~$\mu$s) by switching a long packet or several aggregated short packets. If the first packet of four data packets needs to be switched to port 1 of the WSS, the wavelength of the control signal should be tuned to be $\lambda_{C1}$; if the second packet of four data packets needs to be switched to port 4 of the WSS, the wavelength of the control signal should be tuned to be $\lambda_{C4}$. Compared to the $1 \times N$ packet switch based on cascaded MZI switches, which needs N–1 active switch, the XPM based $1 \times N$ packet switch only needs an active fast tunable laser followed by passive filtering. Based on the $1 \times N$ packet switch, the TAW and TAG protocol can be realized, as shown in Fig. 2.

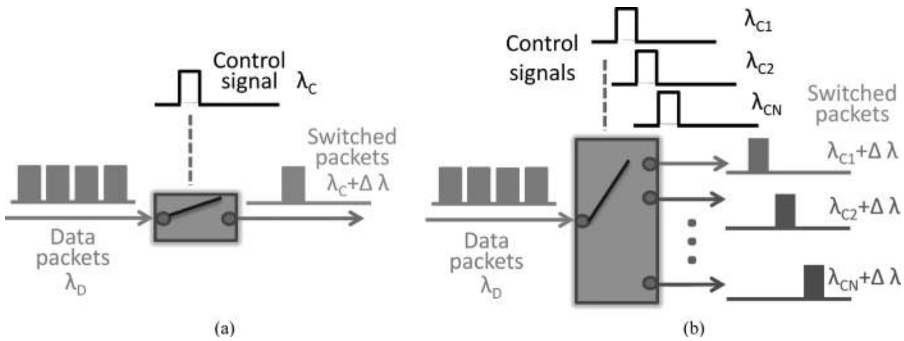


Fig. 4. Illustration of packet switch. (a) One out of four data packets is switched out using $1 \times 1$ packet switch when the control signal is set to be on; (b) One of the input data packets is switched to different path using $1 \times$ N packet switch when the wavelength of the control signal is tuned. Blue box: WSS with different wavelengths at different outputs.

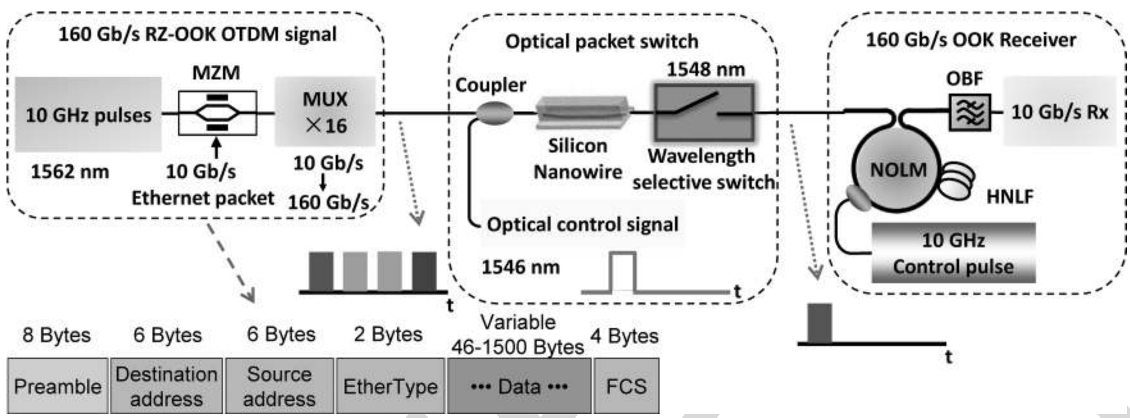


Fig. 5. Experimental setup for the 160 Gb/s all-optical packet switch using a silicon nanowire followed by a WSS.

## V. Experimental Setup

The experimental setup for the 160 Gb/s silicon packet switch is shown in Fig. 5. It mainly includes a 160 Gb/s RZ-OOK transmitter, a $1 \times 1$ silicon based packet switch and a 160 Gb/s on–off keying (OOK) receiver. The erbium-glass oscillating pulse-generating laser produces 10 GHz pulses at 1542 nm with a 1.5-ps full-width at half-maximum pulse width. The spectrum of the pulses is broadened in a 400-m dispersion-flattened highly nonlinear fibre (DF-HNLF, dispersion coefficient $\mathrm{D} =$ $-0.45$ ps/nm/km and dispersion slope $\mathrm{S} = 0.006$ ps/nm$^2$/km at 1550 nm, nonlinear coefficient $\gamma = 10.5\ \mathrm{W}^{-1}\mathrm{km}^{-1}$) due to self-phase modulation [31], [32]. The broadened spectrum is filtered at 1562 nm with a 5-nm optical bandpass filter (OBF) to generate the 10 GHz pulses for the data signal and is also filtered at 1538 nm using a 1 nm OBF to obtain the 10 GHz control pulses used in the OTDM demultiplexing. The generated 10 GHz pulses at 1562 nm are OOK modulated in a Mach–Zehnder modulator (MZM) using a software defined pattern to generate 10 Gb/s Ethernet packets. As shown in Fig. 5, the Ethernet packet with a maximum standardized size of 1518 bytes consists of a preamble, a destination address, a source address, an Ethertype, payload data and a frame check sequence [33]. The packets have duration of 2.19 $\mu$s, consisting of 1.22 $\mu$s of data payload separated by a 0.97 $\mu$s guard band. The generated 10 Gb/s Ethernet packet is multiplexed in time using a passive fiber-delay multiplexer (MUX $\times$ 16) to generate the 160 Gb/s signal.

In the $(1 \times 1)$ silicon based optical packet switch, the generated 160 Gb/s optical packet is amplified by an EDFA, then filtered by a 5 nm OBF and finally launched into the silicon nanowire through a 3-dB optical coupler. The optical control signal is generated from a CW light at 1546 nm, which is modulated by an electrical control signal in a MZM. The electrical control signal is generated according to the BHC of the burst, which has duration of 1.5 $\mu$s and repetition rate of $\sim$114 kHz in order to switch one of the four packets. The optical control signal is also launched into the silicon nanowire through the second input of the 3-dB coupler. Fig. 6 shows the waveforms of the packets and the control signal. The launched average power for the data and the control are 13.5 and 8.5 dBm, respectively, which corresponds to the energy consumption of 140 and 44 fJ/bit. Since the total launched power is well below the two photon absorption (TPA) threshold [6], the TPA and resulting carrier effects are negligible. The polarizations of the data signal and control signal are both aligned to transverse-electric polarizations into the silicon waveguide. The optical packets modulate the refractive index of the silicon waveguide and generate XPM on the control signal. Only if the control signal presents "1" level and aligned in time with a packet, the control signal will be phase modulated by the optical packet and be converted into an amplitude modulated signal by passing through an off-center filter. Note that the refractive index of the silicon waveguide could also be modulated by an electrical signal [8], therefore,

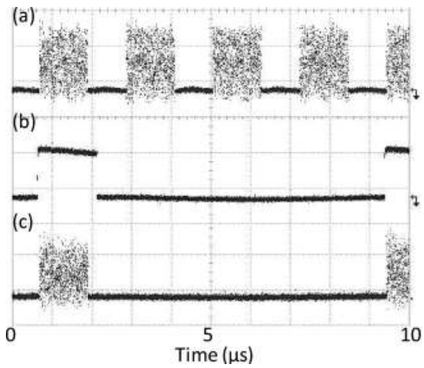


Fig. 6. Oscilloscope traces (a) 160 Gb/s optical packets at the input of the silicon nanowire; (b) optical control signal; (c) one out of four packets switched at the output of the silicon nanowire and WSS.

in principle the scheme could also work if the electrical signal is directly employed on the silicon chip. At the output of the silicon nanowire, a WSS with the center wavelength of 1548 nm is used to filter out the red-shifted sideband of the control signal and select the switched packet.

The 4-to-1 switched 160 Gb/s packet was detected using a 160 Gb/s OOK receiver, which consists of a nonlinear optical loop mirror (NOLM) based OTDM demultiplexer, a 0.9-nm filter, a photo detector (PD) and an error analyzer. The NOLM is used to OTDM demultiplex the 160 Gb/s packet down to 10 Gb/s packets based on the XPM in a 50 m long HNLF. Finally, the demultiplexed 10 Gb/s optical packet was detected using a PD and the performance was evaluated using an error analyzer.

## VI. Experimental Results

Fig. 6 shows the dynamic operation of 160 Gb/s silicon packet switch. When the control plane receives BHC information, a control signal was generated to drive the silicon based all-optical switch. In this case, one of four packets needs to be switched; therefore, the targeted packet was aligned in time with the optical control signal, as shown in Fig. 6(a) and (b). At the output of the packet switch, the targeted packet was successfully switched with an extinction ratio of ~18 dB, as shown in Fig. 6(c). Fig. 7 shows optical sampling oscilloscope (OSO) eye diagrams of 160 Gb/s original packets and 1-of-4 switched packet. The switched packet has an open and clear eye diagram after the packet switch. Actually, some "0" level noise on the original packets was also removed after the $1 \times 1$ packet switch, resulting from the regenerative characteristics of the off-center filtering [29].

The spectra at the input and the output of the silicon nanowire are shown in Fig. 8. XPM on the control signal can be clearly seen (modulation peaks around the control signal) at the output of the silicon nanowire. The blue and red shifted sidebands on the optical control signal were generated from the leading edge and trailing edge of the 160 Gb/s optical packets with the modulation format of RZ-OOK, respectively. A WSS centered at 1548 nm is used to filter out the red-shifted probe light to obtain an amplitude modulated 160 Gb/s signal and separate the switched packet at 1548 nm from the original packet at 1562 nm.

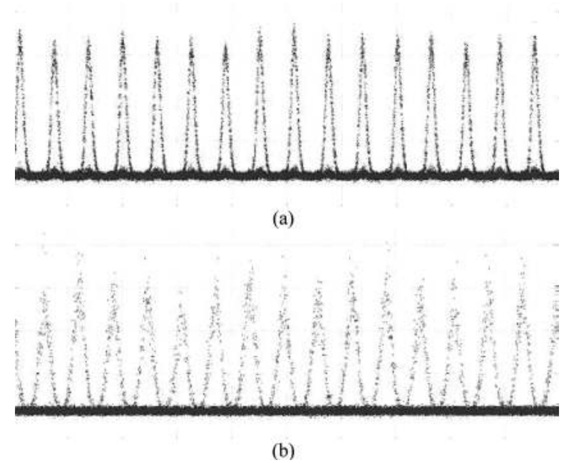


Fig. 7. (a) OSO eye diagrams of 160 Gb/s original packets (b) and 1-of-4 switched packet.

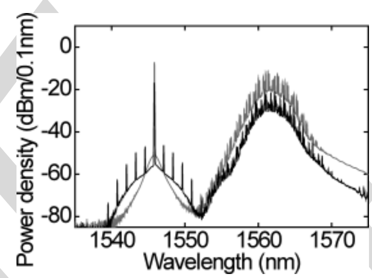


Fig. 8. Optical spectra at the input of the silicon chip (red) and output of the silicon nanowire (black).

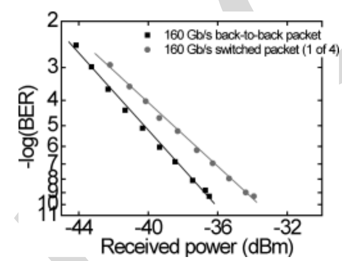


Fig. 9. BER measurements after demultiplexing to 10 Gb/s for the 160 Gb/s back-to-back packet and for the 160 Gb/s 4-to-1 switched packet.

The performance of the silicon based $1 \times 1$ all-optical packet switch for the 160 Gb/s Ethernet packet was evaluated using BER measurements, as shown in Fig. 9. BER curves are plotted for the 160 Gb/s back-to-back packets and for the 160 Gb/s 4-to-1 switched packets. The 4-to-1 switched 160 Gb/s packets achieve an error-free performance (BER $< 10^{-9}$) with a power penalty of ~2.5 dB compared to the back-to-back case. The measured penalty is partly attributed to the pulse broadening due to the filtering effect induced by the WSS, and partly attributed to the OSNR degradation after the packet switch due to the limited phase modulation on the control signal.

## VII. Discussion and Conclusion

We have successfully demonstrated a 160 Gb/s silicon based $1 \times 1$ all-optical packet switch, based on XPM in a silicon nanowire. This scheme could be upgraded to a $1 \times$ N all-optical packet switch if a fast tunable laser is used. The silicon packet switch could be used either for OPS or OBS without optical buffering if the TAW or TAG protocol is used. The 4-to-1 switched 160 Gb/s Ethernet packet shows error free performance (BER $<$ 1E-9), and holds great promise for future photonic switching of ultra-fast data signals.

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