International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 07 Issue: 03 | March - 2023 Impact Factor: 7.185 ISSN: 2582-3930

180 nm FLASH ANALOG TO DIGITAL CONVERTOR

E.SREELAKSHMI[1], B.MOUNIKA[2], B.D.S.L KEERTHANA[3] ,B.SAIGOPAL[4]

[1234]*Students, Dept. of Electronics and Communication Engineering, R.V.R&J.C College of Engineering Guntur, Andhra Pradesh, India*

Abstract - In this paper, Threshold Inverter Quantizer (TIQ) is a novel idea which can effectively replace the reference voltage generator, resistive/capacitive voltage divider network and array of differential comparators in a conventional flash Analog to Digital Converter (ADC) by an internal reference comparator array constructed of Complementary Metal Oxide Semiconductor (CMOS) inverters. The inverter threshold voltage serving as the reference voltage, this architecture claims large improvements in terms of silicon area, power consumption and operating speed. Perturbations due to sensitivity of the inverter threshold voltage to operating temperature/process variations pose impediments in such ADC designs and strongly demand a compensation scheme to such variations. This paper presents a TIQ based flash ADC, with inverter threshold voltage compensation. In this project 5 bit flash adc using TIQ Comparator is designed and simulated using TANNER EDA in 180nm technology.

Key Words: flash, adc, tiq(threshold inverter quantization)

1.INTRODUCTION

Digital signal processing has advanced intensely due to the rapid expansion of science and technology. In the majority of the digital domains, signal processing offers several advantages such as flexibility in design and programmability, reduced silicon area, high accuracy, as well as a smaller amount of power consumption. The design process is cost-effective and faster. Hence it is possible to design a system with a lesser area along with high speed. It is required to have an analog to digital converter that offers much higher speed in wireless communication, image processing, etc.

In last few years the largest portion of electronics industry is dominated by MOS market. It becomes a challenging to design analog circuit reducing its feature sizes, supply voltages as well as transistor channel length. Op amp can easily trade-off between all performance parameters like gain, phase, phase margin, unity gain bandwidth etc. The design can be achieved handling various aspect ratios i.e changing width and length of transistors to be in saturation region so that it can give better performance.

This can be only possible by developing applications that consume less power. Since ADC's act as front-end components in the majority of mixed-signal systems, we focused to design ADC that consumes less power which in turn offers higher speed. We have various types of ADC architectures for instance successive approximation type ADC, Flash type, sigma-delta, etc. Among these Flash ADC is preferred since it offers high speed because of its parallel architecture, the conversion time is not limited by resolution hence these ADC's are utilized in those systems where bandwidth with a wide range and high speed is required.

One single ADC type cannot cover all applications since the performance parameters like sampling rate, power consumption and resolution of an ADC is basically determined by its architecture. Therefore, it is very important to choose an ADC for each particular application.

Different type of ADC's are available like SAR ADC, Dual Slope ADC, Sigma Delta ADC and Flash ADC but among all the se the most commonly used ADC is The Flash adc because of its better tradeoff between its performance metrics. Flash ADC is mainly used for applications which require high speed and low resolution. Flash ADC architectures have been widely studied because of its fast performance among all the ADC's available. It is faster due to its parallel architecture and hence it is also known as parallel ADC.

Flash converter is high speed converter among all other ADCs. It consists of 2N comparators that provide thermometer coded output which is converted to a digital output by an encoder. In high speed ADCs comparator plays an important role for high speed application using minimization techniques. The main disadvantage of flash type ADC is power hungry so the aim is to design low power flash type ADC with low power comparator. The design issues are related to gain, phase, gain bandwidth, resolution, speed, area and power dissipation. Simple two stage opamp with miller capacitance can be used as a high gain comparator. It can be easily operated at low power. A flash ADC constructed of Threshold Inverter Quantizer (TIQ) which utilizes CMOS inverter as a voltage comparator with the inverter switching threshold voltage serving as an internal reference voltage for the comparator was proposed by Tangel et al. This architecture substitute differential amplifier based comparator array by an array of a pair of CMOS inverters connected back to back and eliminates thenecessity of a stable reference voltage source and voltage divider network from the architecture of a conventional flashADC. Properly sized CMOS inverters serving as comparator with internal reference voltage, this architecture offer better speed, area and reduction in static power consumption.Since the switching voltage of Each TIQ module in the comparator array is serving as a distinctive internal reference voltage against which the input signal is compared, its stability

2. DESIGN

To implement N bit flash ADC, we require 2N-1 comparators are needed. Similar to op-amp, the comparator comprises of two inputs where analog input is given to the inverting terminal and reference voltage is applied to non-inverting terminal. Comparators are divided with the help of the resistive ladder network. 2N resistors are utilized to form a resistive ladder network of N bit. Since we have implemented

3-bit, the number of resistors required will be eight. The reference voltage is generated across the resistive ladder network between reference voltage and ground is equally distributed and is differed by the least significant bit. The comparator compares the reference voltage signal with the input analog signal and indicates output as logic high whenever analog input exceeds reference voltage and indicates logic low output when analog input is smaller than reference voltage. The output of comparators forms a thermometer code. Further, we need to translate thermometer code into binary code. The output generated mainly depends on the resolution. But the major disadvantage is as the resolution increases, the number of comparators required will get increases. For example if we need to implement flash ADC of 9 bit, we need 511 comparators which occupy a huge die area and dis sipates a large amount of power. Hence we need to reduce the power and area of flash ADC as they are major constraints.

2.1 TIQ Comparator

In this project, a TIQ comparator based Flash ADC is designed. Figure below shows the threshold compensated TIQ module. The scheme includes three CMOS inverter structures. A In this self-tuning topology, a DC feedback loop is utilized for self-correcting the inverter threshold voltage. The working of the threshold self tune technique is explained bellow. A resistive divider comprising R0 and R1 is used to set the threshold voltage of the master and slave inverters. The main part of the threshold compensated TIQ-comparator is the master inverter connected to the power rails through an NMOS (NM3) and a PMOS (PM3).

These two transistors are biased in their linear (triode) operating region and acting as a negative feedback arrangement in this architecture. The gate terminals of these transistors are driven by the output terminal of the master inverter and effectively working as voltage controlled resistance, the resistances of which are controlled by the output voltage of the master inverter.

The Slave inverter is implemented with the same aspect ratios as that of the master. With its input set to a required threshold voltage, the master inverter generates the necessary control voltage to self correct the resistance of the two MOSFETS connected to the power rails. The negative feedback loop acting as a self correcting mechanism and enables the circuit to maintain the pre-set switching threshold of the master and slave inverters at the set value, irrespective of process or temperature deviations.

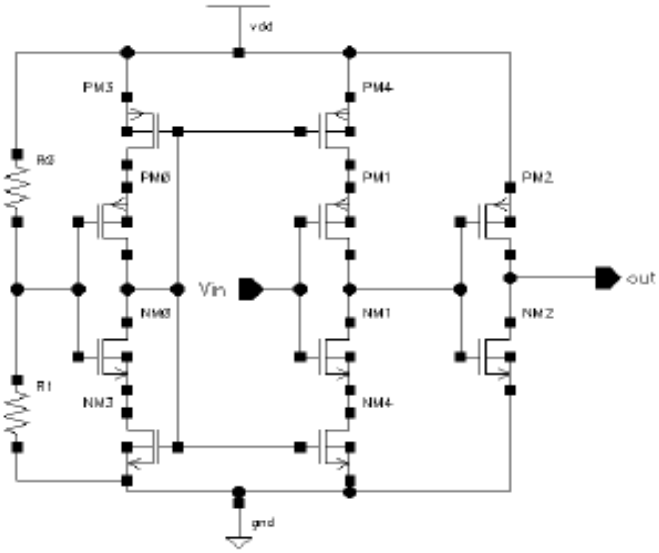

Fig -1: Schematic of tiq comparator

2.2 Design of Encoder

Thermometer code can be translated to binary code in different ways. The name thermometer code is given because the output of the comparators looks like thermometer reading that is as the value increases the number of ones goes on increasing same like the mercury level which increases as temperature increases. There are different types of encoders to convert thermometer code into binary code for instance Wallace tree encoder, encoder design utilizing mux, and encoder using xor as well as ROM encoder. Each of these encoders has its own advantages and disadvantages.

Encoder designed using Mux operates on the simple logic that is if half of the thermometer code represents logic high the most significant bit in binary code is also high. The value corresponding to 2n-1 represents MSB in the binary output. Again this thermometer code is classified into two codes to find next binary output. A select line of the second stage Mux is obtained from the preceding stage mux output. The procedure is continued till the end of the last 2:1 mux and the least significant bit of binary output is obtained. Even if resolution increases we can implement an encoder using this 2:1 mux easily with less area and less power consumption.

. Since it is a 5 bit flash ADC, it requires 32 bit TIQ Comparator array and 32-bit mux based encoder circuit.

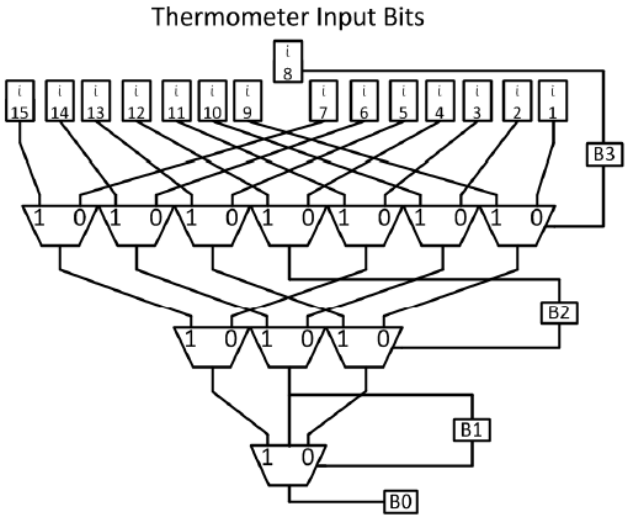

Fig -2: MUX based Encoder

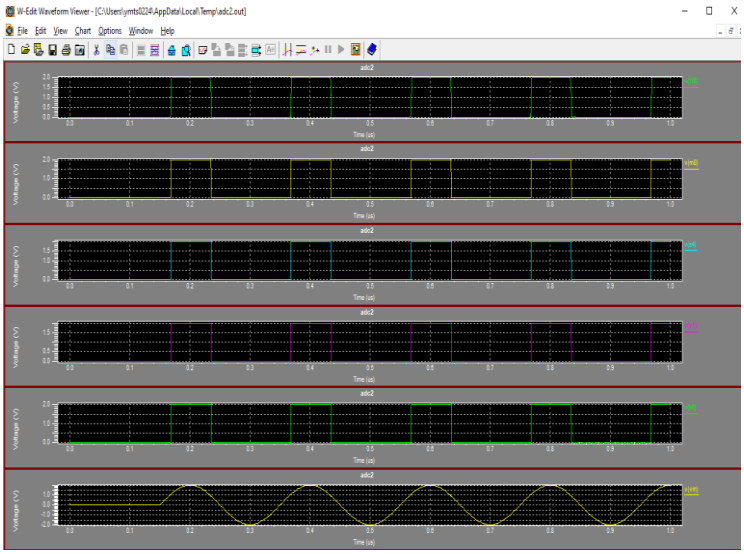

Fig -4: Output Waveform of Flash ADC

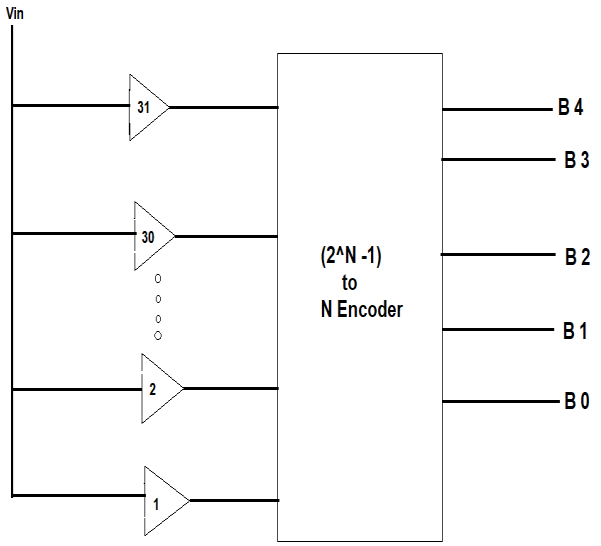

Fig -3: Overall ADC Architecture

2.3 SIMULATION AND RESULTS

Analog-to-digital converters (ADCs) are needed in all applications, which interface with the analogue world and exploit the digital processing of data. As digital processing is more and more gaining ground over analogue signal processing, the importance of ADCs correspondingly increases. The Flash type ADC, also known as Direct Conversion ADC, uses a bank of comparators, operating in parallel to achieve a high data conversion rate. In this paper, a 5-BIT flash ADC is designed using a TIQ based comparator circuit, thermometer to binary converter. All the designs were implemented using 180 nm technology in Tanner EDA

AREA REPORT

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Device and node counts:
          MOSFETs - 632                MOSFET geometries - 8
              BJTs - 0                             JFETs - 0
           MESFETs - 0                           Diodes - 0
        Capacitors - 0                         Resistors - 64
        Inductors - 0                    Mutual inductors - 0
Transmission lines - 0      Coupled transmission lines - 0
  Voltage sources - 2                  Current sources - 0
             VCVS - 0                              VCCS - 0
             CCVS - 0                              CCCS - 0
  V-control switch - 0                 I-control switch - 0
    Macro devices - 0      External C model instances - 0
      HDL devices - 0
       Subcircuits - 0              Subcircuit instances - 58
```

DELAY REPORT

*BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

delay=2.0062e-009
Trigger=1.6667e-007
Target=1.6867e-007

*END NON-GRAPHICAL DATA

POWER REPORT

*BEGIN NON-GRAPHICAL DATA

Power Results
v5 from time 0 to 1e-006
Average power consumed -> 7.132766e-003watts
Max power 1.444820e-002 at time 7.6806e-007
Min power 7.008431e-003 at time 9.68394e-007

*END NON-GRAPHICAL DATA

3. CONCLUSIONS

Analog-to-digital converters (ADCs) are needed in all applications, which interface with the analogue world and exploit the digital processing of data. As digital processing is more and more gaining ground over analogue signal processing, the importance of ADCs correspondingly increases. The Flash type ADC, also known as Direct Conversion ADC, uses a bank of comparators, operating in parallel to achieve a high data conversion rate. In this paper, a 5-BIT flash ADC is designed using a TIQ based comparator circuit, thermometer to binary converter .All the designs were implemented using 180 nm technology in Tanner EDA.

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