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A 5 GS/s 7.2 ENOB Time-Interleaved VCO-based ADC Achieving 30.5 fJ/cs

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Technology scaling has been very beneficial for digital circuits both in terms of speed and power. Traditional analog techniques however are challenged by the ever-decreasing supply voltages. Highly digital VCO-based ADCs are able to benefit directly from improved digital performance [1], however the resolution and sampling rate of state-of-the-art VCO-based designs are insufficient for most applications. This paper presents a faster and more efficient VCO-based ADC architecture based on an improved high-speed, low-power ring oscillator and an asynchronous counting strategy. The architecture is 8x time-interleaved and combined with on-chip calibration. The design was implemented in 28nm CMOS and achieves 45.2 dB SNDR (7.2 ENOB) near Nyquist at 5 GS/s while consuming only 22.7 mW, resulting in a Walden FOM of 30.5 fJ/cs. The core area is only 0.023 mm². These results demonstrate that VCO-based ADCs are a viable choice for next-generation Ethernet and high-speed wireless communication.

Figure 1 shows the ADC architecture. The 5 GHz clock is divided into 8 low-speed, phase-shifted sampling clocks. A timing diagram of the sampling process is shown in figure 4 (top). Each channel samples the input onto a 300 fF capacitor using a bootstrapped switch, while the VCO-based ADC core is connected to V_{cm}. The pseudo-differential implementation rejects common-mode interference and even order distortion. During the hold phase, the sampled voltage is presented to the ADC core, which consists of a voltage-controlled ring oscillator (VCRO) connected to a counter. The input voltage is used as the control voltage of the VCRO. The state of the VCRO and counter is sampled by a bank of sampling flip-flops. The sampled counter value corresponds to the number of cycles that have elapsed, while the sampled VCRO state provides extra fractional (LSB) information which improves the resolution. Once decoded and combined, the resulting value is proportional to the integral of the VCRO frequency. During each tracking phase, the state of the core is sampled and compared to the previous state. The difference is proportional to the VCRO frequency which in turn is determined by the input voltage. The non-linearity, offset and gain error of the VCRO tuning curve is calibrated using a 32-segment lookup table followed by a linear interpolator.

Figure 2 shows the VCRO architecture and corresponding tuning curve. The VCRO has 8 stages and is based on current-starved inverters. It is implemented differentially and makes use of feedforward cross-coupling to suppress common-mode gain without the use of differential pairs. The feedforward path results in a higher oscillation frequency which improves the resolution of the ADC. A single current starving tail transistor is used for the entire oscillator instead of separate transistors for each inverter. The sensitive current starving transistor is moved out of the signal path, so it can be upsized to improve matching and reduce noise. The tail transistor also isolates the ring oscillator from the supply voltage, since the oscillation frequency is determined solely by the current flowing through the tail transistor. As a result, this VCRO design is significantly less sensitive to supply noise. The resulting VCRO has a usable tuning range of 2 – 12.3 GHz with good linearity and an average power consumption of only 0.5 mW.

Previous VCO-based ADC designs used a low-speed ring oscillator with a large number of stages, either because they did not include a counter and needed a large number of output phases to obtain the required resolution, or

because the oscillation frequency had to be reduced to be compatible with a slow, synchronous counter. In both cases, the large number of stages would have resulted in high mismatch and a poor INL, so the transistors of the oscillator had to be upsized to reduce the mismatch, which increased the power consumption. Additionally, the large number of stages required an equally large number of sampling flip-flops, again resulting in increased power consumption.

The design presented in this paper uses a different approach: a fast asynchronous counter with a maximum clock frequency of 15 GHz is used. This counter, shown in figure 3, is an 8-bit ripple counter formed by four cascaded divide-by-4 blocks. Since only the first divider operates at the full clock speed, this circuit is very energy-efficient. Sampling the counter value is challenging though: since the counter value changes asynchronously with respect to the sampling clock, there is a risk that the sampled value will contain a mixture of old, new and metastable bits. The problem is exacerbated by the propagation delay of the dividers: when operating at the maximum clock frequency of 15 GHz, the propagation delay of the entire counter is much longer than one clock cycle.

For synchronous counters, such a problem can be solved with double sampling [1]: the counter value is delayed by a half clock cycle, and both the original and delayed value are sampled. At any point in time, at least one of these two values will be uncorrupted by transitions. The correct counter value can then be selected based on the clock value, which is also sampled.

In this work, the same principle is extended to asynchronous counters by treating the reconstructed value of each divider as the clock for the next divider. Figure 3 shows the schematic of this asynchronous double sampling decoder, and figure 4 (bottom) shows the corresponding timing diagram. For each divider, muxes are used to select the sampled signals which are guaranteed to be stable. For the first divider, this selection is made based on the state of the counter clock (VCRO output). For the remaining dividers however, the reconstructed value of the previous divider is used for this selection, in order to avoid errors due to the propagation delay of the dividers. This strategy avoids metastability errors even when the total propagation delay is longer than one VCRO cycle. With four extra XOR gates (shown only in figure 3), the state of the dividers can be converted to a binary value, which makes the asynchronous counter behave just like a synchronous counter operating at 15 GHz.

The calibration parameters for each channel are determined by using a 5 MHz sine wave as a test signal. These parameters are then loaded into the chip and used for all other measurements. Thanks to the efficient lookup table and interpolation-based approach, the power required for on-chip digital calibration is only 2.7 mW. Sampling time mismatch is corrected using a tunable delay in the clock path (as in [3]).

Measurement results are shown in figure 5. At 5 GS/s, the SNDR peaks at 46.7 dB and drops to 45.2 dB at the Nyquist frequency. The SFDR peaks at 60.3 dB and drops to 57.1 dB at the Nyquist frequency. The SNR is 51.0 dB. The total power consumption (including clock management and calibration) is 22.7 mW when using a 1.0 V analog and 0.85 V digital supply. As the clock frequency is reduced, the effective resolution of the VCO-based core increases since more time is available for integration, and the SNDR gradually increases up to 49.8 dB at 2 GS/s. Thermal noise becomes more dominant in this range. At 1 GS/s the bootstrap capacitor experiences significant charge leakage, and the resulting distortion from the sampling switch limits the ADC performance.

Figure 6 compares the performance of this work to several state-of-the-art ADC designs. Thanks to the energy-efficient high-speed VCRO and counter, the presented architecture achieves a resolution and speed similar to traditional designs, yet with a significant power and area reduction. A die photo is shown in figure 7. These results demonstrate that VCO-based ADCs are competitive with traditional designs for high-speed, medium-resolution

applications.

Acknowledgements:

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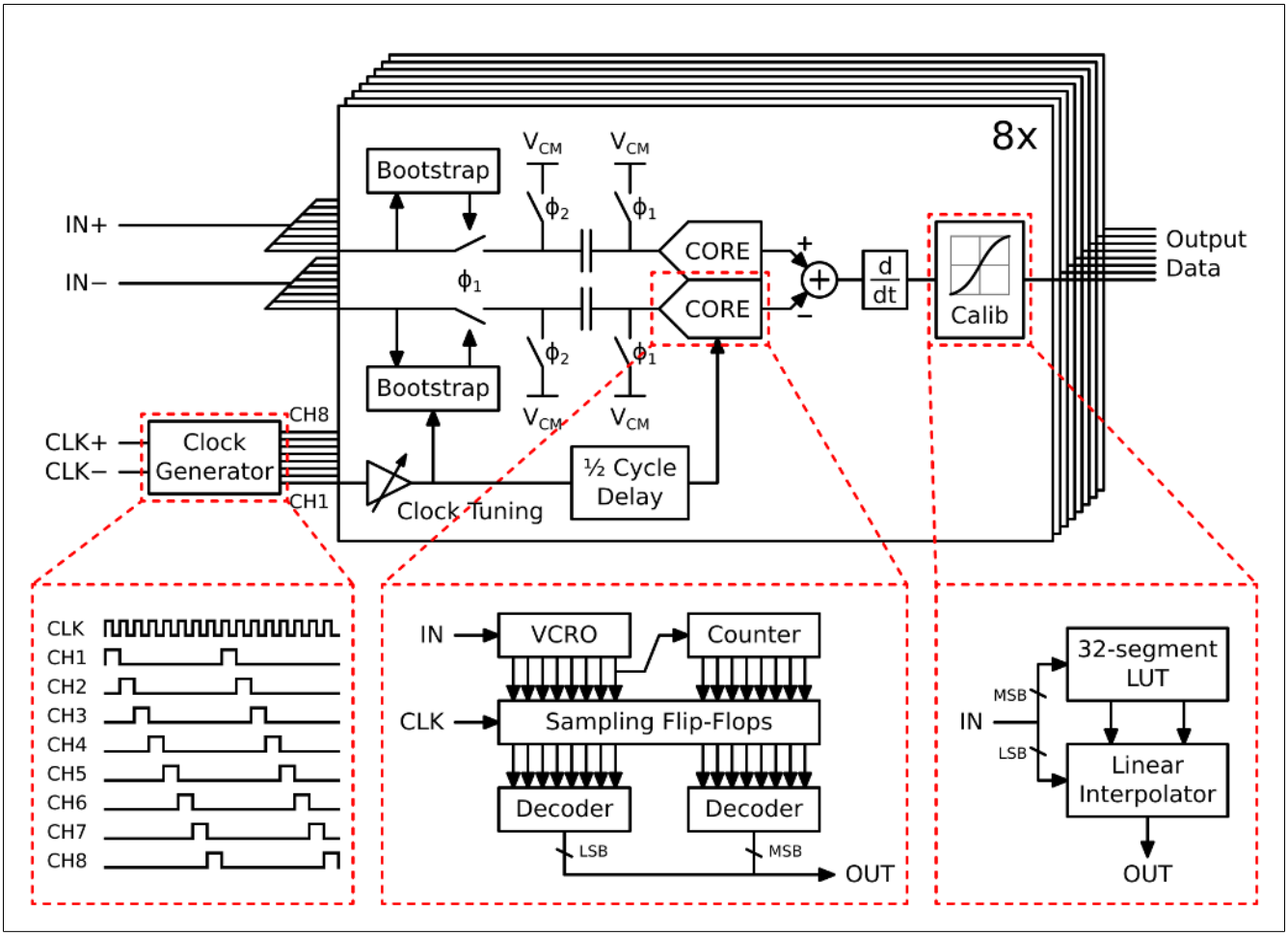


Fig. 1: High-level ADC architecture with detailed view of clock generation, VCO-based ADC core, and on-chip digital calibration.

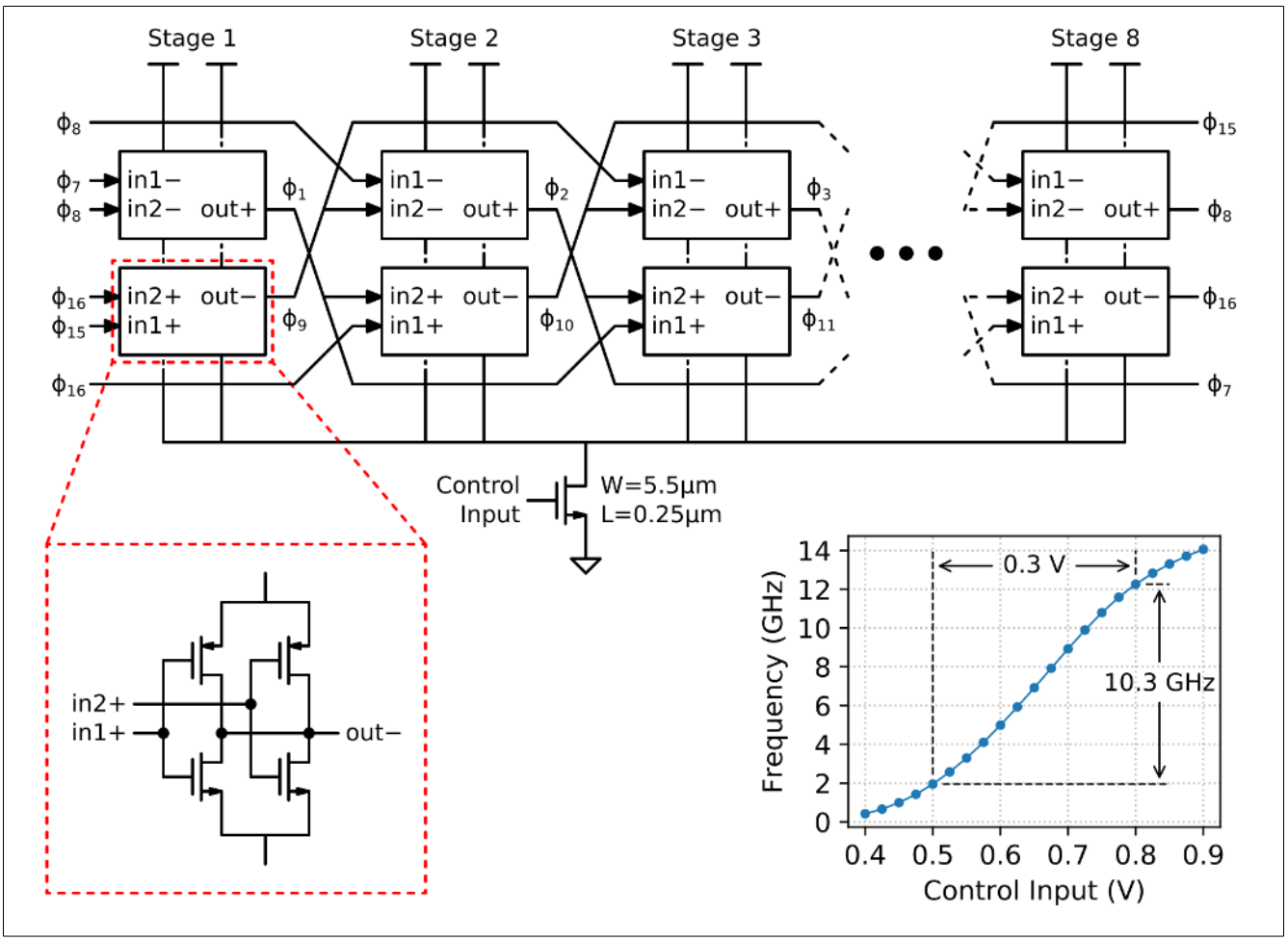


Fig. 2: High speed voltage-controlled ring oscillator (VCRO) with feedforward cross-coupling and shared tail transistor, and the corresponding tuning curve.

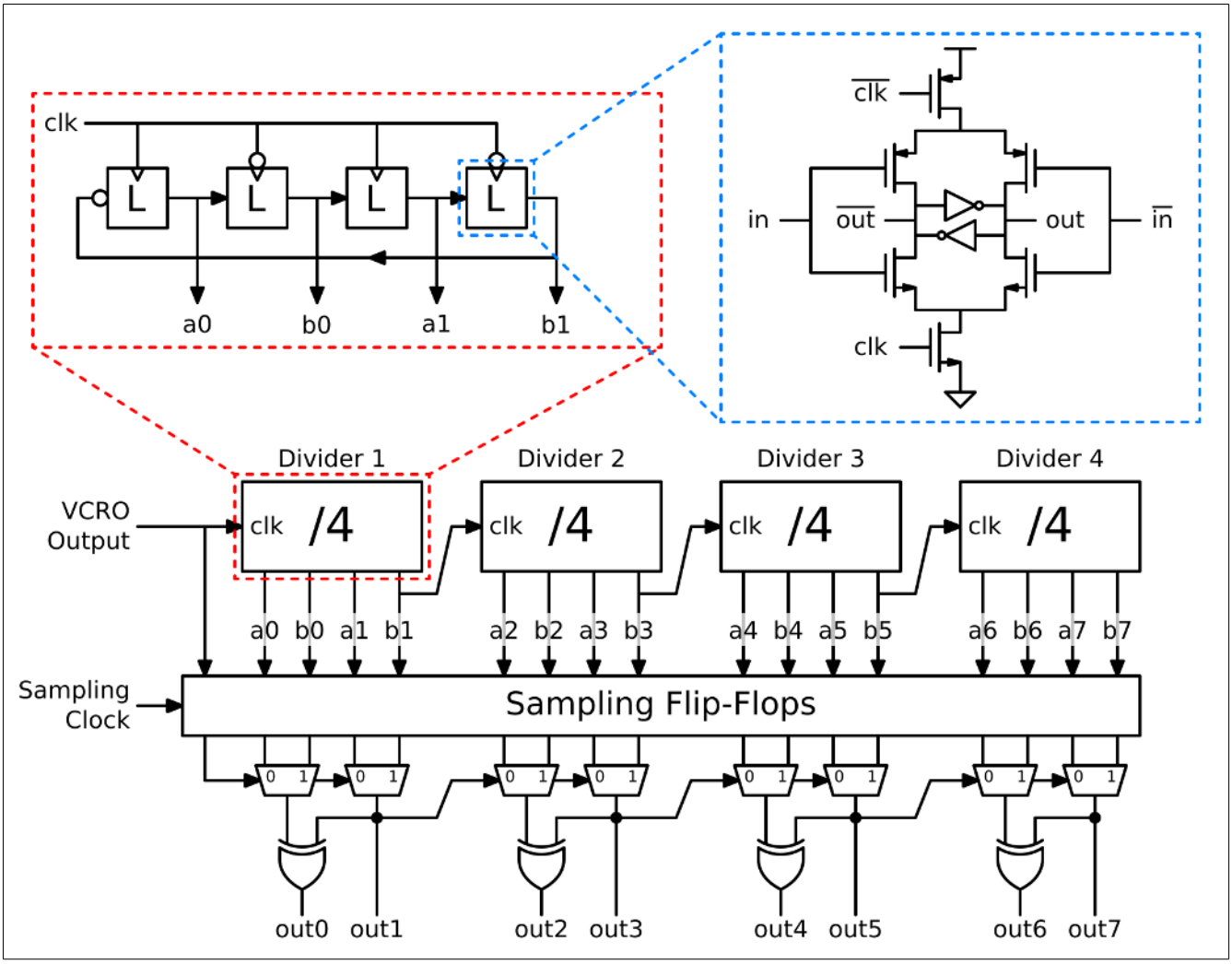


Fig. 3: Asynchronous counter with asynchronous double sampling decoder.

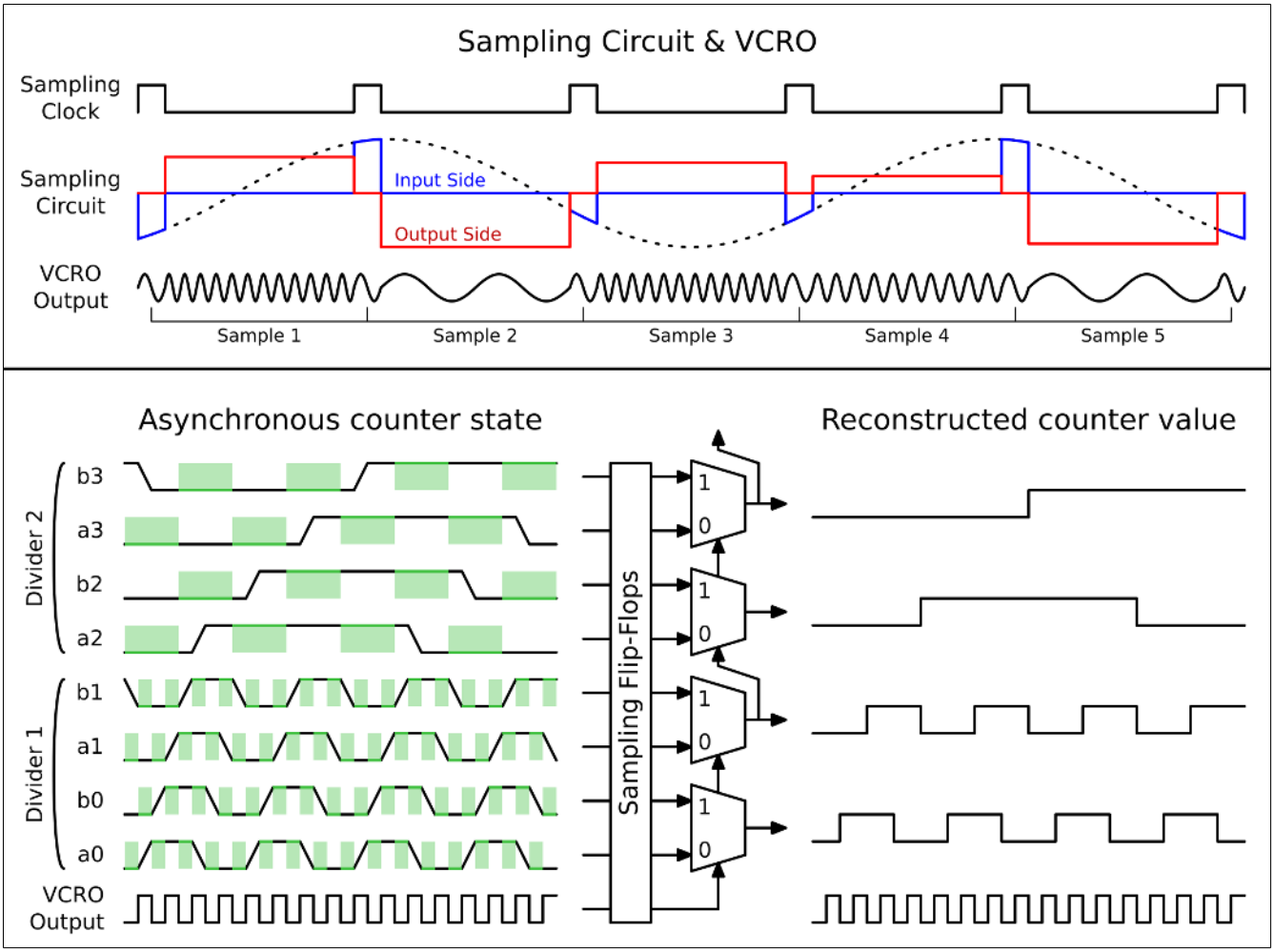


Fig. 4: Timing diagram of the sampling circuit and VCRO (top) and asynchronous counter and decoder (bottom). The decoder selects only signals that are guaranteed to be stable (shaded areas).

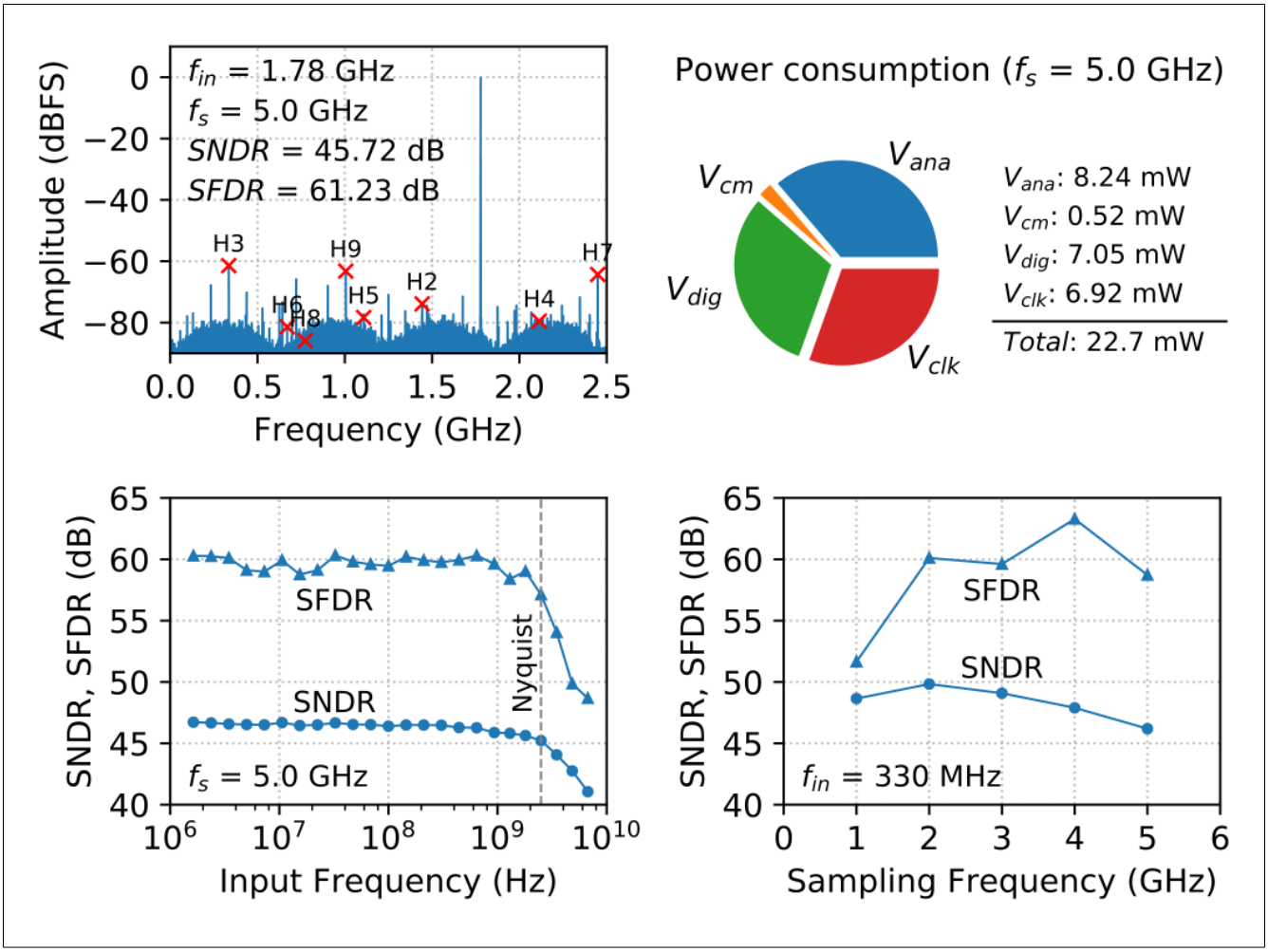
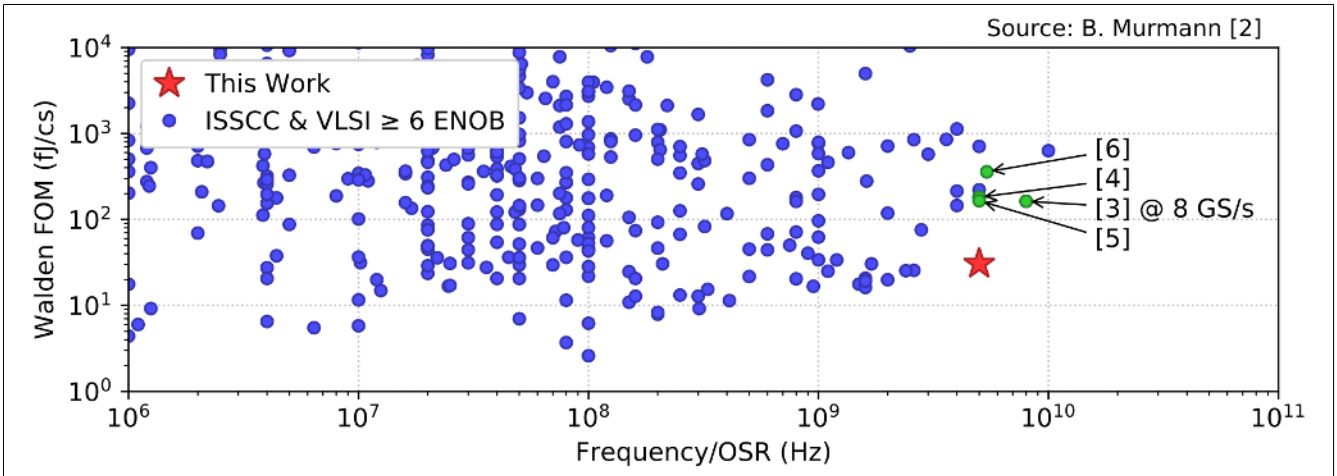


Fig. 5: Measurement results: spectrum for single-tone input, power consumption breakdown and SNDR/SFDR as a function of input and sampling frequency (average of 3 samples).



	This Work	Keane [3]	Brandolini [4]	Fang [5]	Wu [6]
Published	—	ISSCC 2017	ISSCC 2015	CICC 2015	VLSI 2013
Architecture	TI VCO	TI SAR	TI Pipe/SAR	TI SAR	TI Pipe
Technology	28nm	28nm FDSOI	28nm	28nm	28nm
Supply (V)	1.0/0.85	1.8/1.0/0.8	1.0	1.0	1.8/0.9
Sample Rate (GS/s)	5.0	5.0	5.0	5.0	5.4
Interleaving	8x	16x	2x/8x	12x	2x
Power (mW)	**22.7**	150	150	76	500
SNDR (dB)	45.2	51.7	46.1	42	50
SFDR (dB)	57.1	59.2	58.5	54.4	65
Walden FOM (fJ/cs)	**30.5**	95.5	181.9	165	358.4
Schreier FOM (dB)	**155.6**	153.9	148.3	147.2	147.3
Core Area (mm^2)	**0.023**	0.184	0.45	0.57	0.4

Fig. 6: Comparison with state-of-the-art ADCs achieving at least 6 ENOB [2-6]. There are no other VCO-based ADCs that even approach the presented results.

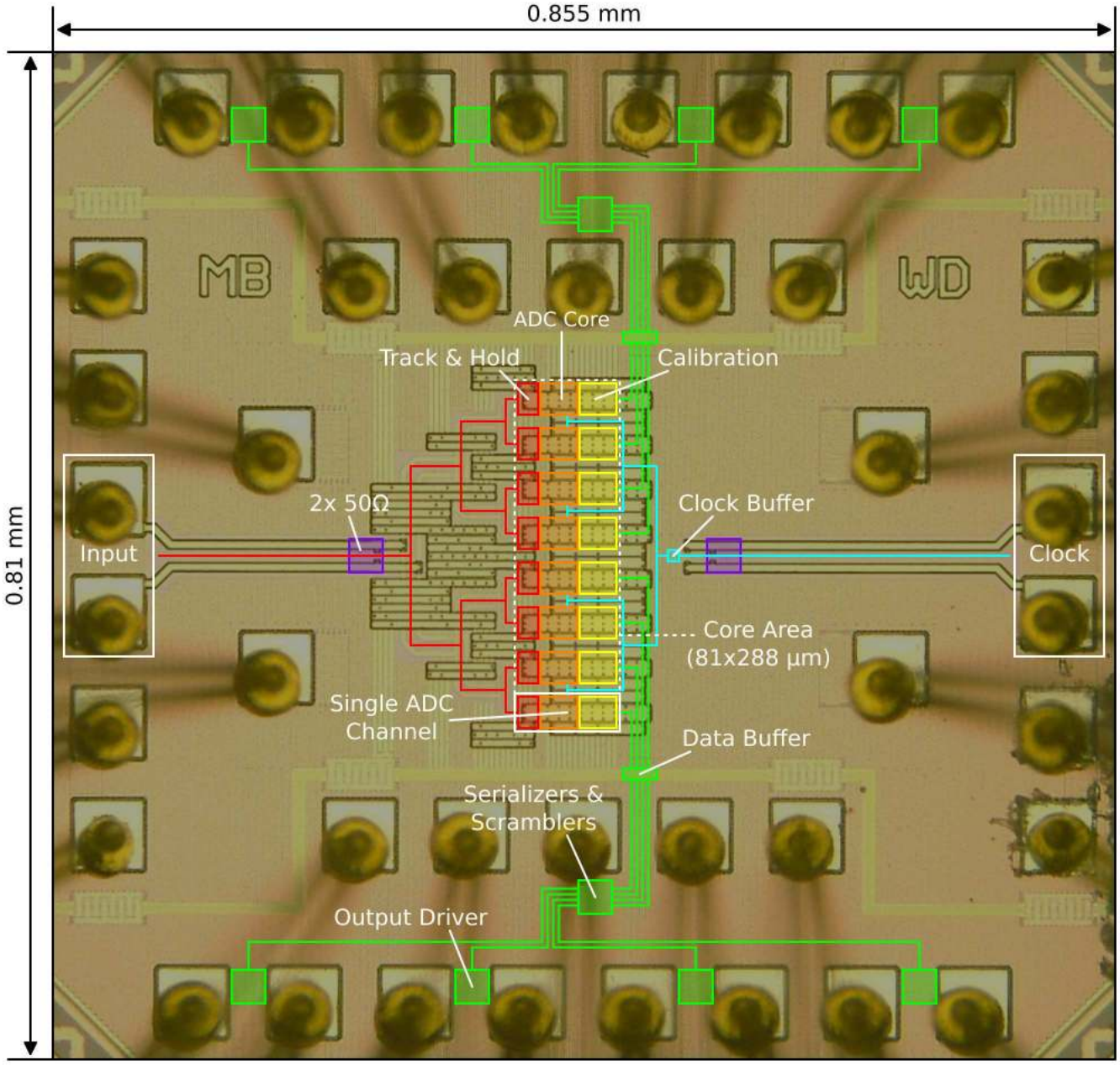


Fig. 7: Die photo with important functional blocks highlighted.