20.8 A 20mW GSM/WCDMA Receiver with RF Channel Selection

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Recent work on RF receivers has exploited N-path filters to address two critical issues, namely, blocker tolerance and high RF selectivity [1,2]. However, these designs face three drawbacks: (1) the low-noise amplifier (LNA) incorporates a G_m stage that, even with a virtual ground at its output nodes, must still withstand strong blockers at its input; (2) the low-order filter transfer function does not provide sufficient selectivity in narrow-band applications such as GSM or WCDMA; (3) they consume roughly 60mW around 2GHz.

This paper introduces a wideband receiver that realizes filtering at the LNA *input* (rather than output) so as to achieve selectivity even for GSM channels. The receiver can tolerate a 0dBm blocker at 23MHz offset and its RF channel selection devices can be readily configured to operate with WCDMA or IEEE802.11b/g as well.

In order to describe the receiver's operation, we begin with the simplified view in Fig. 20.8.1, where an LNA with resistive feedback ensures proper input impedance matching [3]. If an N-path notch filter [4,5] is placed around the amplifier, the resulting Miller multiplication of C_F manifests itself at the input *outside* the notch bandwidth, thereby providing selectivity. Unlike the passive topology in [5], we insert one switch on each side of C_F to allow its parasitic, C_P, to be upconverted and not directly load the LNA input or output. An important benefit of the Miller effect is that it reduces the on-resistance of the feedback switches proportionally, improving the out-of-notch rejection. As a result, the power consumption of the LO distribution network is significantly reduced. The notch bandwidth thus created still exceeds several MHz and hence is inadequate.

In the next step, we consider a three-stage implementation of the LNA [3] and recognize that the latter stages tend to saturate at high blocker levels, allowing less Miller multiplication of C_F. We therefore add a local notch filter, bank 2, around the first stage. Nonetheless, the Miller multiplication produced by the two notch filters still yields a gradual roll-off. In order to increase the selectivity, we seek a "super-Miller" effect, i.e., one creating a multiplication factor that *rises* with frequency. To this end, we add a third notch filter, bank 3, including a multi-stage amplifier, A_2, that contains two zeros near the origin. The overall arrangement produces a flat response within the channel bandwidth and a sharp drop beyond it. The bandwidth is programmed by the feedback capacitors in banks 1, 2, and 3, and the two zeros in A_2.

The various loops around the LNA raise stability concerns, particularly with respect to the bandwidth necessary for A_2. Fortunately, bank 1 and bank 2 help stabilize the loop even if each A_2 is biased at a current of 385μA. This is in contrast to the topology in [2], which requires 5mA of bias in each all-pass amplifier in the feedback path. Moreover, the greater stability permits a loop gain of 50dB for capacitor multiplication, another point of contrast to the 20dB loop gain in [2]. The S_{11} measurements of our prototype confirm the stability of the front end.

An interesting and unique issue that arises in the architecture of Fig. 20.8.1 is that the total delay around the loop - due to the LNA's stages and A_2's stages – slightly *shifts* the center frequency of the channel-selection bandpass response. This is because the delay alters the phase of the signal returning through the N-path filters, thus changing the Miller multiplication factor to a complex value and hence forcing the response to reach a peak slightly away from the LO frequency. Fortunately, this effect can be removed through the use of polyphase signaling: as depicted in Fig. 20.8.2, each A_2 amplifier is decomposed into two so that a fraction of the feedback signal can be injected from one branch to the adjacent branch and compensate for the phase shift.

The quadrature baseband signals are available within all three banks. Since the broadband LNA noise at the LO harmonics folds to the baseband, it is desirable to exploit harmonic-reject (HR) mixing [6]. As shown in Fig. 20.8.2, the downconvered signals in bank 1 are sensed by properly-ratioed G_m stages and combined. In contrast to conventional HR mixers that operate with overlapping phases, this design must perform harmonic rejection by means of nonoverlapping clocks and, consequently, employs weighting factors of 1 and $1+\sqrt{2}$ rather than 1 and $\sqrt{2}$. This arrangement suppresses the third and fifth harmonics, thus reducing the noise figure, according to simulations, by about 3dB. The Q-channel mixing can be performed similarly.

The generation and distribution of eight LO phases with 12.5% duty cycle for the N-path filters can potentially consume a high power, e.g., 36mA at 2.7GHz in 40nm technology [1]. We propose an approach that reduces the total power to 6mA at 2GHz in 65nm technology. Illustrated in Fig. 20.8.3, the idea is to combine the phases at the output of two cascaded ÷2 stages by means of simple combinational logic. For example, an AND gate, G_1, accepts $4f_{LO,0}$, $2f_{LO,90}$, and $f_{LO,135}$ signals to generate a clock with 12.5% duty cycle. Sharing some nodes for proper operation, eight such AND gates produce the eight phases that drive the switches. According to simulations, this arrangement exhibits a phase noise of -165.7dBc/Hz at 20MHz offset owing to its simplicity.

The receiver has been fabricated in TSMC's 65nm digital CMOS technology. Shown in Fig. 20.8.7 is a micrograph of the die, whose active area measures $0.82mm^2$. The capacitors in all banks are programmable through an on-chip serial bus. At 2GHz, the LNA draws 8.6mA, the Miller amplifiers (A_2's) a total of 1.5mA, the baseband combining amplifiers in Fig. 20.8.2 a total of 1mA and the LO generation circuit of Fig. 20.8.3, 6mA.

Figure 20.8.4 plots the measured RF-to-baseband gain as a function of the baseband frequency for three different settings. The 3dB bandwidth varies from 200kHz to 10MHz. We note that the GSM setting provides an attenuation of 15dB in the middle of the alternate adjacent channel. (A layout error does not allow switching in enough capacitors to further reduce the bandwidth.) For the WCDMA setting, the attenuation reaches 16dB in the middle of the alternate adjacent channel.

Figure 20.8.5 shows the measured noise figure (NF) vs. the input blocker level at 23MHz offset, indicating a degradation of 2.5dB as the latter reaches 0dBm. About 0.5dB of this degradation arises from the noise floor of the blocker. This figure also plots the NF vs. the baseband frequency for the exacting requirements of GSM and WCDMA. The measured LO leakage to the antenna falls below -67dBm at 2GHz.

Figure 20.8.6 summarizes the measured performance of our receiver and compares it with the state of the art.

Acknowledgments:
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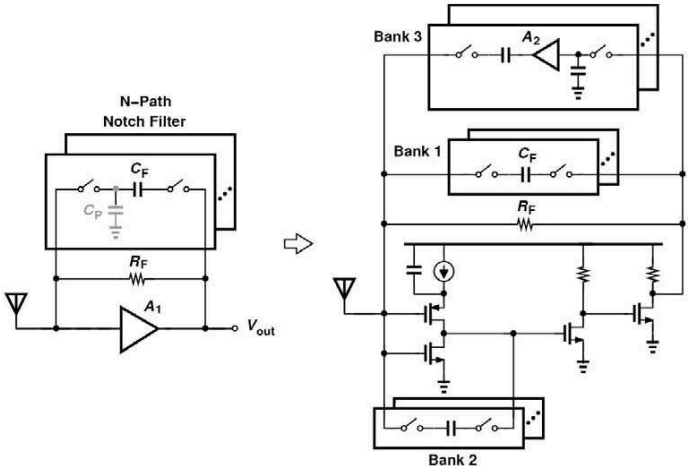

Figure 20.8.1: Channel-selection filtering in LNA by means of N-path filters.

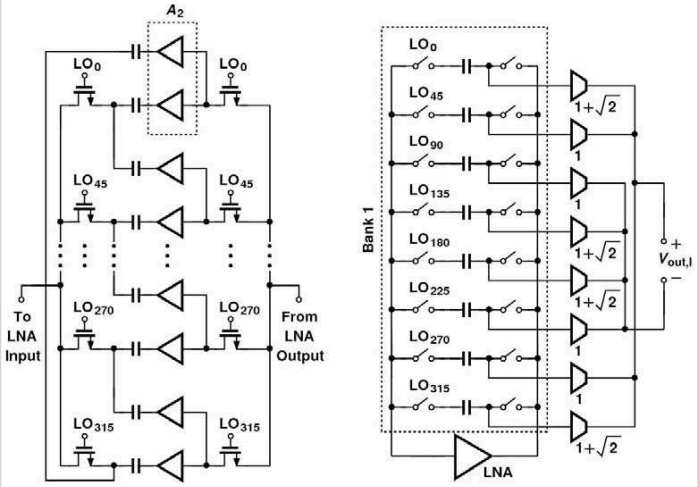

Figure 20.8.2: Bank 3 implementation and harmonic-reject mixing.

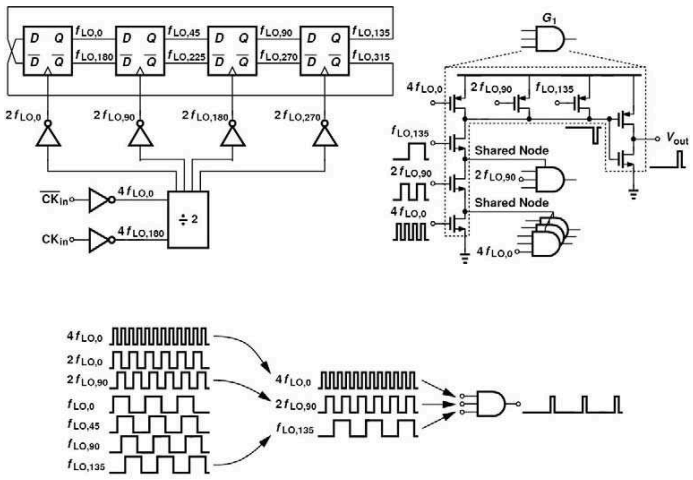

Figure 20.8.3: 8-phase clock-generation circuit.

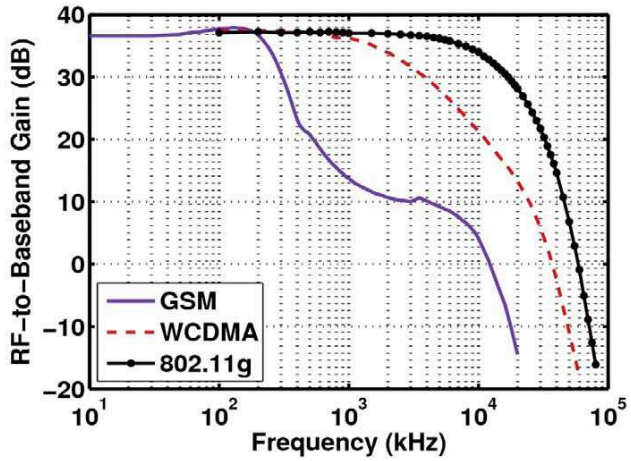

Figure 20.8.4: RF-to-baseband gain for various standards.

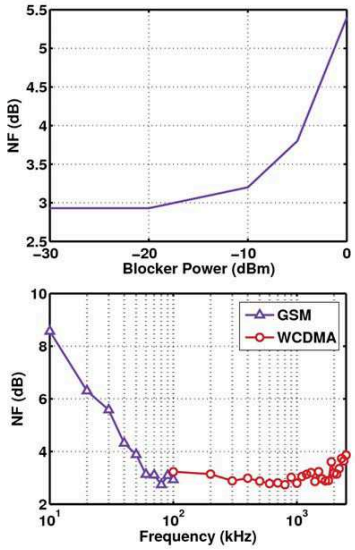

Figure 20.8.5: Measured NF vs. blocker level and vs. baseband frequency.

	[1]	[2]	[7]	This work
Input Frequency [MHz]	80 ~ 2700	1000 ~ 2500	1800 ~ 2400	50 ~ 2500
Channel Bandwidth [MHz]	N/A	5	N/A	0.4 ~ 20
Gain [dB]	72	30	45.5	38
NF [dB]	1.9	7.6	3.8	2.9
NF with 0-dBm Blocker [dB] (at Given Offset)	4.1 (80 MHz)	N/A	7.9 (20 MHz)	5.4 (23 MHz)
Out-of-Band-IIP3 [dBm]	13.5	12	18	10
Active Area [mm^2]	1.2	< 0.06	0.84	0.82
Supply Voltage [V]	1.3	1.2	1.2/1.8	1.2
Power Consumption [mW]	65 (2 GHz)	62[1]	35[2] (2 GHz)	20 (2 GHz)
CMOS Technology	40 nm	65 nm	40 nm	65 nm

[1]Excluding clock circuitry [2]With a 1.8 V supply for LO divider

Figure 20.8.6: Performance summary and comparison.

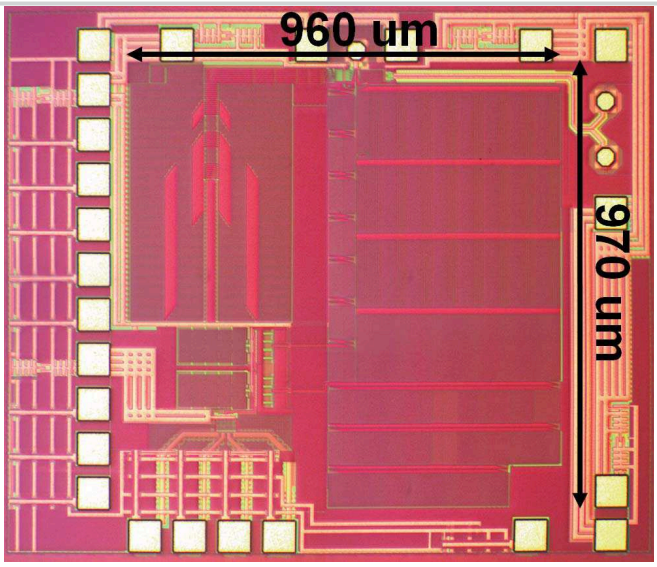

Figure 20.8.7: Die micrograph.

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