210-GHz InAlN/GaN HEMTs With Dielectric-Free Passivation

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***Abstract*—Lattice-matched depletion-mode InAlN/AlN/GaN high-electron mobility transistors (HEMTs) on a SiC substrate were fabricated, for the first time, with a dielectric-free passivation (DFP) process in which the device access region was treated by O_2/Ar plasma. Similar to dielectric passivation using SiN and Al_2O_3, the plasma treatment can effectively shorten the gate-length extension. As a result, the current gain cutoff frequency f_T of a 60-nm rectangular-gate HEMT increased from 125 to 210 GHz after the plasma DFP; this RF performance is among the highest reported f_T for GaN-based HEMTs. The device showed a dc drain current density of 2.1 A/mm and a peak extrinsic transconductance of 487 mS/mm after DFP. The $L_g - f_T$ product of 12.6 GHz $\cdot$ μm is among the highest reported for a gate-physical-length-to-barrier-thickness aspect ratio of 5.6. Small gate lag and drain lag are observed in pulsed I–V measurements with a 300-ns pulsewidth.**

***Index Terms*—AlN, dielectric, GaN, gate-length extension, HFET, high-electron mobility transistor (HEMT), InAlN, passivation, plasma treatment.**

I. Introduction

ONE INTRIGUING question in the GaN-based high-electron mobility transistor (HEMT) community is what prevents the device speed from reaching 300 GHz or higher. An important issue is to minimize the parasitic capacitance associated with the dielectric passivation of surface states in the access region, introduced for minimizing dc-to-RF dispersion and current collapse [1]. SiN passivation by chemical vapor deposition has been widely used for more than ten years [2], and typically, thick SiN (> 50 nm) is necessary to suppress the dispersion. However, the capacitive gate–source and gate–drain parasitics increase with the thickness as well as the dielectric constant of the passivation layer, thus limiting the GaN HEMT speed. To minimize parasitic capacitances, thin-layer passivation schemes have been sought. Higashiwaki *et al.* [3] deposited ultrathin SiN (2 nm) over AlGaN (4 and 6 nm) barrier HEMTs and reported a current gain cutoff frequency f_T of 190 GHz, Sun *et al.* [4] selectively removed SiN around the gate and reported InAlN-barrier HEMTs with an f_T of 205 GHz, and low-k materials [5] and thin Al_2O_3 [6] have also been explored. On the other hand, plasma treatment prior to dielectric passivation has been recognized to play an important role in device dispersion behavior and reliability [7], [8]. It was observed that AlGaN/GaN HEMTs treated with NH_3 plasma without subsequent SiN deposition displayed poor pulsed I–V characteristics but unchanged dc performance [7].

Lattice-matched InAlN/AlN/GaN heterostructures are one of the most promising alternatives to AlGaN/GaN HEMTs, aside from AlN/GaN HEMTs [9] and Al-rich AlGaN/GaN HEMTs [10], for high-speed applications due to their thin barriers and high 2DEG concentrations. Excellent dc and RF performance has been shown [4], [11], [12] as well as low leakage current in devices [13] and promise for mixed-signal circuit applications [14]. In this letter, we report an f_T of 210 GHz in depletion-mode InAlN/AlN/GaN HEMTs on a SiC substrate, achieved by applying a dielectric-free passivation (DFP) process, where the HEMT access region was treated with O_2/Ar plasma only. The effects of DFP on device dc and RF performance were studied. This DFP scheme introduces minimal parasitic capacitances, thus resulting in one of the highest reported f_T's in GaN HEMTs for devices with a 60-nm physical gate length and $\sim$11-nm barrier thickness without gate recess.

II. Experiments

The InAlN/AlN/GaN HEMT structure consists of a 9.8-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier, a 1.0-nm AlN spacer (total barrier thickness $t_{\rm bar} = 10.8$ nm), a 55-nm unintentionally doped GaN channel, and a 1.8-μm semi-insulating GaN buffer on a SiC substrate, grown by metal-organic chemical vapor deposition at Kopin Corporation.

The device fabrication started with mesa isolation using Cl_2-based reactive ion etching, followed by alloyed ohmic contacts using a Si/Ti/Al/Ni/Au stack annealed at 860 °C in N_2. The contact resistance extracted using the transmission line method is 0.38 $\Omega \cdot$ mm. Rectangular Ni/Au (40/90 nm) gates without gate recess were defined by electron-beam lithography and lift-off. Device processing concluded with the DFP treatment, consisting of O_2/Ar plasma at a bias of $\sim$20 V for 2 min. The device has a source–drain distance of 1.6 μm, a source–gate separation of 430 nm, a gate width of 2×50 μm, and a physical

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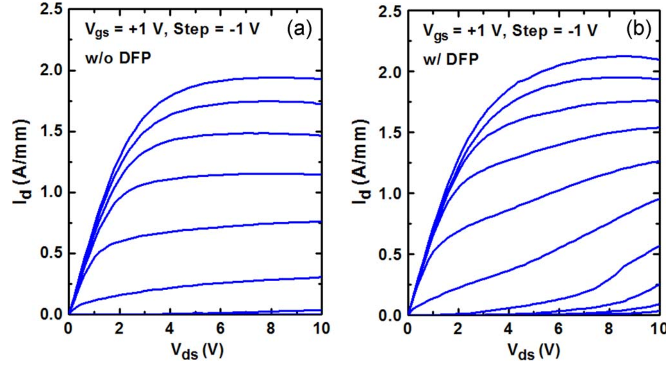

Fig. 1. Common-source family of I–V's (a) before and (b) after DFP on the device with $L_g = 60$ nm and $L_{\mathrm{sd}} = 1.6$ μm.

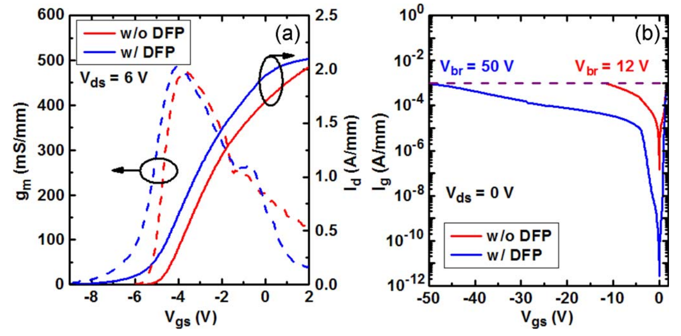

Fig. 2. (a) Measured transfer characteristics, showing a negative V_{th} shift of $\sim$0.8 V and $g_{m,\mathrm{peak}}$ increase at $V_{\mathrm{ds}} = 6$ V after DFP. (b) Gate diode I–V's showing leakage reduction after DFP.

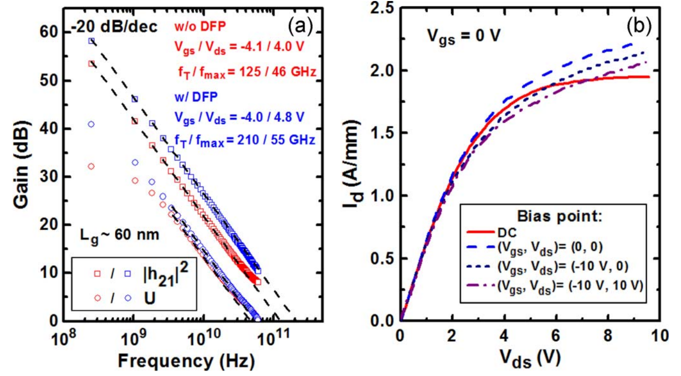

Fig. 3. (a) Current gain and unilateral gain of the device, showing $f_T/f_{\max} = 125/46$ and 210/55 GHz before and after DFP, respectively. (b) Pulsed I–V measurements after DFP, with a 300-ns pulsewidth and a 0.5-ms period.

gate length L_g of 60 nm, thus having a corresponding aspect ratio $L_g/t_{\mathrm{bar}} = 5.6$.

Device dc and RF measurements were taken with an Agilent 4142B source/monitor and an E8361C vector network analyzer from 250 MHz to 60 GHz. The calibration was carried out with LRM off-wafer impedance standards, and measured s-parameters were de-embedded by subtracting on-wafer open pad parasitics. The pulsed I–V measurement was performed using a Keithley 4225 pulse measurement unit.

III. Results and Discussion

Fig. 1 shows the common-source family of I–V's before and after DFP. The device has an on-resistance $R_{\mathrm{on}} = 1.3\ \Omega \cdot \mathrm{mm}$ extracted at $V_{\mathrm{gs}} = 1$ V. Prior to passivation, $I_{d,\max} = 2.0$ A/mm at $V_{\mathrm{gs}} = 1$ V, and a high output resistance was observed; after passivation, $I_{d,\max}$ increased to 2.1 A/mm, and a much more severe short-channel effect was observed. To understand the effects of DFP, room-temperature Hall effect measurements using a van der Pauw test structure were taken. Prior to DFP, the sheet resistance $R_{\mathrm{sh}} = 290\ \Omega/\mathrm{sq}$, with a 2DEG density $n_s = 1.6 \times 10^{13}\ \mathrm{cm}^{-2}$ and an electron mobility $\mu = 1330\ \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$, while after DFP, $R_{\mathrm{sh}} = 257\ \Omega/\mathrm{sq}$ (close to $260\ \Omega/\mathrm{sq}$ extracted from TLM linear fitting), n_s increased to $1.9 \times 10^{13}\ \mathrm{cm}^{-2}$, and $\mu = 1300\ \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$. This observation is consistent with previous studies of plasma treatments and dielectric passivation, in which they were found to reduce the surface barrier height of the nitrides, thereby increasing the 2DEG density in the channel [15], [16]. As a result of the surface passivation, depletion near the gate, also called gate-length extension [17], decreases. This, in turn, leads to a reduction of the electrical gate length, leading to more significant short-channel effects.

It is observed from the transfer curves (Fig. 2) that the peak extrinsic transconductance $g_{m,\mathrm{peak}}$ increased from 473 to 487 mS/mm after DFP, corresponding to intrinsic $g_{m,\mathrm{int}} = 618$ and 637 mS/mm for $R_s = 0.49\ \Omega \cdot \mathrm{mm}$; the gate leakage current was also reduced by more than 10$\times$ after DFP (not shown). The threshold voltage V_{th} at $V_{\mathrm{ds}} = 6$ V shifted from -4.7 to -5.5 V after DFP, obtained from the linear extrapolation of I_d, and the drain-induced barrier lowering measured over a drain-bias range of 0.1–6 V at $I_d = 10$ mA/mm increased from 110 to 530 mV/V; both facts suggest that the device experiences stronger short-channel effects after DFP. The gate diode I–V's before and after DFP of another HEMT with a comparable physical gate length fabricated on the same epiwafer following the same process flow are shown in Fig. 2(b). A reduction in gate diode leakage was observed in both reverse and forward bias directions after DFP, and the two-terminal gate diode breakdown voltage at $I_g = 1$ mA/mm increased from 12 to 50 V. It has been proposed that traps under and/or near the gate, most likely N vacancies, are responsible for current collapse and high gate leakage in GaN HEMTs [8]. This model is consistent with our observation: the leakage current via hopping and tunneling through traps located close to the gate metal is reduced by passivating these trap states since the region directly under the gate metal is not likely to be affected by DFP.

Fig. 3(a) shows the current gain and unilateral gain of the device as a function of frequency at the peak f_T bias conditions. Following a -20-dB/dec extrapolation, $f_T/f_{\max} = 125/46$ and 210/55 GHz are obtained before and after DFP, respectively, with an uncertainty of ± 5 GHz. The low $f_{\max}$ is due to the resistive rectangular gate. The L_g–f_T product of 12.6 GHz $\cdot$ μm is among the highest reported for GaN HEMTs with an aspect ratio L_g/t_{bar} of 5.6. Since, after DFP, $f_T > 140$ GHz is achieved for HEMTs on the same chip with $L_g < 115$ nm, an electrical gate length $L_{g,\mathrm{eff}} \geq 120$ nm can be estimated prior to DFP, associated with the measured f_T of 125 GHz. This indicates that the gate-length extension prior to DFP exceeds 60 nm, which is comparable to L_g. This large gate-length

extension reduction after DFP cannot be explained by the 2DEG density increase ($\sim$20%) alone, indicating that surface states are primarily responsible for the gate-length extension.

The DFP scheme employed in this letter clearly improves the RF performance of the HEMTs and reduces the gate-length extension, suggesting that the plasma treatment is passivating the surface states in the access region. However, historically, passivation also implies protection against degradation of devices due to operation in ambient conditions. To investigate the effectiveness of DFP under large-signal drive, pulsed I–V measurements were performed in air after DFP using a 300-ns pulse width and a 0.5-ms period. As shown in Fig. 3(b), the drain current density I_d at $V_{\rm gs} = 0$ V pulsed from $(V_{\rm gs}, V_{\rm ds}) = (0, 0)$ is higher than that at dc, indicating that the device suffers from self-heating under dc operation. Because of short-channel effects, current saturation is not observed in the cold pulsed I–V. I_d pulsed from (-10 V, 0) and (-10 V, 10 V) showed only modest gate lag (5.5%) and drain lag (3.7%), which are much smaller than the representative gate lag (16%) and drain lag (14%) on devices without DFP (not shown). However, further studies are necessary to fully investigate the suitability of DFP for large-signal amplification at high frequencies since a virtual gate of even a few nanometers can lead to appreciable changes in performance for decananometer-gate-length HEMTs. One possibility for enhancing environmental robustness is the use of a combination of DFP with low-k dielectric coating. It is also worth noting that the post-DFP performance of these HEMTs is unchanged over the course of the measurements reported here, which were taken over a period of several weeks.

Since effective passivation of GaN-based HEMTs with nanometer-length gates is still an open research problem, it appears possible that this DFP process may be a route to achieving $f_T > 300$ GHz. The demonstrated cutoff frequency f_T of 210 GHz is already among the highest reported values in GaN-based HEMTs [3], [4], [18], [19]. Given the robustness of the plasma treatment against large-signal device operation and unchanged device performance over weeks, it is possible that the O_2/Ar plasma treatment has created a thin oxide layer on the HEMT surface; additional investigation (e.g., X-ray photoelectron spectroscopy) is required to explore this possibility. Conventional approaches such as the use of back barriers and thinner top barriers are expected to ameliorate the short channel effects that have been revealed with DFP by reducing the gate-length extension.

IV. Conclusion

Lattice-matched depletion-mode InAlN/AlN/GaN HEMTs on a SiC substrate were fabricated and passivated with an O_2/Ar plasma treatment in the access region without subsequent dielectric deposition, i.e., DFP. This technique is shown to be effective for limiting gate-length extension by passivating surface states but without introducing extra parasitic capacitance, thus improving the transistor speed. The device with DFP and a 60-nm physical gate length shows one of the highest f_T values in GaN-based HEMTs, $f_T = 210$ GHz, as well as a high drain output current density of 2.1 A/mm. Future studies are necessary to better understand the physical mechanism of the DFP plasma treatment.

References

[1] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs—An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[2] B. Green, K. Chu, M. Chumbes, J. Smart, J. Shealy, and L. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.

[3] M. Higashiwaki, T. Mimura, and T. Matsui, "AlGaN/GaN heterostructure field-effect transistors on 4H-SiC substrates with current gain cutoff frequency of 190 GHz," *Appl. Phys. Express*, vol. 1, no. 2, p. 021103, Feb. 2008.

[4] H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J.-F. Carlin, M. Gonschorek, N. Grandjean, and C. R. Bolognesi, "205-GHz (Al, In)N/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 957–959, Sep. 2010.

[5] W.-K. Wang, C.-H. Lin, P.-C. Lin, C.-K. Lin, F.-H. Huang, Y.-J. Chan, G.-T. Chen, and J.-I. Chyi, "Low-k BCB passivation on AlGaN–GaN HEMT fabrication," *IEEE Electron Device Lett.*, vol. 25, no. 12, pp. 763–765, Dec. 2004.

[6] D. H. Kim, V. Kumar, G. Chen, A. M. Dabiran, A. M. Wowchak, A. Osinsky, and I. Adesida, "ALD Al_2O_3 passivated MBE-grown AlGaN/GaN HEMTs on 6H-SiC," *Electron. Lett.*, vol. 43, no. 2, pp. 129–130, Jan. 2007.

[7] A. P. Edwards, J. A. Mittereder, S. C. Binari, D. S. Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of AlGaN–GaN HEMTs using an NH_3 plasma treatment prior to SiN passivation," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 225–227, Apr. 2005.

[8] H. Hasegawa, T. Inagaki, S. Ootomo, and T. Hashizume, "Mechanisms of current collapse and gate leakage currents in AlGaN/GaN heterostructure field effect transistors," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 21, no. 4, pp. 1844–1855, Jul. 2003.

[9] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. Xing, "AlN/GaN insulated-gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 661–664, Jul. 2008.

[10] G. Li, T. Zimmermann, Y. Cao, C. Lian, X. Xing, R. Wang, P. Fay, H. Xing, and D. Jena, "Threshold voltage control in $Al_{0.72}Ga_{0.28}N$/AlN/GaN HEMTs by work-function engineering," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 954–956, Sep. 2010.

[11] R. Wang, P. Sanier, X. Xing, C. Lian, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Gate-recessed enhancement-mode InAlN/AlN/GaN HEMTs with 1.9 A/mm drain current density and 800 mS/mm transconductance," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1383–1385, Dec. 2010.

[12] A. Crespo, M. M. Bellot, K. D. Chabak, J. K. Gillespie, G. H. Jessen, V. Miller, M. Trejo, G. D. Via, D. E. Walker, Jr., B. W. Winningham, H. E. Smith, T. A. Cooper, X. Gao, and S. Guo, "High-power Ka-band performance of AlInN/GaN HEMT with 9.8-nm-thin barrier," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 2–4, Jan. 2010.

[13] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 309–311, Mar. 2011.

[14] Y. Tang, P. Saunier, R. Wang, A. Ketterson, X. Gao, S. Guo, G. Snider, D. Jena, H. G. Xing, and P. Fay, "High-performance monolithically-integrated E/D mode InAlN/AlN/GaN HEMTs for mixed-signal applications," in *IEDM Tech. Dig.*, 2010, pp. 30.4.1–30.4.4.

[15] T. Hashizume, S. Ootomo, S. Oyama, M. Konishi, and H. Hasegawa, "Chemistry and electrical properties of surfaces of GaN and GaN/AlGaN heterostructures," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 19, no. 4, pp. 1675–1681, Jul. 2001.

[16] N. Onojima, M. Higashiwaki, J. Suda, T. Kimoto, T. Mimura, and T. Matsui, "Reduction in potential barrier height of AlGaN/GaN heterostructures by SiN passivation," *J. Appl. Phys.*, vol. 101, no. 4, p. 043 703, Feb. 2007.

[17] Y.-R. Wu, M. Singh, and J. Singh, "Device scaling physics and channel velocities in AlGaN/GaN HFETs: Velocities and effective gate length," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 588–593, Apr. 2006.

[18] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. J. Willadsen, C. Butler, A. Schmitz, D. Wheeler, A. Fung, and M. Micovic, "220 GHz f_T and 400 GHz $f_{\max}$ in 40-nm GaN DH-HEMTs with re-grown ohmic," in *IEDM Tech. Dig.*, 2010, pp. 30.1.1–30.1.4.

[19] J. W. Chung, T.-W. Kim, and T. Palacios, "Advanced gate technologies for state-of-the-art f_T in AlGaN/GaN HEMTs," in *IEDM Tech. Dig.*, 2010, pp. 30.2.1–30.2.4.