A 1.1nW Energy Harvesting System with 544pW Quiescent Power for Next Generation Implants

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Abstract

This paper presents a nW power management unit (PMU) for an autonomous wireless sensor that sustains itself by harvesting energy from the endocochlear potential (EP), the 70–100 mV electrochemical bio-potential inside the mammalian ear. Due to the anatomical constraints inside the inner ear, the total extractable power from the EP is limited to 1.1–6.25 nW. A nW boost converter is used to increase the input voltage (30–55 mV) to a higher voltage (0.8 to 1.1 V) usable by CMOS circuits in the sensor. A pW Charge Pump circuit is used to minimize the leakage in the boost converter. Further, ultra-low-power control circuits consisting of digital implementations of input impedance adjustment circuits and Zero Current Switching circuits along with Timer and Reference circuits keep the quiescent power of the PMU down to 544 pW. The designed boost converter achieves a peak power conversion efficiency of 56%. The PMU can sustain itself and a duty-cyled ultra-low power load while extracting power from the EP of a live guinea pig. The PMU circuits have been implemented on a 0.18μm CMOS process.

I. Introduction

Biomedical implantable electronic systems like pace-makers and cochlear implants are being used extensively today and devices like retinal implants and intracranial pressure sensors are also being developed [1]. Moreover, a wide range of implants are now being envisioned for sensing, *in-vivo* drug delivery and other applications [2], [4]. Typically, these implants are powered by batteries that either need to be replaced periodically or need to be

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charged by wireless means [3]. However, stringent restrictions on the battery electrolytes' containments and on tissue heating [3] making achieving energy autonomy extremely challenging in such implantable systems.

Traditional energy harvesters like photo-voltaic cells, thermoelectric generators and piezoelectric harvesters as described in [5] are not ideal for implantable electronics since these energy sources require conditions that typically do not exist inside a mammalian body. The endocochlear potential (EP) is a 70 to 100mV dc bio-potential [6], [7] that exists inside the mammalian cochlea. It has been demonstrated that by utilizing the EP as the sole energy source, it is possible to power an ultra-low-power implant inside the inner ear that can be used for sensing and in-vivo drug delivery [8]. Due to anatomical constraints inside the inner ear, the total extractable power from the EP is limited to 1.1–6.25 nW. While the work presented in [8] focuses on the biological aspects of the proposed concept and the high-level sensor definition, this paper focuses on the circuit details of the nW power management unit (PMU) [9] that enabled the proposed sensor and powered an ultra-low power, duty-cycled RF transmitter [10] in the sensor.

In order to operate the PMU at nW levels, there are some key circuit design challenges that need to be addressed. First, the PMU needs to be as efficient as possible while processing ultra-low-power. Second, the PMU control circuits need to be always active making it necessary to reduce the quiescent current in these circuits to ensure system sustainability. Third, we need to ensure close to maximum available power is extracted from the energy source at all times. Although the PMU is designed assuming EP to be the energy source in this work, all the circuit techniques that will be presented here can be easily extended to all low power energy harvesting systems. This paper is organized a follows. Section II of this paper highlights the PMU architecture. Section III focuses on the nW boost converter operation, design and optimization. Section IV highlights the pW Charge Pump circuit used to minimize the leakage power in the boost converter. Section V presents the pW Control, Timer and Reference circuits that enabled the sensor operation. Section VI highlights the simulated performance of the PMU under process variations. Section VII focuses on the PMU measured results.

II. PMU Architecture

The PMU, shown in Figure 1, consists of a nW boost converter, pW Control circuits (Φ_1 and Φ_2 Generation circuits), a Charge Pump along with Timer and Reference circuits. Two electrodes connected to the PMU are inserted into the inner ear to tap the EP. Due to the anatomical constraints in the inner ear, these electrodes need to have tip diameters close to 2 μm [8] causing the resistance of each electrode to be around 200–600 kΩ. The energy source can therefore be modelled by a voltage source V_{EP} and a series resistor, R_{elec} which is the sum of the two electrode resistances [8]. With an overall electrode impedance of 400 kΩ to 1.2 MΩ and V_{EP} of 70–100 mV, the maximum extracted power from the EP ($V_{EP}^2/4.R_{elec}$), is close to 1.1–6.25 nW. This is much lower that the power budget of previously published PMUs [11]–[13]. Further, the input voltage for the boost converter is half the EP (about 30–55 mV) when maximum power is extracted.

This implies that we need an efficient boost converter that operates with input voltages from 30–55 mV and can boost it up to 0.8–1.1 V, voltages more usable by CMOS circuits, at nW power levels. The high voltage conversion ratio along with the nW power budget make achieving high efficiencies extremely challenging. The boost converter in this work has been designed to meet the aforementioned requirements. A Charge Pump has been employed to reduce leakage in the boost converter. To ensure system sustainability, the quiescent power of all Control, Timer and Reference circuits has been kept in the 10–100's of pW range.

III. Ultra-Low Power Boost Converter Design and Optimization

A. Ultra-Low Power Boost Converter Operation

Due to the ultra-low power budget, the boost converter used in the PMU operates in the discontinuous conduction mode (DCM). While extracting maximum power, the input voltage is typically close to half of the EP, as shown in Figure 2(a). Therefore, the converter is required to boost up an input voltage (V_{IN}) of 30–55 mV up to 0.8–1.1 V (V_{DD}) which is used to power the Control and Timer circuits, a Charge Pump and a duty cycled load (RF-Tx in this work). The RF-Tx load is periodically enabled (once every 40–360 seconds as shown in Figure 2(a)) causing the boost converter output voltage (V_{DD}) to droop instantaneously. The V_{DD} starts to rise up once the RF-Tx load is disabled. This ensures that the converter is able to accumulate enough energy from the EP to be able to turn on the RF-Tx load for a short burst. The cycle by cycle operation of the boost converter has been shown in Figure 2(b). During the Φ_1 phase, the NMOS power FET (*N0* in Figure 1) is on and the current through the inductor L ramps up storing energy in the inductor. After a fixed time t_1 (say 2.5μs, justified later in Section V), *N0* is turned off and the PMOS power FET (*P0* in Figure 1) is turned on for time t_2 causing the energy stored in the inductor to be transferred to the system power supply capacitor, C_{DD}. Since the converter operates in DCM, after the Φ_2 phase, the converter stays idle until the Φ_1 phase of the next switching cycle. This idle phase (T_{period}-t_1-t_2) is much longer than phases Φ_1 and Φ_2 primarily due to the low input current to the converter.

In traditional energy harvesting systems [14], [15], there are usually two power converters in series between the energy source and the load circuits. The first power converter regulates the input voltage (or adjusts the input impedance for maximum power transfer) storing the harvested energy on to an energy buffer (supercapacitor or battery) and the second converter regulates the output voltage to the load circuits. However, due to the stringent power budget in this PMU, a single boost converter has been used. The converter has an input impedance close to the electrode impedance in order to ensure close to maximum power is transferred from the EP. The output of the converter is unregulated and settles to a level where the sum of the losses in the boost converter, power dissipated in the control and load circuits equals the power harvested by the boost converter (0.8–1.1V in this implementation). For a variety of sensing applications, the load, usually RF-Tx circuits, can be aggressively power gated and duty cycled. These circuits need to make infrequent RF transmissions and then can be idle for long periods in time. Therefore, depending on the input power to the PMU, the frequency of triggering the RF load can be varied to coarsely adjust the output voltage. If the input power is high, the duty cycled load can be trigger more frequently and vice-versa. In

this implementation, the frequency of triggering the load is adjusted by externally configuring 2 bits as the electrode impedance is known before implantation (explained later in more detail in Section V).

Previous work [16] has shown that for boost converters in DCM, operating with high voltage conversion ratio, the input impedance (ratio of input voltage to average input current) is approximately given by Eq. 1, where t_1 is the *N0* on time, f_s is the switching frequency and *L* is the converter's inductor. In this work therefore, *N0* on time, switching frequency and the boost converter inductance have been selected such that the input impedance of the boost converter is close to the sum of the electrode resistances. This will be discussed in more detail later.

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \approx \frac{2 \cdot L}{t_1^2 \cdot f_s} \quad (1)$$

B. Ultra-Low Power Boost Converter Design Considerations

Traditionally, majority of the losses in the boost converter arise from conduction loss in *N0*, *P0* and the inductor and switching loss due the gate capacitances of *N0*, *P0* and the overall switch node capacitance (C_{EFF}) as shown in Figure 3(a). However, for nW operation there are some additional design considerations before we optimize the converter for efficiency.

1) Leakage Loss in Boost Converter—While handling ultra-low power levels, the losses arising from the sub-threshold leakage currents through *N0* and *P0* (Figure 3(b)) can become comparable to the conduction and switching losses due to the power FETs in the boost converter. In order to reduce the losses due to leakage currents, lets first see the leakage paths involved. During the converter's idle phase in DCM, both *N0* and *P0* are off as shown in Figure 3(b) and the V_{DRAIN} node voltage settles to V_{IN}. Moreover, for the converter in this work, due to the low input current, the idle time is much longer than the Φ_1 and Φ_2 durations as shown before in Figure 2(b). For typical boost converters with high voltage conversion ratios, there are two leakage paths, one from the input and the other from the output as shown in Figure 3(b). If we compute the power loss due these leakage paths, we can see that the loss due to the output leakage path tends to be much higher than the loss due to input leakage- 12.5 times higher in this implementation. This is mainly due to the fact that the output voltage, V_{DD}, is much higher than the input voltage, V_{IN}, for the boost converter. Further, this leakage current is governed by the sub-threshold leakage through *P0*. In this work, an auxiliary converter (Charge Pump) has been implemented to reduce the leakage in *P0* which reduces the power loss due to the output leakage path in the boost converter. In order to do so, a gate signal with a supply voltage higher than V_{DD} is used as shown in Figure 4. When off, *P0* sees a negative source to gate voltage (V_{SG}) which helps reduces sub-threshold leakage current in the transistor [17] by biasing it to the super cut-off region. The Charge Pump is used to generate the higher supply voltage (V_{PUMP}). This leakage reduction of course comes at a small cost of generating the V_{PUMP} supply. This will be discussed in detail later in Section IV.

2) Switching Loss due to Switch Node Parasitic Capacitor—In traditional power converters, $C_{PAR,EFF}$, the total parasitic capacitance at the switching node (sum of the PCB parasitic capaciatace, inductor parasitic capacitance, ESD and bond pad capacitance) is usually smaller than the power FET intrinsic capacitances. However, due to the low current levels in this converter, the power transistors $N0$ and $P0$ are sized such that $C_{PAR,EFF}$ becomes more than the intrinsic FET capacitances. Following the Φ_2 phase of the boost converter, the common drain terminal of $N0$ and $P0$ rings due to the resonant circuit formed by L, $C_{PAR,EFF}$ and C_{IN} as shown in Figure 2(b). During this ringing, the stored energy in $C_{PAR,EFF}$ is partly dissipated in the body diode of $N0$ (V_{DRAIN} rings and goes a diode voltage below ground turning on the $N0$ body diode) and in the inductor during the idle time of the boost converter. To get a quantitative idea, let's consider a typical value of 5pF for $C_{PAR,EFF}$. At a typical switching frequency of 1kHz and 1V V_{DD}, this would cause 2.5nW loss which is more than the system power budget's lower limit by 2.27 times and is 40% of the system power budget's upper limit. Further, it must be noted that depending on the board layout and the type of inductor, it might be difficult to control this parasitic capacitance. Therefore, the switching frequency of the converter needs to be appropriately selected.

Therefore, keeping the leakage currents in the power train and the parasitic capacitances in mind, the boost converter has been optimized. These two key aspects along with the input impedance requirement make converter's efficiency optimization different from previously published low power switching converters [12], [15].

C. Loss Optimization

Eq. 2 gives the approximate expression for the sum of the different losses in the boost converter- gate drive losses (due to $N0$ and $P0$ with the Miller Effect), FET conduction losses, conduction loss due to inductor ESR, FET leakage losses. Here, $C_{GS,N0}$, $C_{GD,N0}$, $C_{GS,P0}$ and $C_{GD,P0}$ are the gate to drain and gate to source capacitances per unit width for $N0$ and $P0$, W_N and W_P are the corresponding transistor widths, η is the efficiency of the charge pump, I_p is the peak inductor current, $R_{N,0}$ and $R_{P,0}$ are the resistance per unit width for $N0$ and $P0$, $I_{LEAK0,N}$ and $I_{LEAK0,P}$ are the leakage currents per unit width of $N0$ and $P0$, $R_{L,ESR}$ is the effective series resistance of the inductor and $I_{LEAK0,NGDRV}$ and $I_{LEAK0,PGDRV}$ are the leakage currents in the $N0$ and $P0$ gate drivers per unit width of $N0$ and $P0$. The FET drain to source capacitances along with $C_{PAR,EFF}$ can be all absorbed into C_{EFF}. It must be noted that the loss due to the Miller effected capacitance appears only for $N0$ since the switch node (V_{DRAIN}) gets charged up to V_{DD} by the inductor current if there is adequate dead-time between turning off $N0$ and turning on $P0$. Moreover, the miller capacitance due to $N0$ gets multiplied by the $\Delta V_{DRAIN}/\Delta V_{GATE}$ of $N0$ which is V_{IN}/V_{DD}.

$$Total\ Loss \approx \left[C_{GS,N0} + C_{GD,N0} \cdot \left(1 + \frac{V_{IN}}{V_{DD}}\right) \right] \cdot W_N \cdot V_{DD}^2 \cdot f_s$$

$$+ \frac{1}{\eta} \cdot \left[C_{GS,P0} + C_{GD,P0} \right] \cdot W_P \cdot V_{PUMP}^2 \cdot f_s$$

$$+ V_{DD} \cdot I_{LEAK0,NGDRV} \cdot W_N + \frac{1}{\eta} \cdot V_{PUMP} \cdot I_{LEAK0,PGDRV} \cdot W_P$$

$$+ \frac{I_p^2}{3} \cdot t_1 \cdot f_s \cdot \frac{R_{N,0}}{W_N} + \frac{I_p^2}{3} \cdot t_2 \cdot f_s \cdot \frac{R_{P,0}}{W_P} \qquad (2)$$

$$+ V_{IN} \cdot I_{LEAK0,N} \cdot W_N + (V_{DD} - V_{IN}) \cdot I_{LEAK0,P} \cdot W_P$$

$$+ \frac{1}{2} \cdot C_{EFF} \cdot V_{DD}^2 \cdot f_s + \frac{I_p^2}{3} \cdot (t_1 + t_2) \cdot f_s \cdot R_{L,ESR}$$

Further, since a boost converter with high voltage conversion ratios is being optimized, on approximating the inductor's volt-second rule, we can relate V_{IN} and V_{DD} by $V_{IN} \cdot t_1 \approx V_{DD}$ · t_2. We also know that $t_1 \gg t_2$ and $I_p = \frac{V_{IN} \cdot t_1}{L}$. By imposing the impedance condition given by Eq. 1, along with Eq. 2, we can simplify the conduction loss terms (for *N0*, *P0* and inductor *ESR*) and make the approximation the V_{DD} is much greater than V_{IN} for the boost converter in this work to give us Eq. 3.

$$Total\ Loss \approx \left[C_{GS,N0} + C_{GD,N0} \cdot \left(1 + \frac{V_{IN}}{V_{DD}}\right) \right] \cdot W_N \cdot V_{DD}^2 \cdot f_s +$$

$$\frac{1}{\eta} \cdot \left[C_{GS,P0} + C_{GD,P0} \right] \cdot W_P \cdot V_{PUMP}^2 \cdot f_s$$

$$+ V_{DD} \cdot I_{LEAK0,NGDRV} \cdot W_N + \frac{1}{\eta} \cdot V_{PUMP} \cdot I_{LEAK0,PGDRV} \cdot W_P$$

$$+ \frac{2^{3/2}}{3} \cdot \frac{V_{IN}^2}{L^{1/2}} \cdot \frac{1}{Z_{IN}^{3/2}} \cdot \frac{1}{f_s^{1/2}} \cdot \left[\frac{R_{N,0}}{W_N} + \frac{R_{P,0}}{W_P} \cdot \frac{V_{IN}}{V_{DD}} + R_{L,ESR} \right] \qquad (3)$$

$$+ V_{IN} \cdot I_{LEAK0,N} \cdot W_n + V_{DD} \cdot I_{LEAK0,P} \cdot W_P +$$

$$\frac{1}{2} \cdot C_{EFF} \cdot V_{DD}^2 \cdot f_s$$

Since the converter needs to be optimized for given Z_{IN}, V_{IN}, V_{DD} and *L*, optimal values of f_s, W_N and W_P can be obtained from Eq. 3. The FETs need to be sized optimally in all power converters and the switching frequency is typically selected based on the size and efficiency requirement. However, in energy harvesting systems like the one presented, there is an additional constraint coming from the input impedance which is frequency dependent as shown in Eq. 1. The loss optimization in this paper takes this input impedance requirement into account and shows that in boost converters for energy harvesting systems like the one presented, there exists an optimal switching frequency as shown in Figure 5(a). For frequencies higher than this optimal, the switching losses dominate and for frequencies lower than this optimal, the *N0* conduction time (t_1) increases for maintaining the same input impedance causing the rms currents in the converter to increase. For this optimization, it has been assumed that V_{IN} is 40mV, V_{DD} is 1V and *L* is 47μH. It can be observed from Eq. 3, a

higher boost converter inductance gives lower losses for a fixed input impedance due to the fact that higher inductance translates to lower rms currents. Therefore, there is a trade-off between efficiency and form-factor. A 47μH 4.8mm × 4.8mm × 1.8mm inductor was found to be satisfy the system form-factor requirement [8] which is why this has been assumed in the analysis. Figure 5(b) shows the corresponding $N0$ width optimization. The $P0$ width optimization has been considered after taking into account the overhead associated with the Charge Pump. This has been described in detail in Section IV later. Further, $I_{LEAK0,N}$, $I_{LEAK0,P}$, $C_{PAR,EFF}$ (10pF) and Z_{IN} (1.6MΩ) have been intentionally over-estimated to account for variability or any additional parasitic capacitance that may affect the efficiency of the actual implementation. The leakage current over-estimation leads to smaller device widths (W_N and W_P). The corresponding efficiency overhead is estimated to be less than 1% in this implementation. This design margin has been intentionally kept due to the ultra-low power nature of the design and its sensitivity to leakage.

IV. Charge Pump for Boost Converter Leakage Reduction

A. Charge Pump Operation and Loss Analysis

As discussed before in Subsection III-B, a Charge Pump circuit (implemented as a Voltage Doubler) [24] is used to create an auxiliary power supply, V_{PUMP} (≅1.5V), to mainly power the gate driver circuit for the boost converter power FET $P0$. This results in a negative V_{SG} for $P0$ when the device is off thereby, reducing the sub-threshold leakage from the output in the boost converter as shown in Figure 4. Further, the Charge Pump is also used to power the footer transistors that have been used to reduce the leakage in the duty cycled load shown in Figure 1. As the footer transistors has been implemented by thick oxide, higher V_T devices, the V_{PUMP} supply ensures the footer transistor has enough overdrive to turn on when the load is enabled. The higher Ion/Ioff ratio of the thick oxide device helps significantly reduce the leakage in the load [10].

Figure 6 shows the implementation of the Charge Pump circuit. The Charge Pump has been designed to deliver 30 to 40pW to the $P0$ gate driver circuit. The circuit is switched at the same clock frequency that is used by the boost converter. The circuit utilizes MiM capacitors for C_{PUMP} capacitors. A total of 34.8pF is used as the charge transfer capacitors ($2×C_{PUMP}$). A 350pF output decoupling capacitor for the V_{PUMP} supply is also integrated with the Charge Pump. In order to operate efficiently, the power FETs $N1$ and $N2$ in Figure 6 use deep n-wells to avoid any threshold voltage increase due to body effect. The gate driving of $P1$, $P2$, $N1$ and $N2$ is implicitly done by the cross coupled inverter structure.

It must be noted that while optimizing the power conversion efficiency of the Charge Pump, the sub-threshold leakage currents in the Charge Pump need to be taken into account. Figure 7 shows the current paths through C_{PUMP} and the leakage current in the Charge Pump during the two clock phases, direction of switching currents (I_{SW1} and I_{SW2}) has been shown in blue and the leakage currents (I_{LEAK1} through I_{LEAK4}) in red. The currents charging up the gate capacitances of $P1$, $P2$, $N1$ and $N2$ have not been shown for simplicity. The total output current from the V_{PUMP} supply is given by Eq. 4 and the total input current from V_{DD} is given by Eq. 5 where α is the ratio of bottom plate parasitic capacitance to the actual

capacitance and C_{Tran} is the total switching effective gate capacitance due to the *P1*, *P2*, *N1* and *N2*.

$$I_{OUT,doubler} \approx 2C_{PUMP}[2V_{DD}-V_{PUMP}]f_s - C_{Tran}[V_{PUMP}-V_{DD}]f_s - I_{LEAK1} - I_{LEAK2} \quad (4)$$

$$I_{IN,doubler} \approx 4C_{PUMP}[2V_{DD}-V_{PUMP}]f_s + 2\alpha C_{PUMP}V_{DD}f_s - C_{Tran}[V_{PUMP}-V_{DD}]f_s - I_{LEAK1} - I_{LEAK2} + I_{LEAK3} + I_{LEAK4} \quad (5)$$

Therefore, the efficiency of the converter can be expressed as in Eq. 6 with terms k_1 and k_2 which have been defined in Eq. 7 and Eq. 8 respectively.

$$\eta_{doubler} \approx \frac{[1-k_1]}{[2+k_2]} \cdot \frac{V_{PUMP}}{V_{DD}} \quad (6)$$

$$k_1 = \frac{C_{Tran}[V_{PUMP}-V_{DD}]f_s + I_{LEAK1} + I_{LEAK2}}{2C_{PUMP}(2V_{DD}-V_{PUMP})f_s} \quad (7)$$

$$k_2 = \frac{2\alpha C_{PUMP}V_{DD}f_s - C_{Tran}[V_{PUMP}-V_{DD}]f_s + I_{LEAK3} + I_{LEAK4} - I_{LEAK1} - I_{LEAK2}}{2C_{PUMP}(2V_{DD}-V_{PUMP})f_s} \quad (8)$$

Eq. 6 is similar to the efficiency expression for the conventional *1:2* voltage conversion charge pump except for the fact that terms account for leakage losses. The power conversion efficiency has been optimized to around 77% in this implementation. Since the converter switches at 12.8Hz, it operates well within its slow-switching limit [25]. Therefore, the devices have been sized essentially to minimize leakage while providing the required speed by following the methodology in [26]. Due to the ultra-low power requirement, the C_{PUMP} capacitors has been intentionally over-sized to account variations in leakage current through the doubler circuit transistors or in the *P0* gate drive circuit which is the load circuit for the doubler. Higher C_{PUMP} would enable us to suppress the variations in leakage in the Charge Pump (Eq. 7 and Eq. 8) and would also help in supplying more current to the *P0* gate drive circuit (Eq. 4). Over-sizing C_{PUMP} results in about 4pW of extra switching loss.

B. Leakage Reduction, Net Power Savings and P0 sizing

For this implementation, because of the Charge Pump, the leakage power due to sub-threshold leakage in *P0* is reduced from 224 pW (simulated without Charge Pump) to as low as 0.75 pW (simulated with Charge Pump) at the typical corner. This comes at the cost of increased switching loss and leakage in the *P0* gate drive circuit due to higher supply voltage. This overhead is estimated to be 30–40 pW. On factoring in the efficiency of the Charge Pump, this overhead becomes 39 to 52 pW. Without the Charge Pump, the gate drive circuit would have consumed 4 pW. Therefore, an overall benefit of 175 to 188 pW (simulated) is obtained. Although may seem a small amount, this power reduction is close to 17% of the minimum system power budget. Moreover, in the fast corner, a benefit of about 950pW is obtained indicating that the Charge Pump enables the PMU operation for all process corners. One may consider reducing the leakage in the boost converter *P0* power

FET by simply reducing its width. In this case, the FET size needs to be done by minimizing the sum of conduction, switching and leakage losses as shown by the red plot in Figure 8. However, from the optimization analysis done before in Section III-C, it is observed that after accouting for the overhead associated with the Charge Pump, this technique results in a lower minimum loss (124.7 pW lower, which is 12.4% of the input power in this analysis). Figure 8 also shows that this technique enables us to use wider *P0* device with lower conduction losses and lower leakage. Therefore, the Charge Pump becomes essential for ensuring ultra-low power operation of the PMU.

V. Control, Timer, Reference and Startup Circuits

In order for the PMU to sustain itself, all the control circuits and drivers have been designed to consume less than the energy harvested by the boost converter. The control circuits consists of circuits ensuring maximum power extraction (shown as Φ_1 Generation in Figure 1), ZCS control for DCM (shown as Φ_2 Generation in Figure 1) and Timer with references.

A. Φ_1 Pulse Generation

The boost converter is configured to present an input impedance (Eq. 1) close to the electrode impedance to ensure maximum power extraction. A tunable pulse generator (shown in Figure 9) is used to create the t_1 pulse with the desired width required during the Φ_1 phase of the boost converter. The pulse generator has been designed for widths ranging from 0.25μs to about 4μs with 5 external tuning bits. Since the electrode impedance is known before hand, the input impedance can be set appropriately before implanting the sensor. The wide t_1 range provides the ability to trim t_1 prior to implantation. This enables us to not only account for variability in process and electrode impedances but also to support different boost converter inductances (Eq. 1). Since the system is meant to implanted, the temperature of the operating environment is well regulated so the variations in pulse widths due to temperature can be ignored. In order to minimize variations in pulse widths due to voltage variations, the transistors used in the logic gates of the pulse generator blocks are 2V transistors that operate above threshold for V_{DD} of 0.8–1.1V. The majority of the delay is generated due to the adjustable resistor and the capacitor C_{DELAY} shown in Figure 9. This makes the pulse widths and hence the converter's input impedance less sensitive to V_{DD}. Moreover, small variations in converter's input impedance caused by variations in supply during the sensor's operation can be tolerated if the power transfer inefficiency due to mismatch between the electrode (source) impedances and the (load) converter's input impedance is small. For this design, with a worst case V_{DD} variation of 0.8–1.1V over the course of sensor's operation translates to a power transfer inefficiency of about 3% (effective power transfer efficiency of 97%). In principle, a MPPT loop would help remove this inefficiency however even practical ultra-low power MPPT implementations reported have similar tracking efficiency (96% in reference [16]).

B. Φ_2 Pulse Generation

Since the boost converter operates in DCM with synchronous rectification, it is necessary to ensure that *P0* turns off when the inductor current is close to zero. A Zero Current Switching (ZCS) scheme similar to [15], [16], [18], [19] has been implemented. Figure 9 shows the

details of the circuits performing ZCS. The width of t_2 is required to be smaller than t_1 for the boost converter implemented. This pulse generator creates pulse widths varying from 9ns to 96ns to account for variability and wide range of t_1 values. A feedback loop is implemented to adjust the t_2 pulse width appropriately. Since the pulses created by the pulse generator blocks are discrete in nature, in the steady state, the t_2 pulse width toggles between two pulse width settings-one where the t_2 pulse width is slightly less than the ideal value and the other where the t_2 pulse width is slightly greater than the ideal value [15], [16]. By using a clocked comparator (StrongARM register [20]) that compares the V_{DRAIN} voltage with V_{DD} after $P0$ is turned off, the feedback loop detects if the t_2 is greater than or smaller than the ideal value. The comparator output is used by an Increment/Decrement Logic block that either increases or decreases the t_2 width depending on the comparator decision. The logic gates have been implemented in the Increment/Decrement block are not required to be very fast due to the low switching frequency of the converter. Therefore, they have been implemented with high V_T transistors, operating in sub-threshold with long gate lengths to minimize leakage currents.

C. Timer and Reference Circuits

A pW Relaxation Oscillator similar to [21] and a clock divider have been implemented as Timer circuits (Figure 10(b)). The oscillator is designed to generate a 12.8 Hz clock (Sys_Clk), with frequency close to the optimal f_s for the boost converter. The clock divider creates a lower frequency clock (Sys_Clk_Div) from Sys_Clk which is used to enable the RF-Tx once in 40 to 360 seconds. Two analog comparators, $Comp_1$ and $Comp_2$ (differential amplifier stage followed by common source stage), are used to compare the voltage across C_{OSC} with two reference voltages, V_{REF1} and V_{REF2}. References V_{REF1} and V_{REF2} are set to $2V_{DD}$=3 and V_{DD}/3 respectively by a voltage divider formed by cascading twelve PMOS transistors biased in the sub-threshold regime (Figure 10(a)). Currents I_{CHG1}, I_{CHG2} and the analog comparator bias currents are mirrored from the a supply independent current reference [22], [23] with 60pA reference current.

D. Low Voltage Startup

Some previously published works have demonstrated low voltage startup using MEMs switches [15], silicon post processing [27], transformers with normally on transistors [28], startup ring oscillators [12]. Most of these techniques have special requirements from the technology used [15], [27], [28] or are limited to startup voltages in 100's of mV [12]. In this work, it is envisioned that the sensor can be started up by wireless means after it has been implanted. An external transmitter is used to transfer an initial burst of energy to the sensor. The same antenna used by the RF-Tx in the sensor is utilized to receive this energy burst. The ESD diodes rectify the AC voltage and charging the power supply V_{DD} [8], [10]. This initial charge up (V_{DD} getting charged to 0.9V observed to be sufficient) starts up the pW Relaxation Oscillator in the system. Since the oscillator clock directly goes to the boost converter Φ_1 and Φ_2 Generation Circuits and the Charge Pump, both the boost converter and the Charge Pump start up. Moreover, the bits for Φ_1 pulse width are set before implantation so the Φ_1 generation circuit (Figure 9) starts up from a known state. For the Φ_2 generation circuit, there are 3 registers that hold the pulse width information (Figure 9). In case these registers start up in the wrong state, since there is a ZCS feedback loop, in the worst case

this would take 9 cycles to correct itself. In this implementation this was found to not effect the system performance.

VI. System Simulation with Process Variations

The PMU has been designed taking into account process variations. Figure 11 shows the loss distribution in the PMU for slow-slow, nominal and fast-fast corners. Since the boost converter output voltage is unregulated (although it can be coarsely controlled by changing how frequently the load is triggerred), the output voltage settles to the value where the sum of the power converter's losses, control and load circuitry power dissipation becomes equal to the power being harvested by the boost converter. For the slow-slow and the nominal corners, the input power to the PMU is 1nW and the outputs settle to 1V and 0.97V respectively. However, it is observed that 1nW is not sufficient for the system to sustain itself in the fast-fast corner due to increased leakage. For the fast-fast corner simulation, the input power to the boost converter is 1.09nW and the output settles to 0.78V. We can also observe that the load power is significantly lowered at this corner due to lower frequency of triggerring the RF load.

VII. Experimental Results

The PMU circuits have been implemented in a 0.18μm CMOS process. Figure 12 shows the die micro-photograph with the PMU details. Most of the active area is occupied by the current reference resistor (470MΩ for low quiescent current requirements, implemented as a high resistivity poly resistor) and the decoupling capacitor for the V_{PUMP} supply (350pF). The large decoupling capacitor is to minimize the droop in the V_{PUMP} supply during a RF-Tx transmission as the V_{PUMP} supply does not use any off-chip capacitors. Figure 13 shows the implantable sensor board. The board is designed to fit into the human mastoid cavity [8]. The only off-chip components are the boost converter inductor L (47μH, 4.8mm × 4.8mm × 1.8mm), system supply capacitor C_{DD} (200nF), input capacitor C_{IN} (1μF) and an antenna (3mm × 4.3mm) for the RF-Tx.

A. Boost Converter Power Stage Output Power and Efficiency

Figure 14 shows the boost converter power stage performance for an electrode impedance of 1M (emulated by a 1MΩ resistor for this measurement) for two different values of the EP (80mV and 100mV, emulated using a voltage source for this measurement as shown in Figure 14(c)) with a V_{DD} of 0.9V and boost converter inductance of 47μH. The input voltage to the boost converter is varied by changing the input impedance of the boost converter (by varying the Φ_1 pulse width) as shown in 14(c). In order to characterize the boost converter power stage output power and efficiency, power has been supplied to all the control circuits using an external power supply (P_{CTRL}) here. The converter's power stage efficiency is measured by taking the ratio of $P_{BC,OUT}$ to $P_{BC,IN}$. It can be observed from Figure 14(a), maximum power is extracted by the boost converter power stage for voltages close to half of the EP. This is when the converter's input impedance equals the electrode impedance. For the boost converter power stage efficiency in Figure 14(b), it is observed that the efficiency tends to be higher for higher input voltages. This is due to smaller inductor peak currents and therefore, smaller conduction losses. However, for input voltages higher than a certain

level, the efficiency reduces due to lower input power to the boost converter power stage as the converter's input impedance does not match the source (emulated electrode) impedance. Figure 15(a) shows the output power from the boost converter power stage for EP of 80mV, electrode impedance of 750kΩ, V_{DD} of 0.9V for different values of boost converter inductor. Figure 15(b) shows the corresponding efficiency plot. It can be observed that the efficiency and output power is lower for lower inductance for the same input impedance is due to higher rms currents.

B. Power Consumption of Individual Blocks

The quiescent power consumption of the individual blocks has been measured. For an input power of close to 1.2nW (with emulated EP of 80mV and electrode resistance of 1.28MΩ which is the maximum electrode impedance that the system can handle), the boost converter efficiency is observed to be around 53% with V_{DD} around 0.9V. This translates to a total output power of 637pW from the boost converter. Figure 16 shows the power breakup of the individual circuits utilizing this power. Overall, 544pW is consumed in the converter's control circuits (Boost converter Impedance adjustment block, ZCS circuits, Timer, Reference and Charge Pump). Therefore, the PMU (without the RF-TX load) can sustain itself with close to 1.1nW input power. Careful design of the boost converter with the supporting control and auxiliary circuits ensure that the output power from the converter is not only enough to sustain the converter but can also be used to power duty cycled load circuits like a RF-Tx or other potential loads.

C. Supply Voltage Measurements during Surgical Experiments

Measurements have been made with the PMU connected to electrodes tapping the EP of a anesthetized guinea pig and supplying power to aultra-low-power duty cycled RF-TX [10]. Figure 17(a) shows the V_{DD} measurements made during three separate surgical experiments for EP values of 80–100mV and electrode impedances in the range of 400kΩ to 1MΩ. Figure 17(b) shows the corresponding V_{PUMP} measurements. The supply voltages droop when the duty cycled RF-Tx is enabled. For the measurements made, the RF-Tx is enabled either once in 40 to 80 seconds as can be seen in Figure 17.

D. Comparison with State-of-Art Ultra-Low Power DC-DC Converters

Figure 18 compares this work with State-of-Art ultra-low power converters [11]–[13]. As can be seen, the converter implemented is the lowest power dc-dc converter reported.

VIII. Conclusion

In this work, an ultra-low-power PMU has been described that powers an implantable wireless sensor by extracting energy from the EP, a 70 to 100mV bio-potential existing in the mammalian ear. This is the first reported PMU system that can sustain itself by extracting energy from a mammalian bio-potential. The power budget of the entire system is 1.1–6.25nW. Low power control circuits operating at a low voltage (0.8–1.1V) and a low frequency (12.8Hz) help keep the quiescent power of all the control circuits down to 544pW. Using leakage reduction techniques normally used in low power digital designs using a Charge Pump, the efficiency of the boost converter is increased. Maximum power

point tracking techniques have not been implemented in this work since for the required sensor, the harvester source impedance (electrode impedance here) remains constant over time for a given electrode. However, techniques presented in [16] can be used in conjunction with this design to cater for an energy harvester that requires maximum power point tracking.

Acknowledgment

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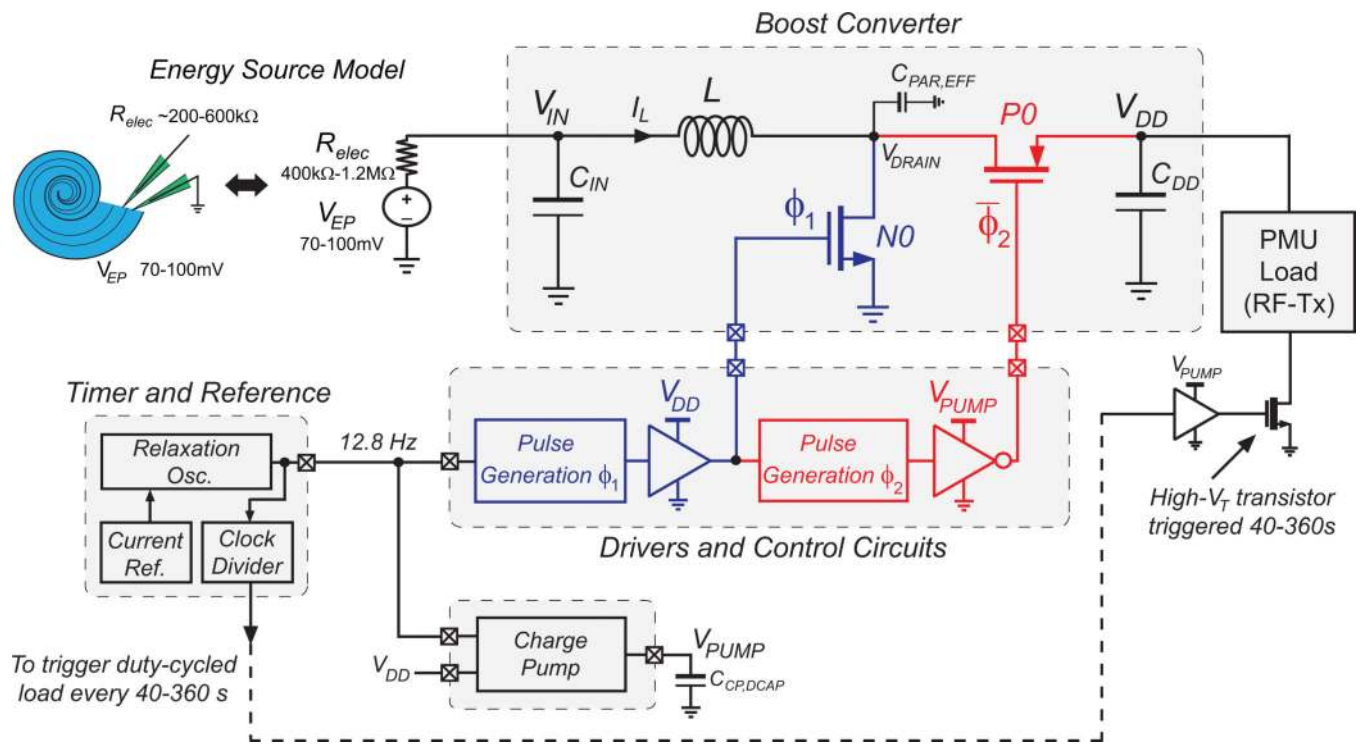
Fig. 1.
nW Power Management Unit
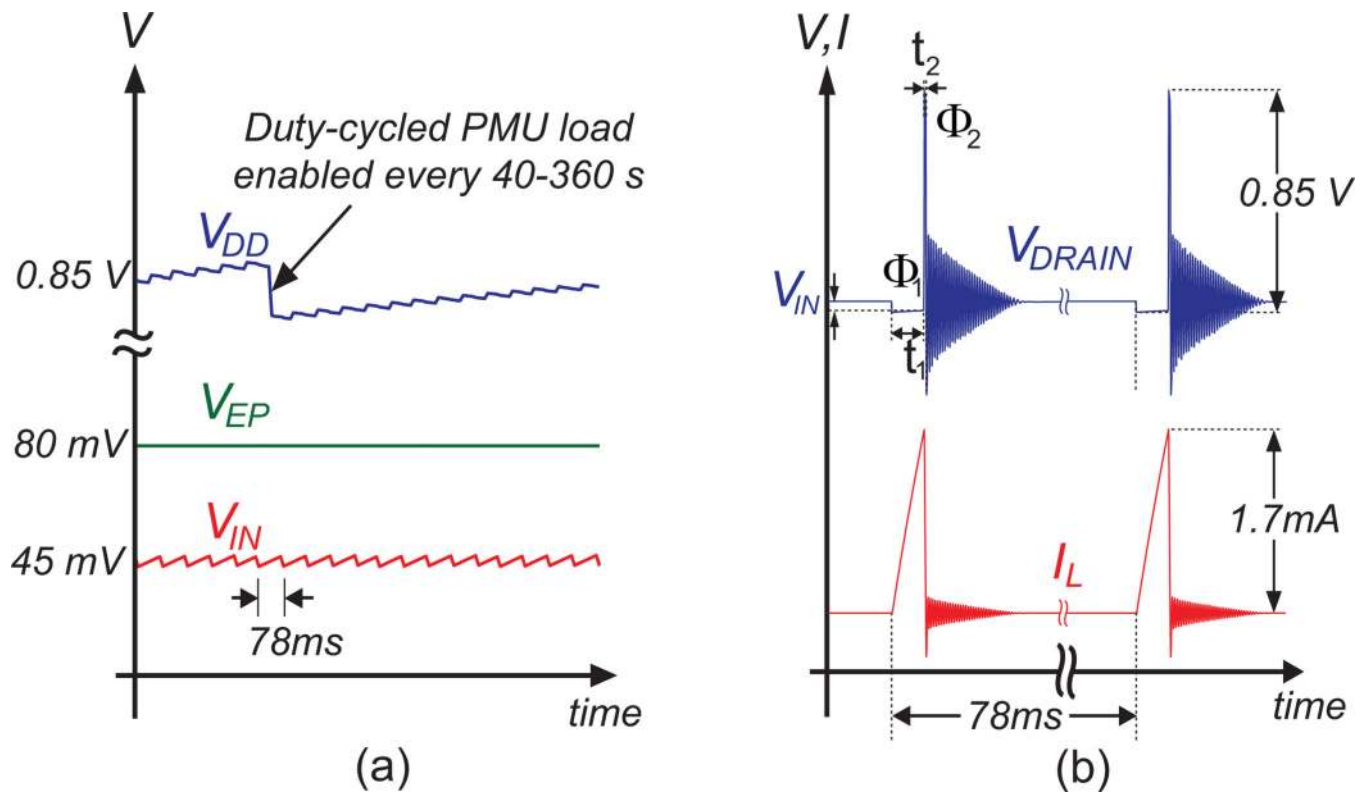
Fig. 2.
Boost Converter Operation, (a) Boost converter trickle charging system power supply, (b)
Boost Converter Operation on a cycle basis
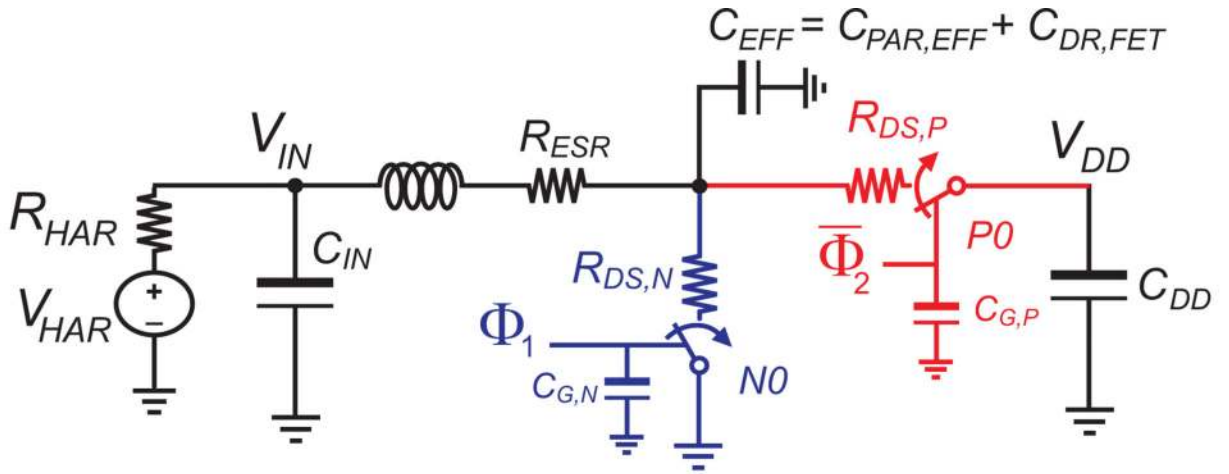
$$Conduction\ Loss = I_{N,RMS}^2 R_{DS,N} + I_{P,RMS}^2 R_{DS,P} + I_{IN,RMS}^2 R_{ESR}$$

$$Switching\ Loss = C_{G,N}V_{gate}^2 f_s + C_{G,P}V_{gate}^2 f_s + 0.5C_{EFF}V_{DD}^2 f_s$$

(a)
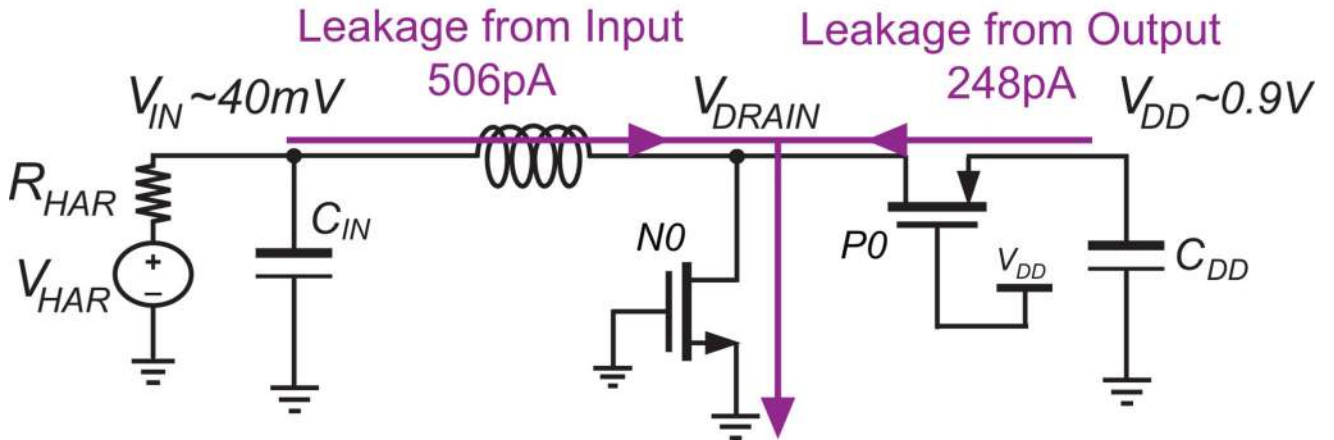
(b)

Fig. 3.
Boost Converter Losses, (a) Conduction and Switching Losses, (b) Leakage Paths in Boost Converter, leakage current simulated in typical corner
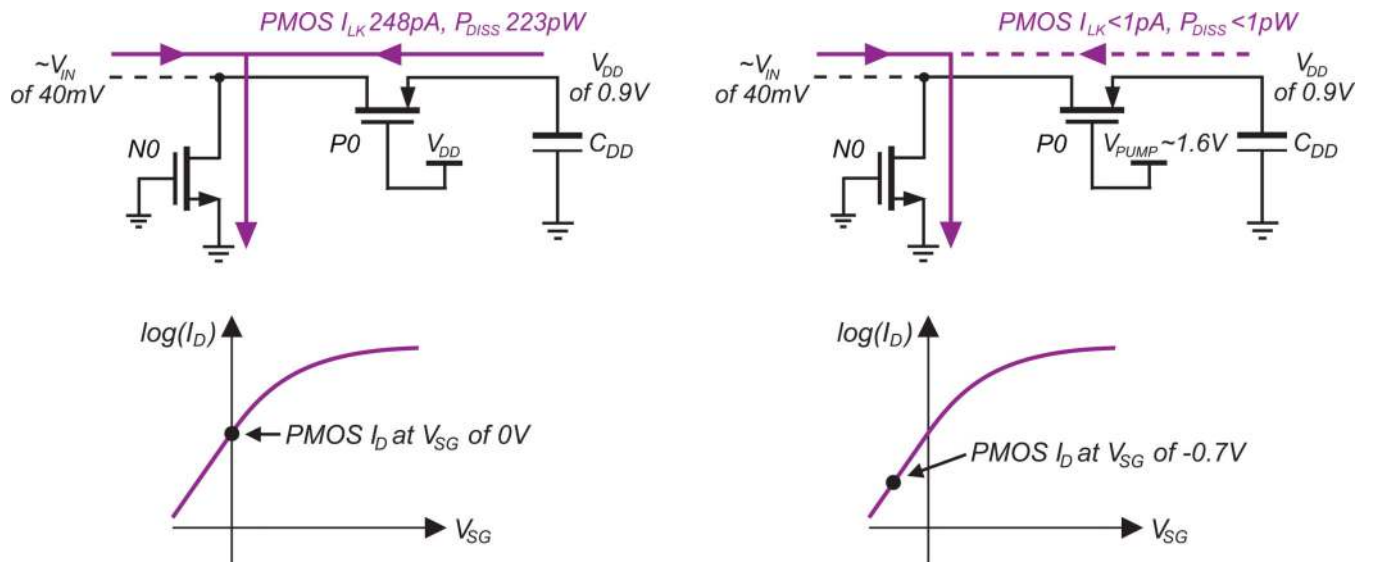
Fig. 4.
Leakage reduction by negative source to gate bias
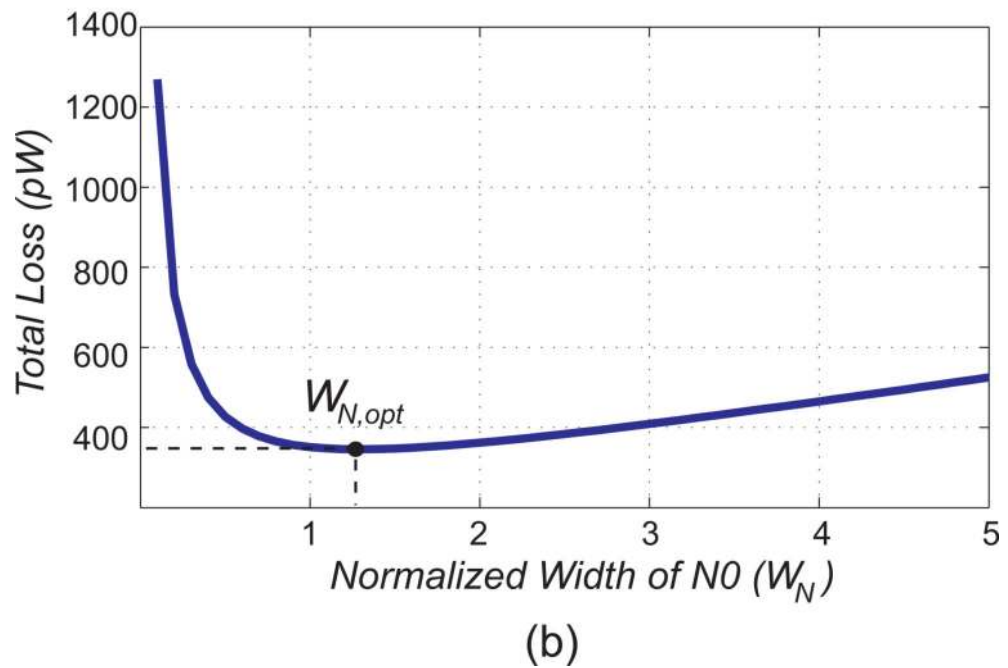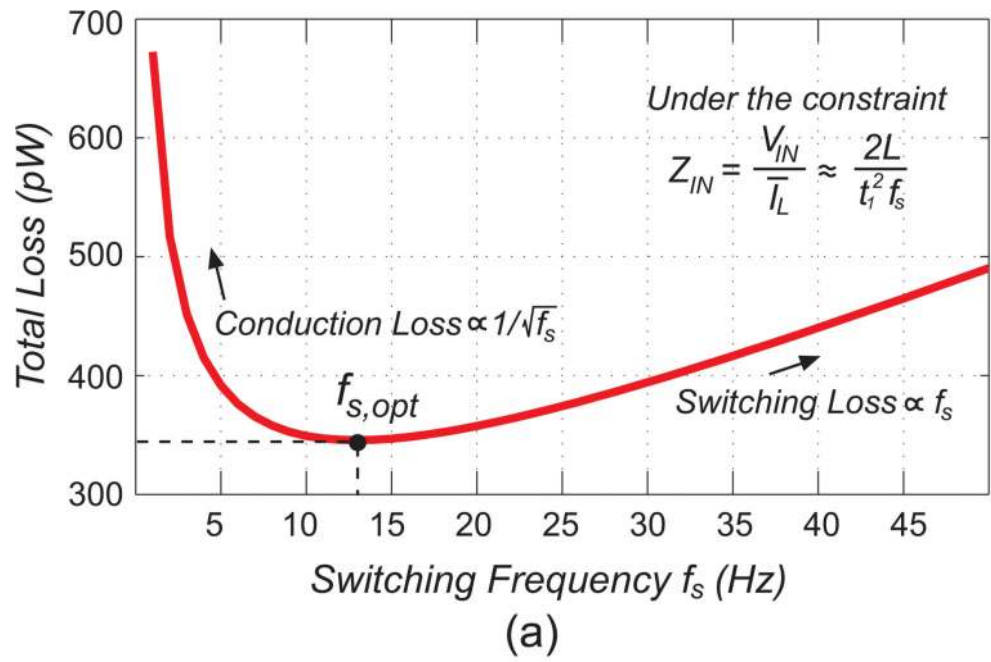
Fig. 5.
Loss Optimization with respect to (a) f_s, (b) W_N
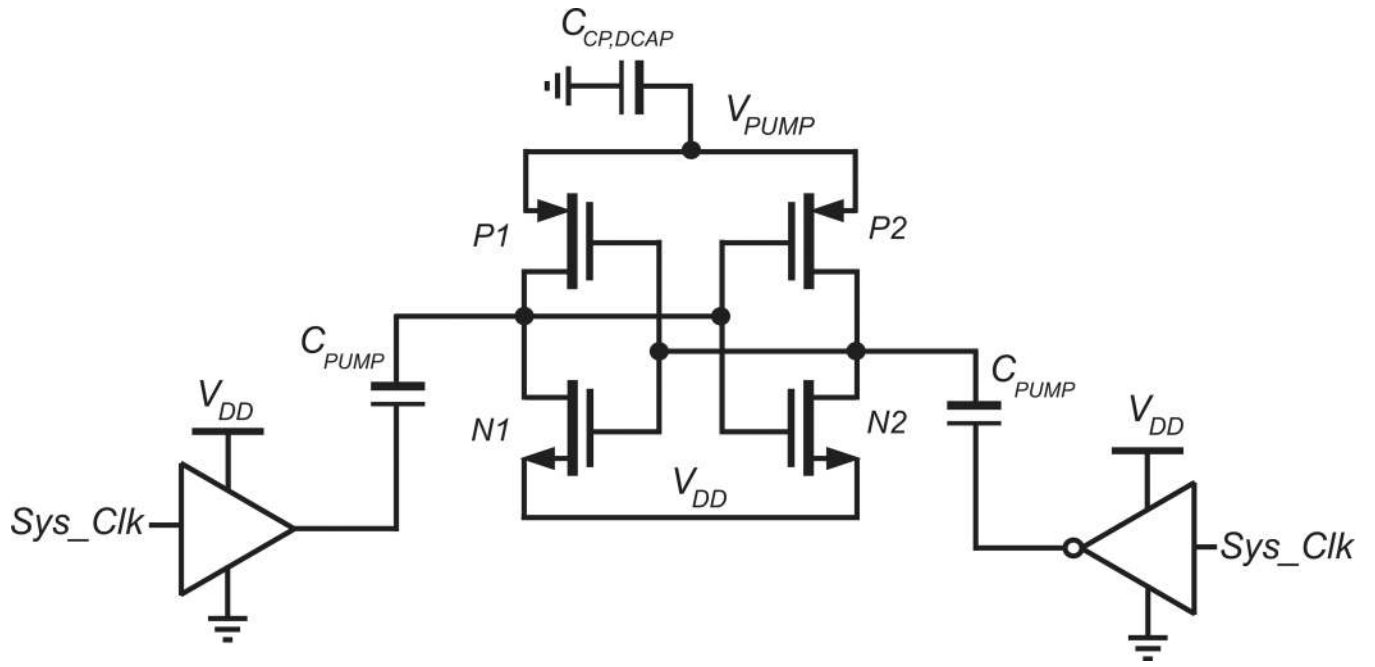
Fig. 6.
Charge Pump for Leakage Reduction
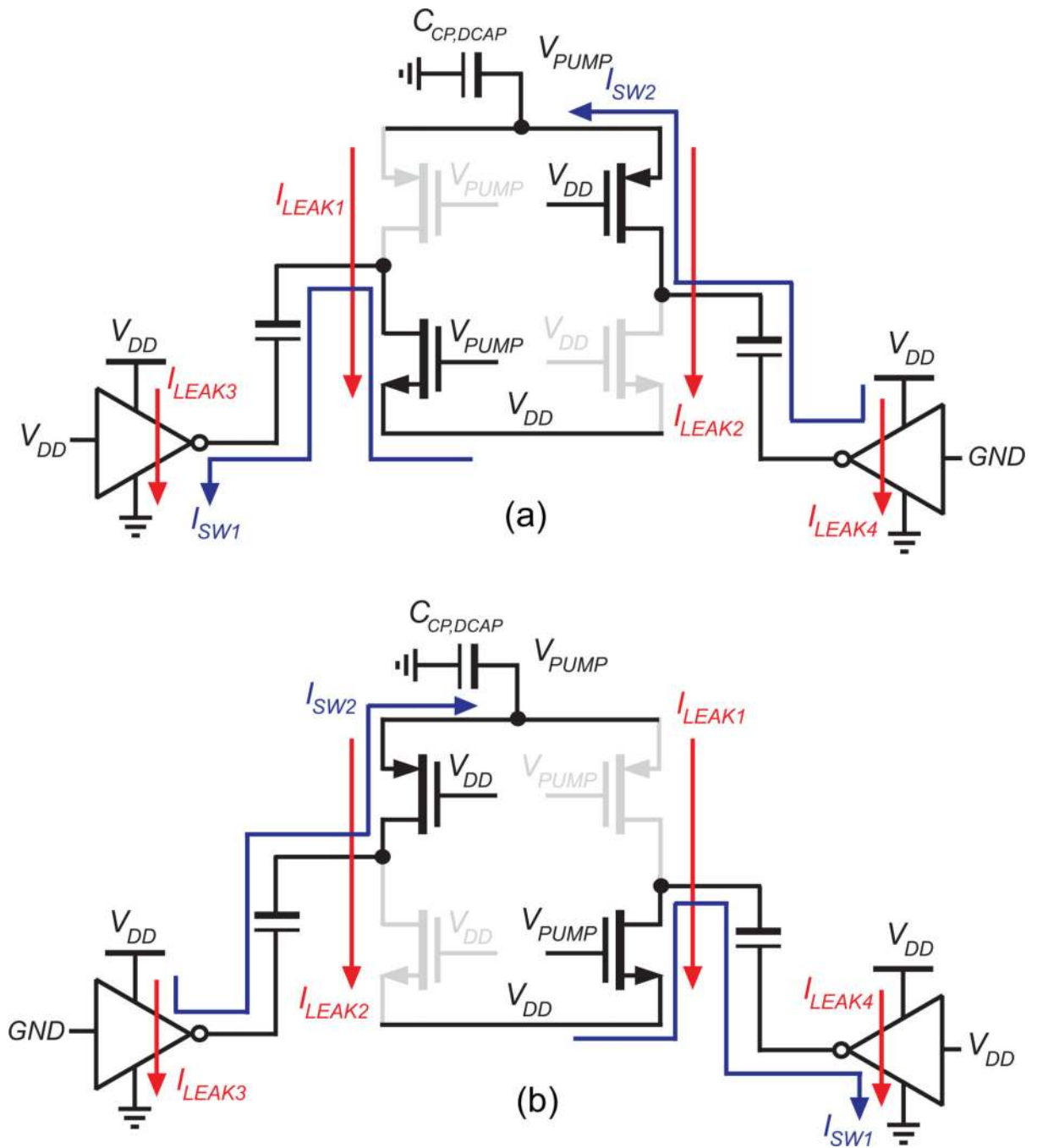
Fig. 7.
Current Paths Charge Pump in: (a) *Sys_Clk=GND*, (b) *Sys_Clk=V_DD*
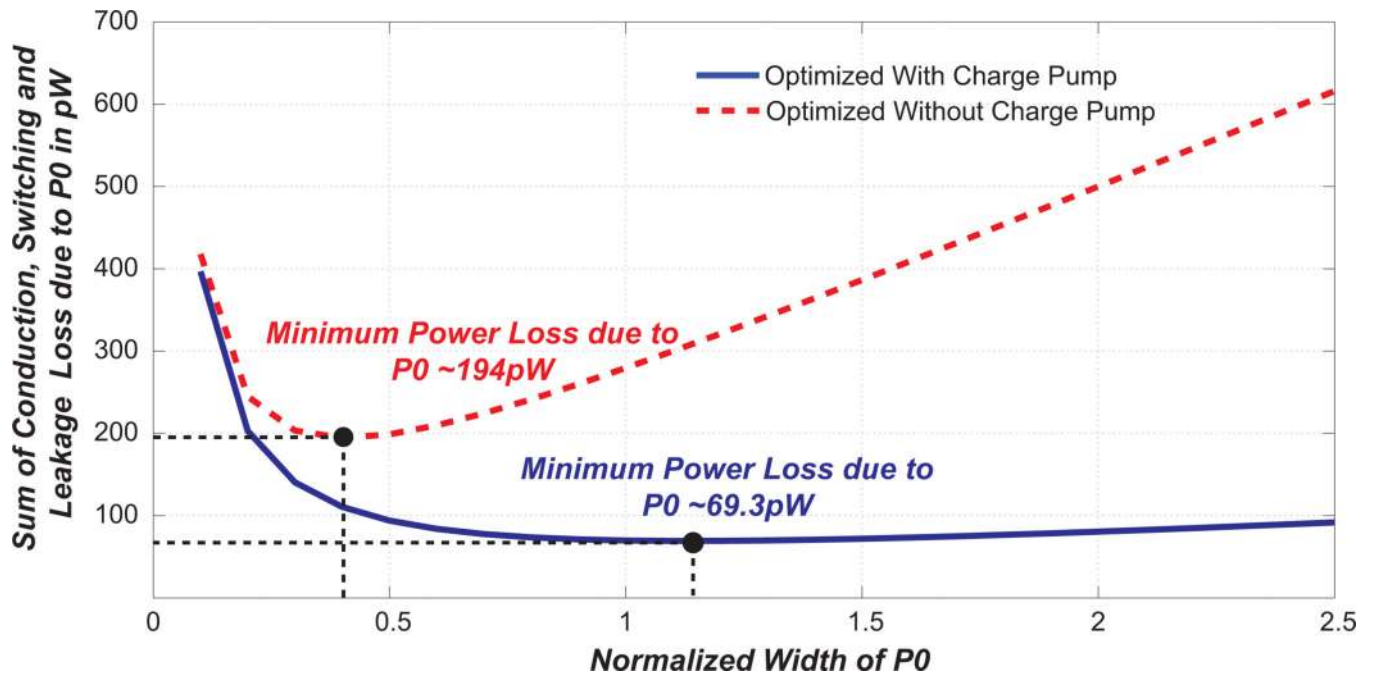
Fig. 8.
Lower Minimum Loss achieved by Charge Pump
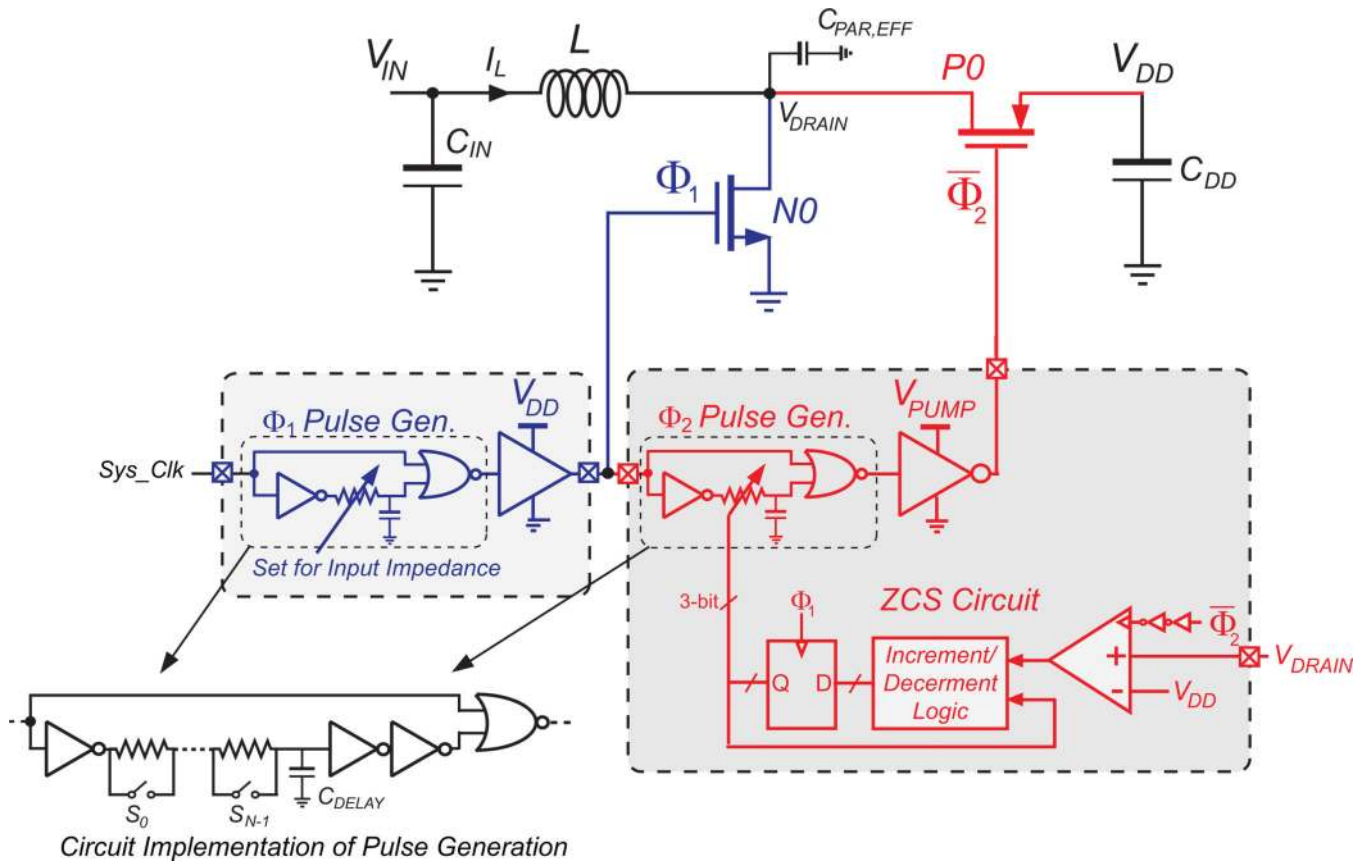
Fig. 9.
Pulse Generators for Φ_1 and Φ_2 phases of Boost Converter
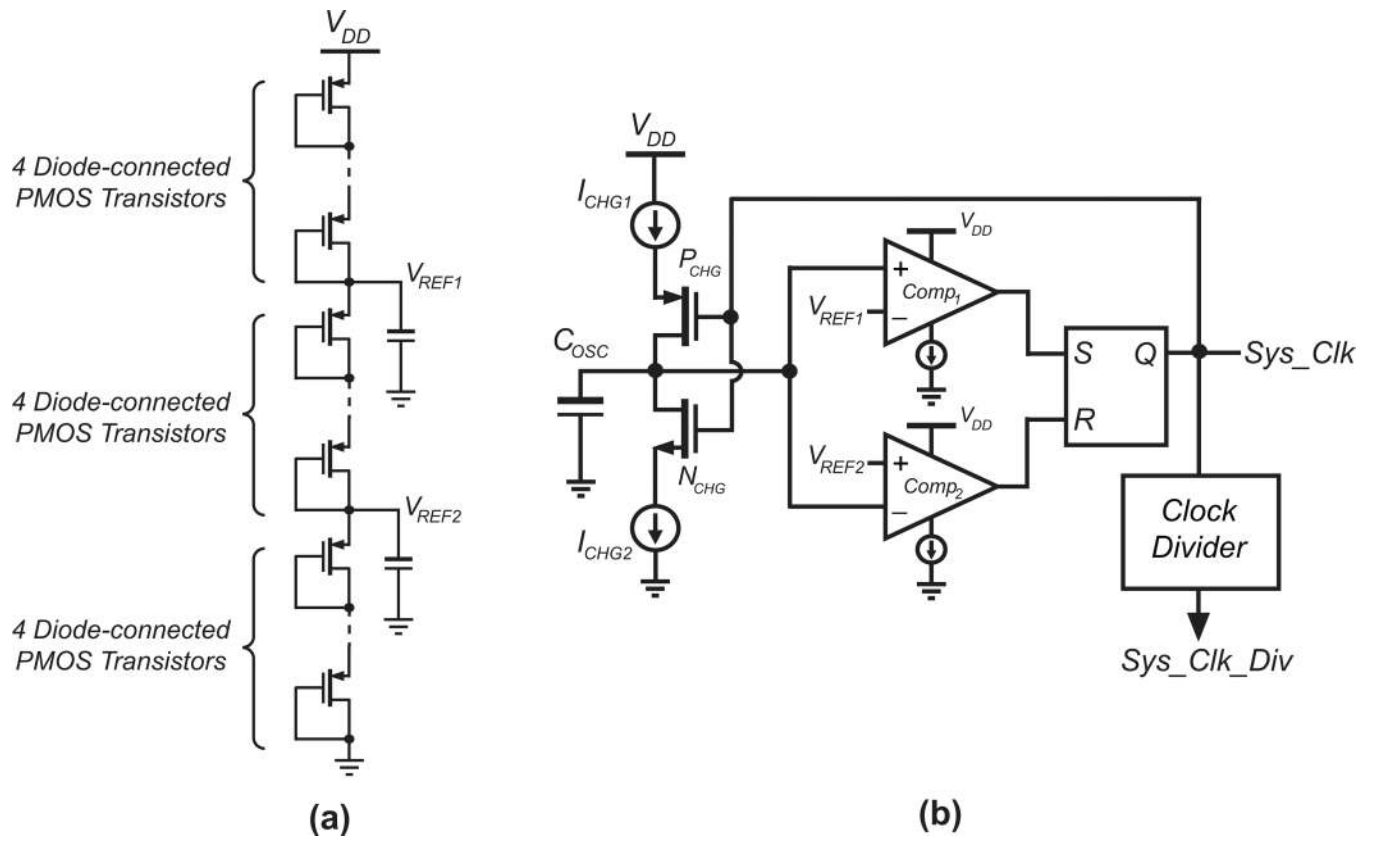
Fig. 10.
(a) Voltage divider for voltage references V_{REF1} and V_{REF2}, (b) pW Relaxation Oscillator
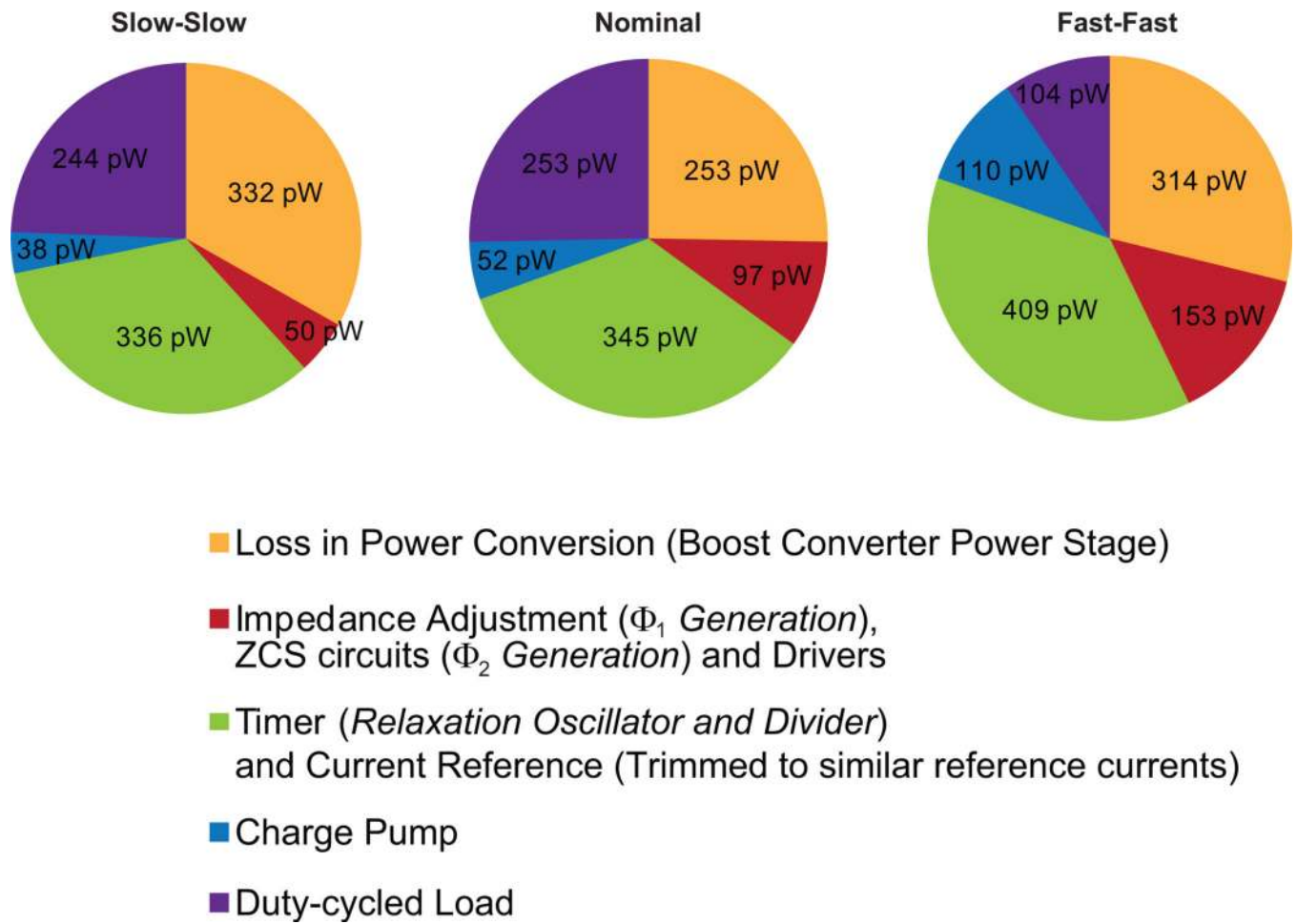
Fig. 11.
Simulated Performance of the PMU under process variations
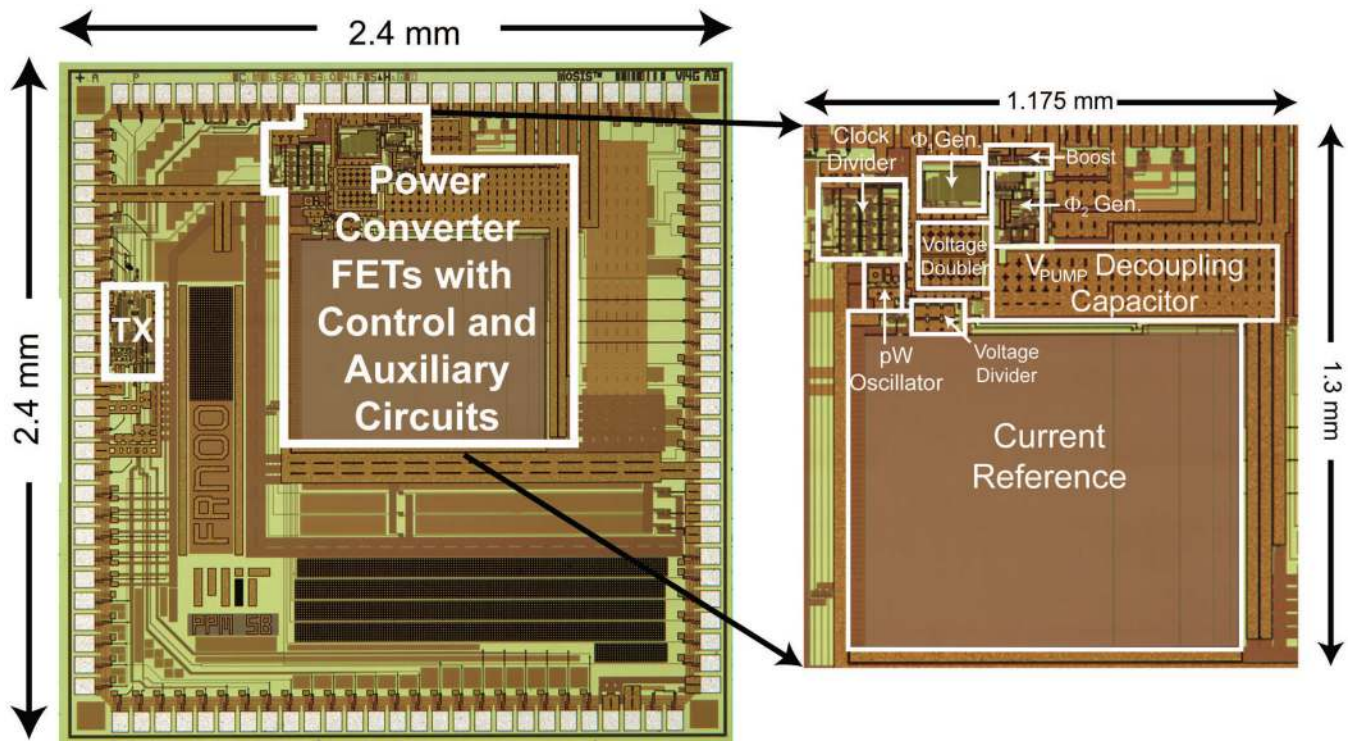
Fig. 12.
Die Micro-photograph with the PMU details
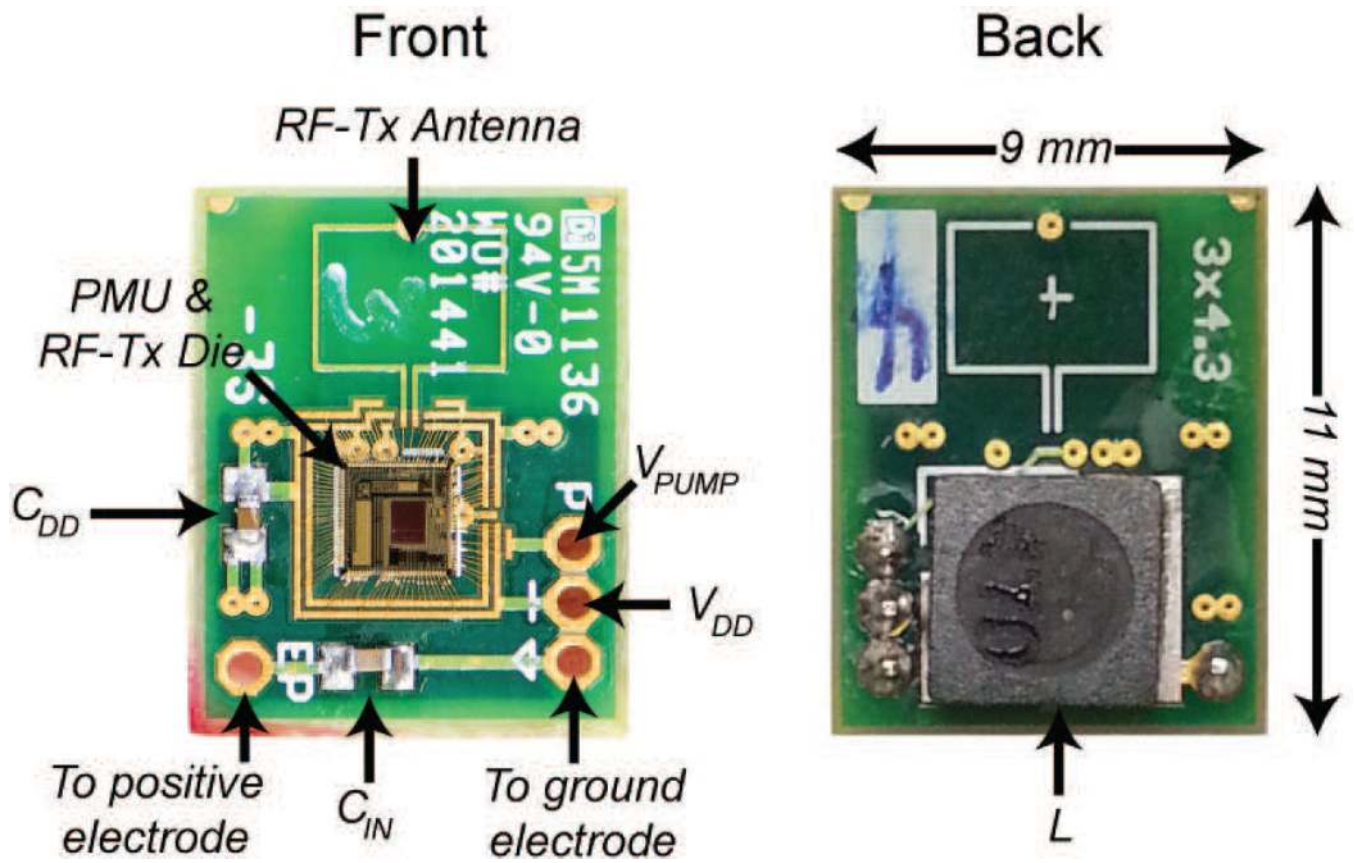
Fig. 13.
Implantable Senor Board Front and Back
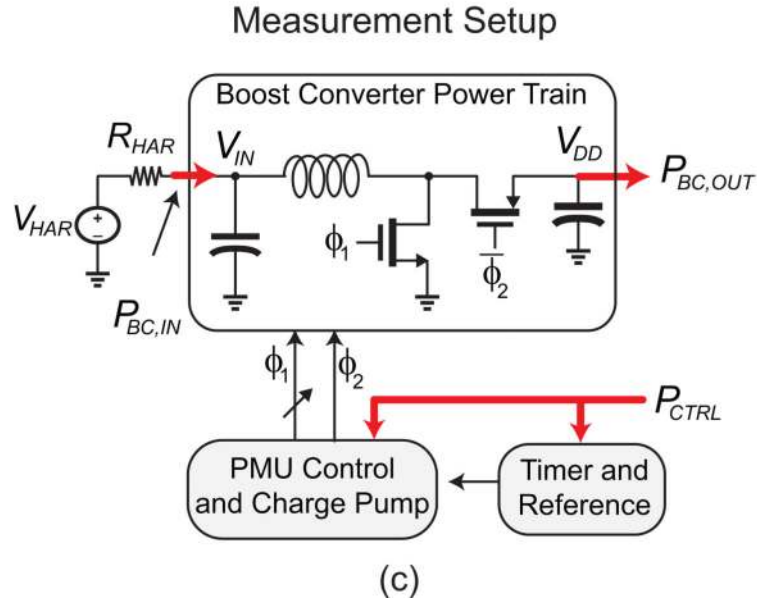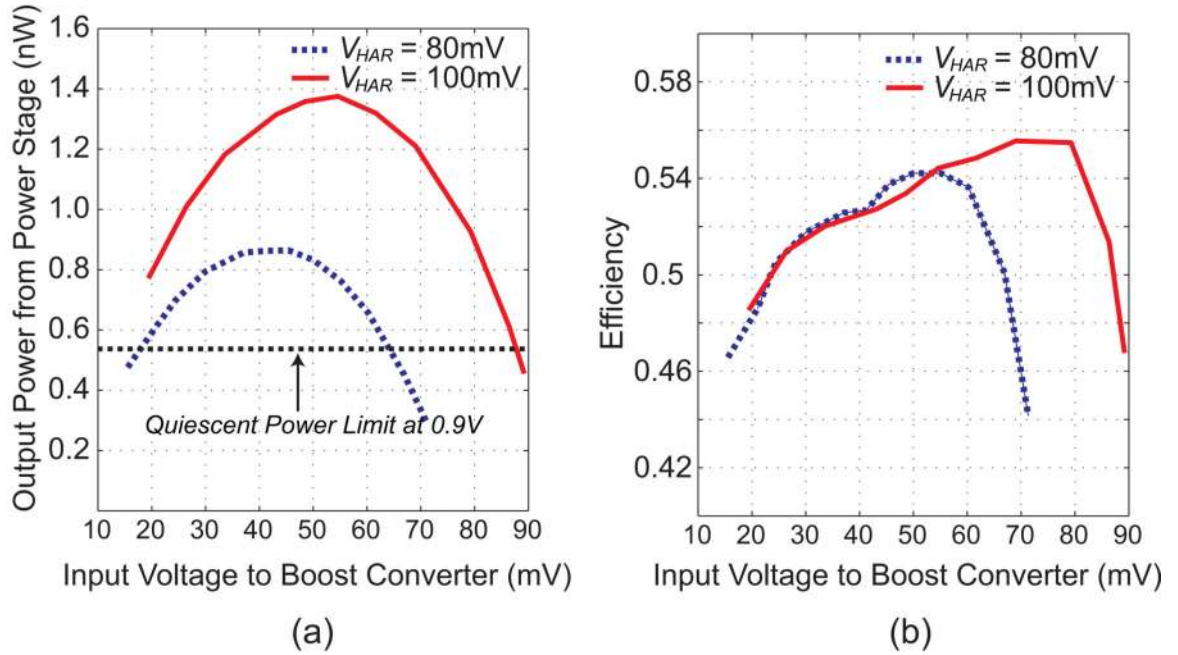
Fig. 14.
Boost Converter Results for different EP voltages: (a) Measured Power v/s Input Voltage,
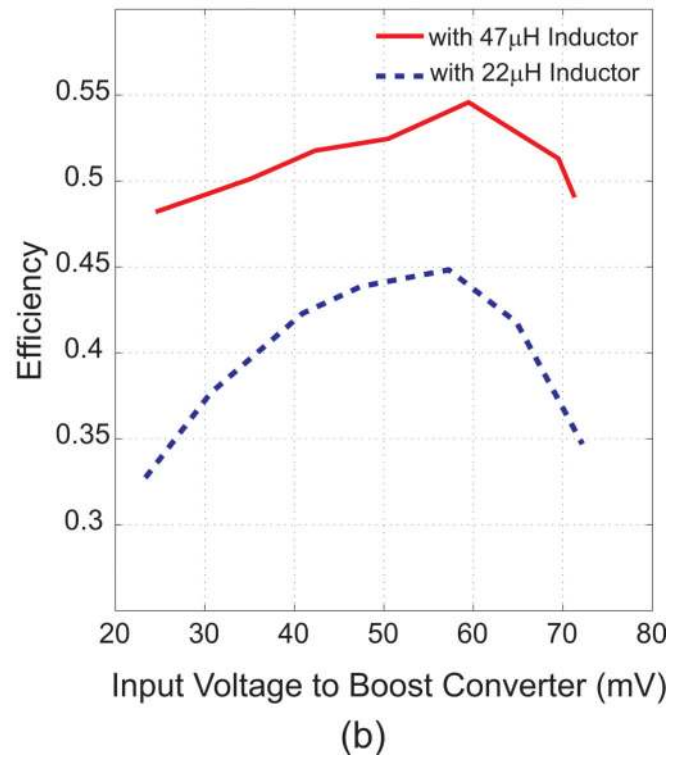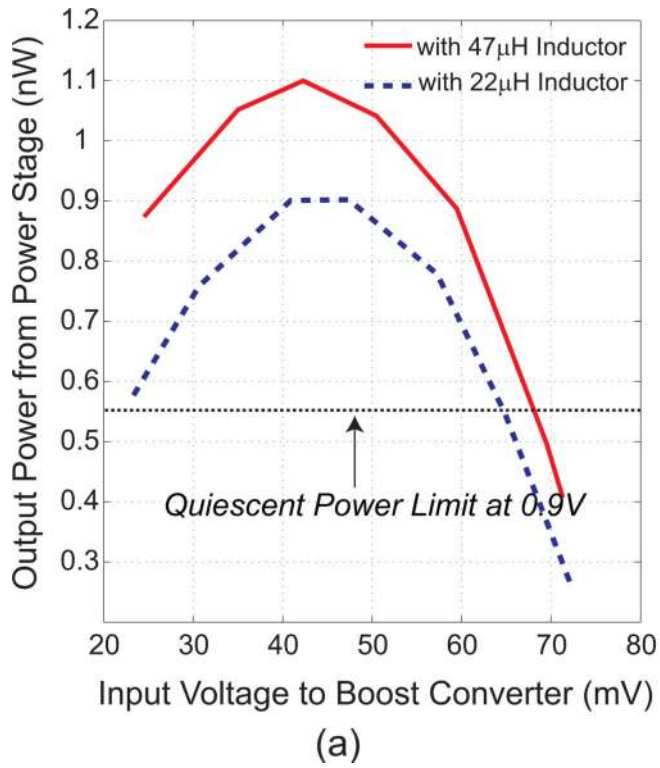(b) Measured Efficiency v/s Input Voltage, (c) Measurement Setup

Fig. 15.
Boost Converter Results with 80mV EP for different inductors: (a) Measured Power v/s
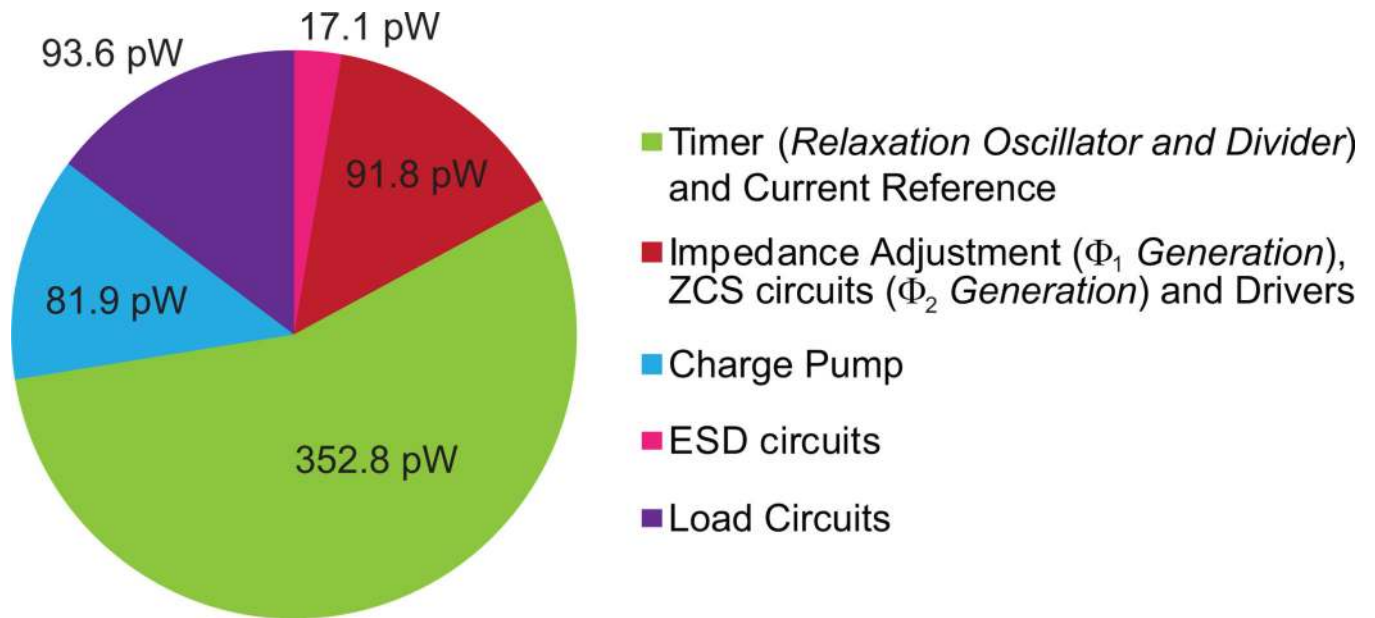Input Voltage, (b) Measured Efficiency v/s Input Voltage

Fig. 16.
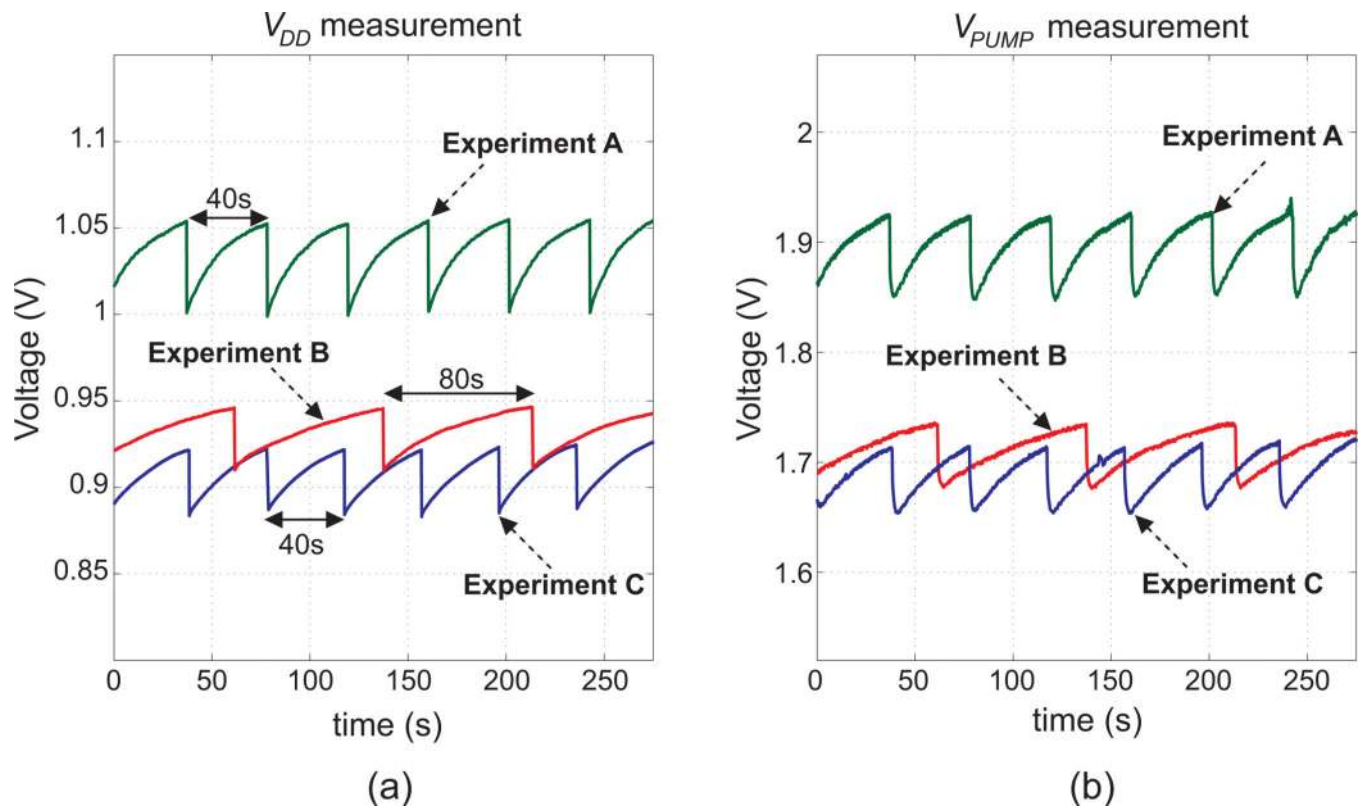Power Consumption of Individual Circuit Blocks

Fig. 17.
Short Term Transient Measurements: (a) V_{DD} measurement, (b) V_{PUMP} measurement

	[11]	[12]	[13]	This Work
Topology	Switched Capacitor Charge Pump (Boost)	Boost	Buck	Boost with Voltage Doubler
Voltage Conversion	450mV boosted to 3.6V	80mV-2.5V boosted to 3-5V	2-5.5V step down to 1.3-5V	Inductive Boost:- 20-70mV boosted to 0.8-1.1V Voltage Doubler:- 0.8-1.1V boosted to 1.5-1.9V
Output Power	10nW to 160nW	1μW-30mW	2.5μW-125mW	544pW-4nW
Efficiency at Ultra-Low Power	35% at 10nW	20% at 1μW	55% at 2.5μW	53% at 1.2nW (1.1nW to PMU)
Quiescent Power	7.3nW	9.9nW	760nW	544pW

Fig. 18.
Comparison with State-of-Art Ultra-Low Power DC-DC Converters