256×256, 100kfps, 61% Fill-factor time-resolved SPAD image sensor for microscopy applications

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***Abstract*—**A 256×256 Single Photon Avalanche Diode (SPAD) image sensor operating at 100kfps with fill factor of 61% and pixel pitch of 16μm is reported. An all-NMOS 7T pixel allows high uniformity gated operation down to 4ns and ~600ps fall time with on-chip delay generation. The sensor operates with 0.996 temporal aperture ratio (TAR) in rolling shutter and has a parasitic light sensitivity (PLS) in excess of -160dB when operated in global shutter. Gating and cooling allow the suppression of dark noise, which, in combination with the high fill factor, enables competitive low-light performance with electron multiplying CCDs (EMCCDs) whilst offering time-resolved imaging modes.

I. Introduction

SPAD image sensors offer photon shot noise limited performance with picosecond timing resolution for applications in fluorescence lifetime imaging microscopy (FLIM), time-of-flight 3D imaging and spectroscopy [1]. However, the external quantum efficiency (EQE) of these sensors has been limited by low fill-factor and large pixel pitches required by the complex digital pixel electronics necessary to count and time the SPAD pulses. Analog circuit approaches or single bit quanta pixels have considerably simplified the pixel electronics replacing counting or full-well capacity with oversampled readout and external frame summation [2,3]. The resulting improvements in EQE have been considerable but are still an order of magnitude lower than the best EMCCD or BSI sCMOS sensors.

The sensor presented in this paper (Fig. 1) achieves the highest peak EQE of around 24.4% at 480nm and 3V excess bias of any SPAD image sensor without requiring microlenses. A 7T all-NMOS pixel with 16μm pitch and 61% fill-factor is comparable with that available from state-of-the-art, non-imaging Silicon Photomultipliers (SiPM) or Multi-Pixel Photon Counters (MPPC) (see Fig.2). Pixel bias voltage settings allow simultaneous optimization of readout settling time and pixel dynamic memory leakage whilst achieving uniformly distributed 4ns gate with ~600ps fall time. The frame rate of 100kfps ensures that there is practically no read-out pile-up, and hence no loss of photons, in typical microscopy usage scenarios of around 10k photons/s/pixel at output aggregate video rates of 10fps. Gating and cooling of the sensor are shown to significantly suppress dark count noise resulting in comparable performance to an EMCCD sensor whilst providing FLIM capability.

II. Sensor Architecture

The sensor is implemented in 130nm 1P4M CMOS image sensor technology. With the maximization of fill factor being a priority in the design of the chip, the compact 7T all-NMOS pixel architecture depicted in Fig. 4 was optimized for binary operation from [4]. The pixels are read out via dynamic comparators at the ends of the columns (situated in an alternating top/bottom pattern) with a 40ns line time (Fig. 3). Each pixel presents a binary output of either 0 (no detected photon) or 1 (for at least one detected photon). Read out noise is negligible due to the large voltage swing resulting from a photon detection. A 64 bit-wide, 100 MHz digital output bus is used to read the bit-plane data off-chip. Lines on the output bus serve four pixel columns each, whose contents are transferred using 4-bit serializers. The range of pixel rows read out may be reduced to further increase the frame rate. Exposures are taken using a rolling shutter, on which a global gate signal, produced by a programmable, on-chip pulse generator, may be imposed. The gate signal, in turn, can be triggered by an external sync signal. The individual line reset and read signals are generated by a shift register. In the test results presented here, the necessary control and clocking signals (and chip configuration) for acquiring image frames were handled by an FPGA board (Opal Kelly XEM6310). The board is capable of continuous data streaming, at rates of >100MB/s, when the on-board SDRAM chip is used as an output buffer.

With the raw output consisting of binary frames, or bit-planes, captured at a fast rate, the sensor can be considered as an example of a Quanta Image Sensor [5] (in other words, an oversampled binary camera). Conventional, "grayscale" frames can be produced by aggregating bit-planes in time and/or space. Different methods of aggregation may be preferable depending on the application, such as non-overlapping, rolling, and signal-only summations [6].

III. Pixel Operation and Gating

The pixel circuit is shown in Fig. 4 and has four main parts: (1) a SPAD with passive quenching, which produces a voltage pulse whenever the SPAD triggers, (2) time gating circuitry (3) a switched current source, controlled by the time-gated SPAD pulse, that draws charge away from a capacitor C, and (4) a source follower to buffer the voltage VC of the capacitor onto the column.

The values of the quench voltage *VQ* and source voltage *VS* have significant bearing on the operation of the circuit, especially on the rise time of the time gate. As indicated in Fig. 5, SPAD pulses have a relatively long tail, so to achieve sharp time gating, one must ensure that only SPAD events where the main pulse – rather than just the tail of the response – falls within the time gate enable signal are registered. Increasing *VQ* shortens the tail of the SPAD pulse, whilst increasing *VS* raises the voltage threshold required to activate the switched current source. Both actions therefore result in the actuation of the current source becoming increasingly reliant on the peak of the SPAD pulse, leading to sharper gating. However, too high a *VQ* or *VS*, and the current source will not be switched on for long enough (if at all), or draw away enough current from *VC*, for all SPAD pulses to be registered. Loss of sensitivity therefore occurs, necessitating a careful balance to be struck in the choice of *VQ* and *VS*.

Figures 6 and 7 plot experimental data showing the effect of *VS* and *VQ*, respectively, on the effective time gate. The results were obtained by imaging the diffused light from a pulsed laser (Hamamatsu PLP-10), whose sync signal, delayed in time by a delay generator (SRS DG645), was used to trigger the time gate of the sensor. For each voltage setting, the time delay was swept across a range of values to obtain the time gate profile. The results indicate an optimized time gate that is comparable to other SPAD image sensors [7], and is ideal for selectively time-gating the common fluorophores used in microscopy. Aside from its role in optimizing the time gate, another important function of *VS* is reducing the voltage swing on *VC* and thereby accelerating settling on the column line, thus increasing the frame rate. Furthermore, *VS* also reduces the leakage from *VC*, an effect illustrated in Fig 8. It can be seen that for *VS*=0V, the majority of pixels show leakage as the exposure time approaches 10s. However, even moderate values of *VS* bring pixel leakage back to minimal levels.

IV. Example Data

The sensor was used to image a Convallaria slide on an Olympus IX81 microscope, with excitation being provided by a pulsed laser (Picoquant LDH-405). The sync signal from the laser was fed into a delay generator (SRS DG645), which then supplied the trigger signal for time gating. Reference (non-time-gated) images were captured of the same field of view, by an EMCCD camera (Hamamatsu ImageEM) via a 50:50 beam splitter. The fluorescent response of the sample was very weak, with only around two photoelectrons/pixel/ms being registered by the EMCCD, which is lower than the median dark count rate of the SPAD device. Without gating, the SPAD image (shown in Fig 9a) is indeed rather poor. However, by applying a 12ns time gate, adjusted in time so as to encompass the fluorescent response of the sample, a significantly better image is obtained (Fig. 9b). The resulting image is still considerably noisier than the corresponding EMCCD output (Fig. 9c), with areas away from the brighter features having a five times higher standard deviation. The advantage of the SPAD device is the ability to characterize the fluorescent response (lifetime). This is done by sliding the time gate with respect to the laser pulse, which, for the 10×10 ROI indicated, gives the response curve shown in Fig 10. The rising edge of the profile corresponds to the integral of the fluorescent response. By fitting an exponential to it, an estimate for the fluorescence lifetime may be obtained. Summing pixels values in groups of 10×10, and repeating the above analysis, leads to the lifetime map of Fig 9d, which shows some distinct regions, the lifetimes being in line with expected values.

Whilst the EMCCD device has built-in cooling, the SPAD results are for room temperature and it is therefore important to assess the improvement that cooling provides. Fig. 11 plots the dark count rate (DCR), as measured at 25ºC and -5ºC, for different excess bias settings. The DCR is seen to reduce by an order of magnitude for lower bias values. This is consistent with previous studies involving similar SPAD structures, which suggested a halving of DCR for every 8ºC temperature drop. Thus cooling, when used in conjunction with time gating, offers a means of matching the signal to noise ratio (SNR) offered by EMCCD in low light imaging. In the above example, it is expected that cooling down to -15ºC (giving a ×32 reduction in DCR with respect to room temperature) would result in equivalent SNR between the two systems.

V. Conclusion

A time-resolved SPAD image sensor, designed for microscopy, and featuring the highest quantum efficiency in its class, has been presented. The sensor's characteristics are summarized in Table I.

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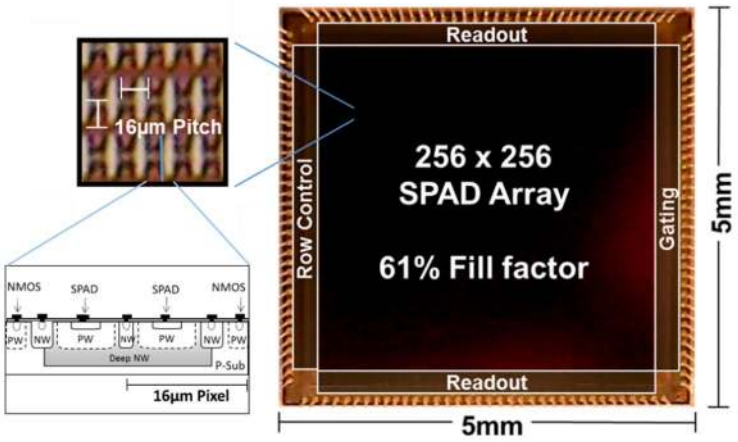

Fig 1. Micrograph of image sensor and cross-section of SPAD structure

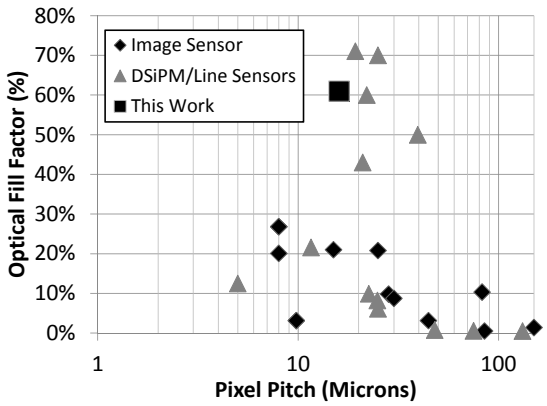

Fig 2. Comparison of pixel pitch and fill factor with existing SPAD sensors

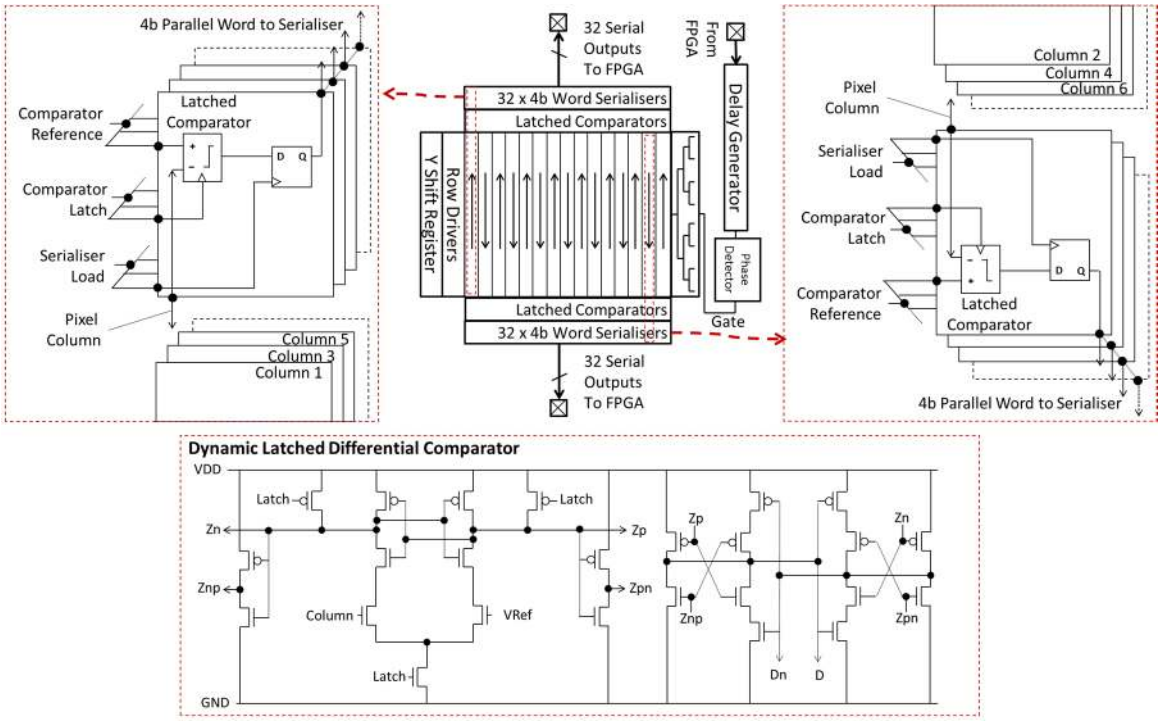

Fig 3. Readout architecture and schematic diagram of comparators

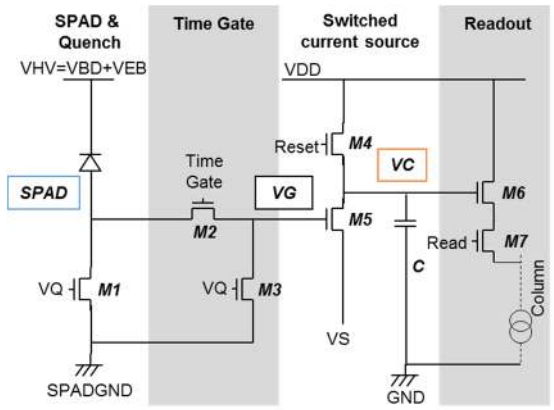

Fig 4. Pixel architecture, highlighting the voltage nodes *SPAD, VG,* and *VC*

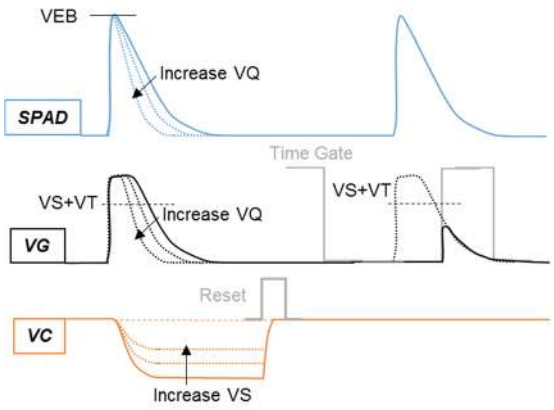

Fig 5. Example voltage waveforms for pixel circuitry, indicating the effect of varying *VQ* and *VS*. As a result of the time gate shown, only the tail of the second SPAD pulse is seen at *VG*, and as it is lower than *VS* plus the transistor threshold voltage *VT*, the pulse is not registered.

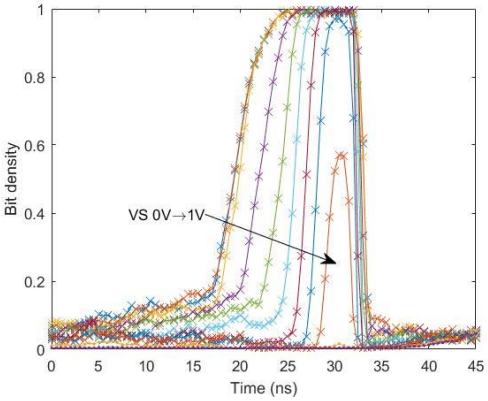

Fig 6. Time gate profile for varying *VS* (*VQ*=1.3V, *VHV*=16V). Each data point corresponds to the average bit density, over the whole array, based on 1000 bit-plane exposures. At high *VS* the time gate edges are seen to become "eroded", indicating a loss in sensitivity.

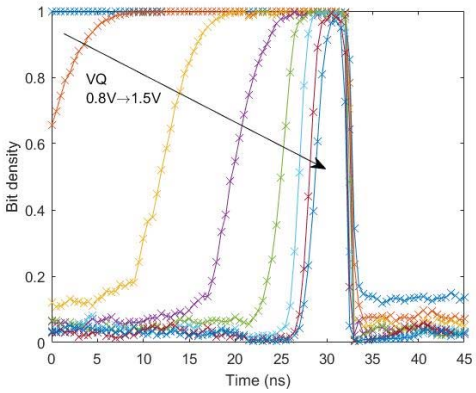

Fig 7. Time gate profile for varying *VQ* (*VS*=0.6V, *VHV*=16V). The results indicate that a 4ns time gate (FWHM), with ~600ps fall-time is achievable.

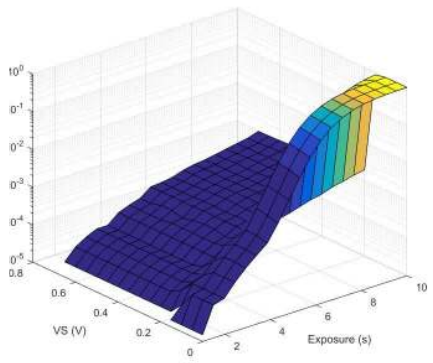

Fig 8. Plot of the density of pixels that "flip" due to leakage, as a function of VS and exposure time, under office lighting The SPAD bias voltage *VHV* set to 0V so that there are no SPAD events.

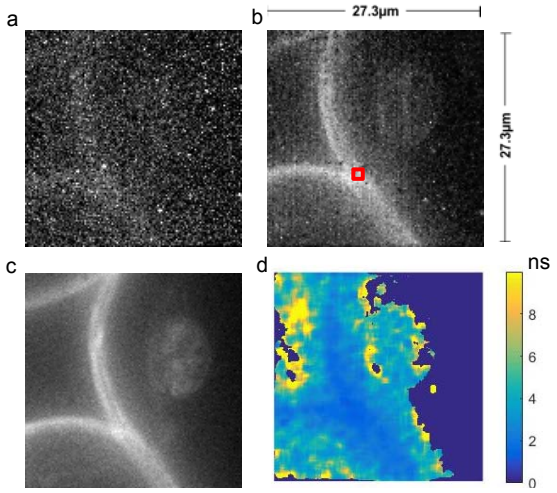

Fig 9. Convallaria slide, as observed through a ×150 objective, and imaged using a) SPAD sensor with no time gating (VHV=16V), b) SPAD with 12ns gating, c) EMCCD (EM gain=400), and d) fluorescence lifetime estimate derived from a set of gated SPAD images. SPAD images are composed by summing 1000, 100µs bit-plane exposures (for a total exposure time of 1s). Hot pixel and background compensation has been applied.

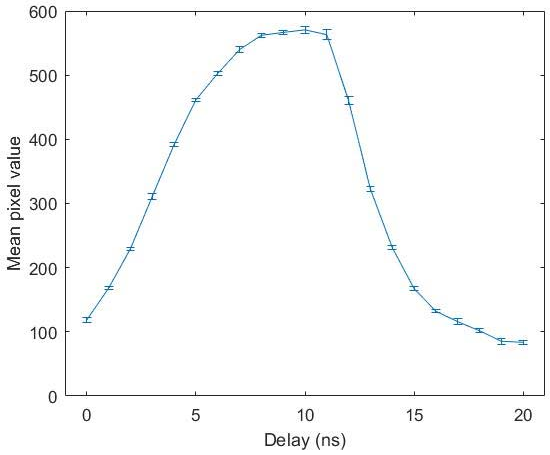

Fig 10. Mean pixel intensity over the ROI shown in Fig. 9b (square), as a function of the time delay imposed on the time gate, varied in steps of 1ns. The observed profile is indicative of the fluorescent response of the microscopy sample. To generate Fig. 9d, the first 10 time delay settings were used to estimate lifetime, equating to 10s total exposure time.

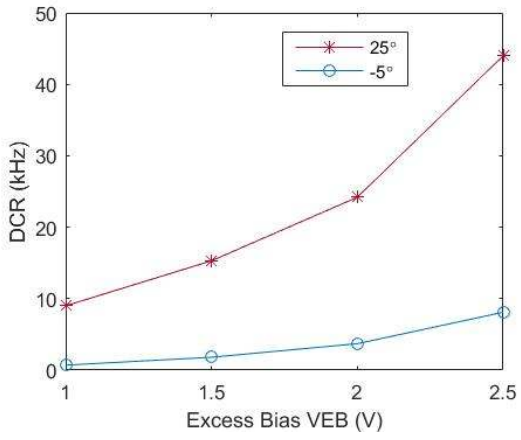

Fig 11. The dark count rate plotted as a function of the excess bias at room temperature and with the chip cooled down to -5°.

Parameter	Value	Condition
Peak EQE	24.4%	at 480nm and 3V excess bias
Resolution	256×256	
Pixel pitch	16µm	
Fill factor	61%	drawn
Max. frame rate	100kfps	for full array
Read out noise	Negligible	
Dark count rate (median)	<10kHz	at 25° and 1V excess bias
	<100Hz	at -5ºC and 1V excess bias assuming 10ns time gating with 10MHz repetition rate
Min. time gate width	4ns	
SPAD breakdown voltage	13.9V	
PLS	-160dB	
Time gate falling edge mismatch	180ps σ	across whole array

Table I. Chip specifications