280-GHz Schottky Diode Detector in 130-nm Digital CMOS

Ruonan Han[1], Yaming Zhang[2], Dominique Coquillat[3], Julie Hoy[4], Hadley Videlier[3], Wojciech Knap[3], Elliott Brown[4], Kenneth K. O[1, 2]

[1]University of Florida, Gainesville, FL 32603, [2]University of Texas at Dallas, Richardson, TX 75080
[3]University of Montpellier II, 34095, France, [4]University of California, Santa Barbara, CA 93106

***Abstract*-A 2×2 array of Schottky-barrier diode detectors with an on-chip patch antenna and a preamplifier is fabricated in a 130-nm logic CMOS process. Each detector cell can detect the 25-kHz modulated 280-GHz radiation signal with a measured responsivity and noise equivalent power (NEP) of 21kV/W and 360pW/$\sqrt{\text{Hz}}$, respectively. At 4-MHz modulation frequency, NEP should be about 40pW/$\sqrt{\text{Hz}}$. At supply voltage of 1.2V, the detector consumes 1.6mW. By utilizing the detector, a millimeter-wave image is constructed, demonstrating its potential application in millimeter-wave and THz imaging.**

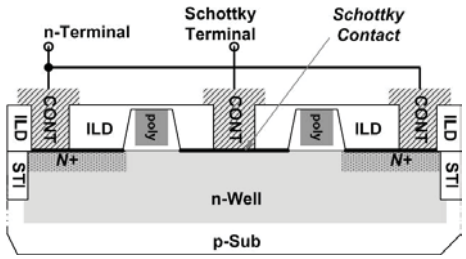
I. Introduction

The electromagnetic spectrum in millimeter-wave and sub-millimeter wave frequency range (30GHz~3THz) is attracting increasing attention for potential applications in concealed weapon detection, aviation assistance, spectroscopy for detection of harmful molecules and breath analyses, short range radar, secured high-speed data transmission and more [1]-[3]. A critical component for the systems for these applications is a detector. The improvement of high frequency capability of CMOS process has made this technology a realistic option for implementing such a detector [4]. In particular, Shallow Trench Separated (STS) Schottky barrier diodes (SBD) fabricated in foundry 130-nm CMOS without any process modifications was shown to have a cut-off frequency of 1.5 THz [5] and has been used to detect 182-GHz amplitude modulated signals; but because of the measurement set-up, the responsivity and noise performance could not be characterized [6]. NMOS transistors have also been utilized to detect signals at 600GHz -800GHz [7],[8].

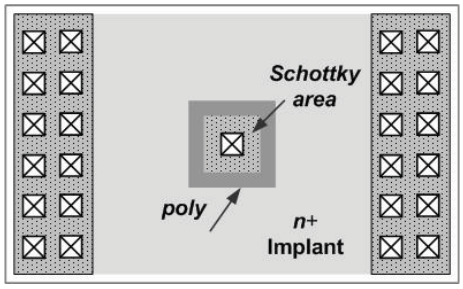
Schottky diodes, being a bulk type device instead of NMOS transistors in linear region of operation with an inversion layer, should have lower loss and better high frequency performance. As a step toward improving the understanding of this, a 280-GHz detector that uses a Polysilicon-Gate Separated (PGS) Schottky Barrier diode (Fig. 1) fabricated in 130-nm CMOS and its characteristics are reported in this paper. An image formed using this detector is also reported.

II. Schottky Diode and Square-Law Detection

A PGS SBD in digital foundry CMOS was first reported in 2009 [4]. Its unit-cell cross section and top view are shown in Fig.1. Polysilicon gates are used to separate the anode and the cathode. Compared to STI-separated SBD's, the current path between the Schottky contact area and cathode n^+ doping region in a PGS diode is shorter. The series resistance drops from ~13Ω to ~8Ω (30 unit cells). Due to a design rule limitation, the Schottky area increases from 0.32×0.32um^2 (STI SBD) to 0.4×0.4μm^2 (PGS SBD), which makes the junction capacitance increase from 8fF to 10fF. But, the overall cut-off frequency still increases from 1.5 THz to 2 THz [4].



(a)



(b)

Fig. 1. Poly-Gate-Separated Schottky-barrier diode in 130-nm CMOS process: (a) cross section and (b) top view

Detector voltage responsivity R_v, the ratio between a voltage change Δv across the diode and the input RF power P_{in}, is [9]:

$$R_v = \frac{\Delta v}{P_{in}} = \frac{\Delta i}{P_{in}} \cdot R_j \approx \frac{i^{(2)}(v)}{2i^{(1)}(v)} \cdot \frac{nkT}{qI_D} \approx \frac{1}{2I_D} \quad , \tag{1}$$

where I_D is the diode DC bias current and $i(v)$ is the exponential relationship between diode current and voltage, and $i^{(1)}(v)$ and $i^{(2)}(v)$ are the first and second derivatives. At zero-bias, the voltage responsivity can be very high (R_{v0}=~0.5/I_s). But unfortunately, due to the low saturation current of the diode (I_s=~50nA), junction resistance R_j is too high (~700kΩ) for good power matching. Because of these, the diode is forward biased in the detector design.

III. 280-GHz Diode Detector Design

A schematic of diode detector is shown in Fig. 2. Four

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detector cells are fabricated on the same die. Due to a chip area limitation, the outputs of two detector cells on each side are combined on chip to reduce the number of bond pads. A low-noise preamplifier is included to amplify the detected signal. The C_{couple}'s are off-chip coupling capacitors.

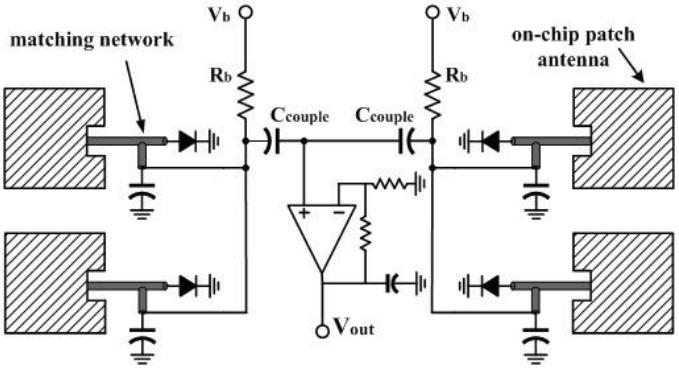

Fig. 2. Schematic of the 280-GHz Schottky diode detector.

280-GHz radiation from an external antenna is picked up by an on-chip 255μm×250μm patch antenna, which is formed by the top Aluminum pad layer. Metal 1 and Metal 2 layers are shunted together to form the ground plane, which shields the lossy silicon substrate. The gap between the patch and ground is 7.2 μm. The antenna performance is simulated in the full-wave 3-D simulator, HFSS. The effects of other nearby three antennas are also included in the simulations. The simulated directivity and gain of each antenna are 5.1dBi and -1.6dB, respectively, which indicate that the efficiency of the antenna is ~21 %. The loss is attributed to the finite metal conductivity and relatively thin gap between the patch and ground plane. The simulated resonant impedance on the edge of the patch is 130Ω. An inset reduces the impedance to 72Ω. The simulated impedance bandwidth of the antenna is ~7GHz.

A forward-biased diode has complex impedance. To improve power transfer, a short-stub matching network is inserted between the antenna and the diode formed using GCPW lines (Fig. 3). The characteristic impedance of line is 72Ω. A multi-finger metal capacitor C_1 connected to the end of section L_2 shorts the 280-GHz signal to ground, while presenting high impedance to DC bias and baseband signal. The detector performance is more sensitive to the parasitics on node "*a*" than to that on node "*b*". Because of this, the diode bias current is injected and the down-converted output signal Δv is extracted from the top plate of C_1. The HFSS-simulated loss of matching network is about 0.6dB.

With the modulation frequency in the kHz range, the sensitivity of detector is mainly determined by the flicker noise of diode [10]:

$$\overline{i_n^2} = K\frac{I_D}{f}\Delta f \quad , \tag{2}$$

If m detector diodes are connected in parallel, the total noise current power will be increased by m times:

$$(\overline{i_n^2})_{total} = \sum_{j=1}^{m}(\overline{i_n^2})_j = mK\frac{I_D}{f}\Delta f \tag{3}$$

However, the total noise voltage power at the output is decreased by a factor of m.

$$(\overline{v_n^2})_{total} = (\overline{i_n^2})_{total}\cdot R_{total}^2 = mK\frac{I_D}{f}\Delta f\cdot(\frac{R_j}{m})^2 = \frac{K}{f}(\frac{nkT}{q})^2\frac{\Delta f}{mI_D} \tag{4}$$

The output signal level does not change in the parallel configuration, so the *SNR* increases by a factor of m.

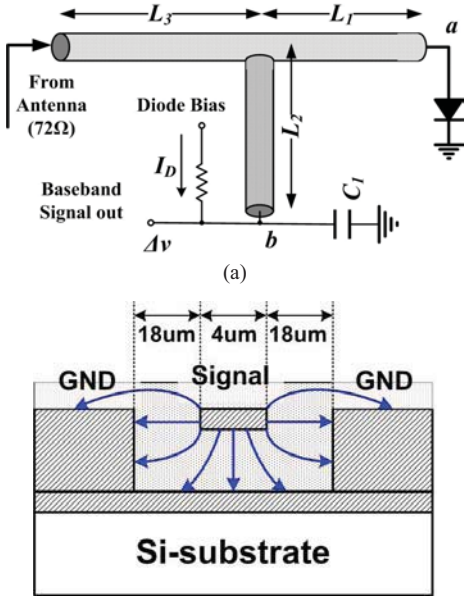

Fig. 3. Matching network between the on-chip antenna and Schottky diode: (a) schematic and (b) cross section of a GCPW line.

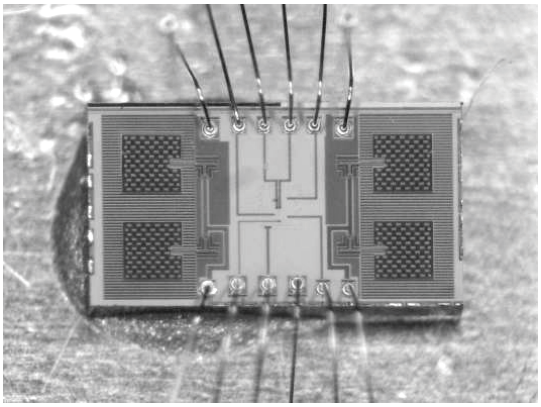

Fig. 4. Die photo of the 280-GHz CMOS SBD detector after mounting on a printed circuit board.

A preamplifier is included on chip and is shared by the two pairs of detectors on the left and right. The amplifier has a common-centroid PMOS input pair to reduce the input referred flicker noise and offset. With a resistive feedback, the amplifier provides 50-dB gain across ~1-MHz bandwidth. The power consumption of the amplifier is 1.3mW at 1.2-V supply voltage.

IV. Measurement Result

The detector is fabricated in the UMC 130-nm logic CMOS process. The chip area is 1.5×0.8 mm^2 and its die photo is shown in Fig. 4. The responsivity and NEP (noise equivalent power) of the detector are measured using the set-up shown in Fig. 5. By cascading a frequency sextupler and a tripler, the input signal at 15.5 GHz is multiplied by 18 times to generate 280-GHz signal. The RF signal is radiated through a horn antenna (22-dBi gain). The radiated power at 280 GHz is 82μW. The source signal is modulated at 25 kHz using a PIN switch. The diode detector is placed at a distance of 2cm, with its antenna aligned to the horn antenna. The outputs of the detector and preamplifier are measured with an oscilloscope and a lock-in amplifier.

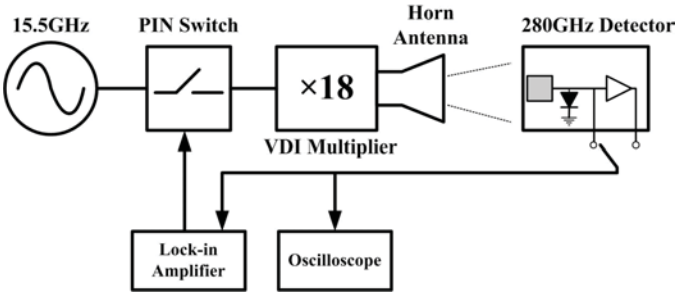

Fig. 5. 280-GHz detector measurement set-up.

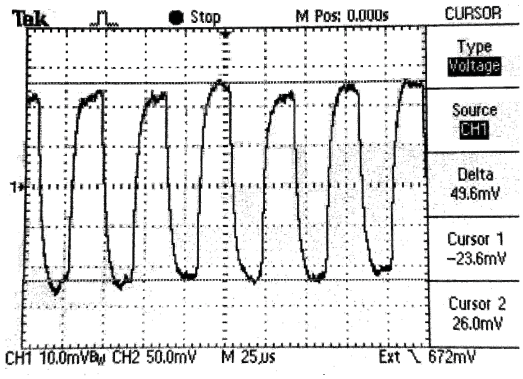

Fig. 6. Waveform at the output of preamplifier (f_{RF}=280.6 GHz, f_{chop}=25 kHz, distance=2cm)

Fig. 6 is the waveform at the preamplifier output with each diode cell biased at 50μA. The peak-to-peak output voltage is ~50mV. The detector output is also measured with the lock-in amplifier at varying source frequencies (Fig. 7). The detector is most sensitive at 280.6 GHz, and the other peaks and valleys are due to the standing wave between the horn antenna and the detector. The RMS output of lock-in amplifier measures the band-pass filtered modulated input signal. If the chopping function implements 50-% square wave, then a Fourier analysis indicates that the ideal reading from the lock-in amplifier V_{rms} should be $\pi/\sqrt{2}$ ≈2.2 times smaller than the peak-to-peak value of the square wave captured by the oscilloscope [11].

Using the Friis transmission equation and the simulated detector antenna directivity, the incident power received by each detector cell is ~0.8μW. Therefore, the voltage responsivity of detector is ~21kV/W. After de-embedding the preamplifier gain, the responsivity of each detector cell is ~70V/W.

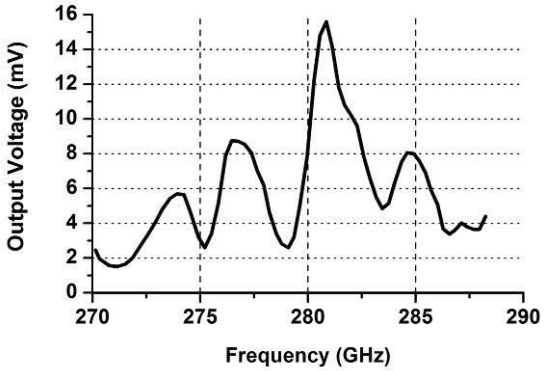

Fig. 7. Detector output (the RMS value) at varying source frequencies measured by the lock-in amplifier.

Responsivity at varying diode bias current is also measured and plotted in Fig. 8. For comparison, the simulated responsivity is also provided. Both curves give the same optimum bias point for the peak responsivity. The reasons for the difference between the measurements and simulations are being investigated.

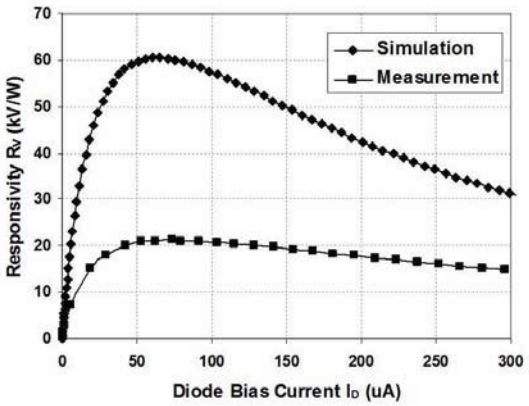

Fig. 8. Detector responsivity versus diode bias current

To determine the noise equivalent power (NEP) of detector, the output noise of diode and preamplifier is amplified by an external low-noise (800pV/$\sqrt{\text{Hz}}$ input referred noise) voltage amplifier (EG&G Model 5184), and then measured by a dynamic signal analyzer (HP 3561a). The noise of detector is plotted in Fig. 9. The noise level difference between two diodes in shunt and four in shunt is 3dB, which is consistent to Eq. (4). At 25 kHz, the output noise voltage of four detector cells is 12.5nV/$\sqrt{\text{Hz}}$. Each detector cell generates ~25nV/$\sqrt{\text{Hz}}$ noise. Based on calculated shot noise of diode (~3nV/$\sqrt{\text{Hz}}$) [10], the 1/f noise corner frequency is expected to be around 2 MHz.

Using the measured responsivity with these noise data, the NEP of each cell at 25-kHz modulation frequency is ~360pW/$\sqrt{\text{Hz}}$. The ratio between the preamplifier output noise and the diode output noise is close to the 50-dB preamplifier

gain, which indicates that the noise added by the preamplifier is not significant at 25 kHz. Presently, the modulation frequency is limited by the lock-in amplifier. By increasing the modulation frequency to ~4 MHz, the NEP can be reduced to ~40pW/$\sqrt{\text{Hz}}$. This indicates that Schottky diode detectors may be able to outperform the MOS transistor-based detectors.

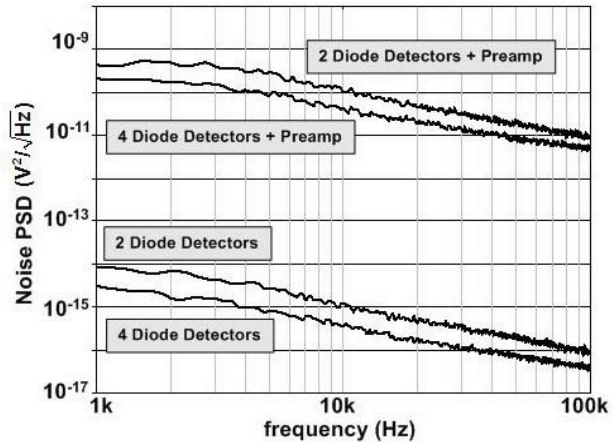

Fig. 9. Measured output noise voltage power spectrum of the detector.

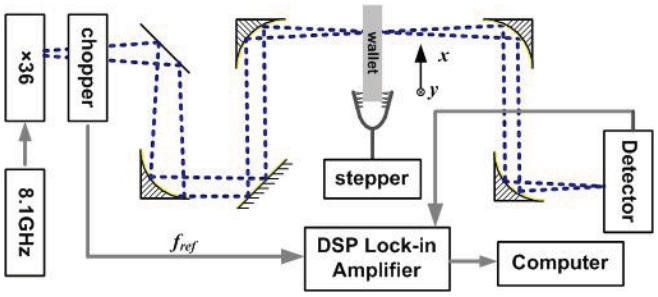

Fig. 10. Block diagram of the THz imaging system.

Lastly, the 280-GHz Schottky diode detector was integrated into a 2-D focal-plane image scanner shown in Fig. 10. The transmitted power from the source is ~ 4 mW. Since the scanner source frequency is 292 GHz, the detector was operated away from its optimum. Despite this, the detector could be used to form images. Fig. 11 shows one of the images: a coin and a blade concealed inside a leather wallet. Sampling of each pixel takes 40 ms and around 20 minutes to scan the entire image. This demonstration indicates that the CMOS-compatible Schottky-barrier diode can be used to fabricate an array for millimeter-wave and sub-millimeter wave imaging.

V. CONCLUSIONS

This paper has shown that CMOS-compatible Schottky barrier diodes can be used to detect millimeter-wave and THz radiation. At 25-kHz modulation frequency, it provides comparable NEP as that for NMOS based detectors [7], [8]. At 4-MHz modulation frequency, NEP is expected to be reduced to ~40pW/$\sqrt{\text{Hz}}$ for the diode detector, which will be 10X lower than that for the NMOS based detectors [7], [8]. Given that the cut-off frequency of PGS SBD's is ~2 THz, detectors operating at frequencies higher than 1 THz should be possible in the 130-nm CMOS process.

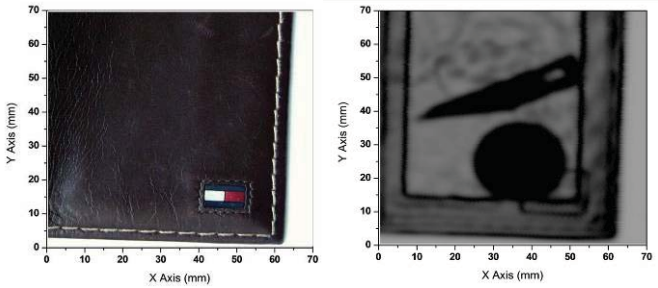

Fig. 11. Image of a leather wallet formed using the diode detector at 292 GHz shows the coin and blade hidden inside.

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