2D-FDTD Electromagnetic Simulation of an Ultracompact All-Optical Logic Gate Based on 2D Photonic Crystal for Ultrafast Applications

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Abstract

In this paper, the concept of photonic crystals (PhCs) is fundamental to the design and simulation of an all-optical device. The proposed logic device is composed of two-dimensional (2D) photonic crystal waveguides with a central photonic crystal ring resonator (PCRR). The new all-optical NAND logic gate is composed of two linear waveguides coupled to each other through a single compact PCRR. The plane wave expansion (PWE) and finite-difference time-domain (FDTD) methods are used to analyze the behavior of the structure that is implemented on the operational wavelength of 1700 nm on an air wafer of only 12 μm × 12 μm. The simulation results show that the proposed all-optical NAND gate is a strong candidate to be used for ultrafast photonic integrated circuits (PICs) being highly advantageous with high transmitting power, simple design and without use of the optical amplifiers and nonlinear materials.

1 Introduction

In today's world, with rapidly growing technologies, advancements are needed in every field of research, especially in electronics and communications devices. In this way, we are interested in the context of this advancement form electronics to world of optics.

The photonic crystal devices are periodic nanostructures of alternating layers of certain materials, with different refractive indices, which enable the manipulation of various forms of electromagnetic radiation.

The waveguides of a photonic crystal can have very sharp curves, with low losses in the structure, contributing to an increase in the density of integration of components, by several orders of magnitude.

Photonic crystals offer a wide range of applications in ultra-compact all-optical integrated circuits with a high reduction in energy consumption. Currently, several logic gates based on photonic crystal platforms have been demonstrated (Lee et al. 2008).

In order to recognize the performance of all-optical logic gates, different structures have also been proposed, such as, Multimode Interference, MZI (Mach-Zhender Interferometer), SOA (Semiconductor Optical Amplifier), among others.

Initially, all-optical logic gates based on SOA properties were reported (Zhou et al. 2005; Houbavlis et al. 1999; Kim et al. 2006). However, there are some limitations to these methods, among which we can mention the high input power with a low power transmission, complex and expensive projects, the latency time, in addition to the speed and size of the structures, causing that are less used, making on chip integration difficult (Saranya and Anbazhagan 2020).

The study of photonic crystals allowed the design of certain structures with interesting optical properties, including the specific frequencies range denoted by photonic band gap (PBG) and that can be calculated using the plane wave expansion (PWE) method. The light in this range of frequencies does not propagate through this structure. (Leung and Liu 1990; Meade et al. 1992; Sakoda 2004). In this way, the electromagnetic waves incident with frequencies located in this range are reflected by the crystal, and therefore the light flux can be controlled (Joannopoulos et al. 2008).

Lately, many researchers have become interested in the design of optical logic gates from photonic crystals, as it is one of the most important optical media to form optical processors and optical communications systems. Some of these authors designed logic gates based on resonators, whether linear or non-linear, where they studied the advantages and disadvantages in each method used.

In this direction, some works have already been developed, among which, refer to that of Chunrong Tang et al. (2013), where several completely optical logic gates of a 2-D photonic crystal were designed, based on multimodal interference (MMI). Some logic gates were obtained: OR, NAND, XNOR and XOR. These structures are analyzed and simulated using the FDTD and PWE methods. The contrast ratio for OR and NAND logic gates is 13dB, for XNOR it was 17dB and for XOR, about 21dB in C-Band (C-Band / Conventional Band) with the spectral region from 1530 nm to 1565 nm. These logic gates are potential candidates for constituting photonic integrated circuits (PICs), which will be used in all-optical signal processing, all-optical networks and in photonic computing.

In another study, Yuanliang Zhang et al. (2007), demonstrated a device used to obtain optical logic gates. The working principle is shown through simulations using the FDTD method. This device is applicable for the frequency range of 0.188-0.199 (a/λ). The contrast ratio obtained within the frequency range s is 17 dB with the maximum being about 21dB. Due to its simple structure and its clear operating principle, this structure can be used for future applications in PICs.

In Junjie Bao et al. (2014), the authors investigated a new approach for the design of all-optical logic gates based on 2D photonic crystals in a square lattice of silicon rods (Si) on silica (SiO_2). It consists of two photonic crystal resonator rings (PCRRs) and cross-shaped waveguides without the use of optical amplifiers and materials nonlinear. The layout of the optical logic gate is simulated and analyzed by the FDTD and PWE methods. The results of the numerical simulation demonstrate that the structure acts as a NOR and NAND logic gate. The logical levels, high ‘1’ and low ‘0’ are defined. Since this structure is composed of a linear material, it presents low power consumption compared to structures composed of non-linear materials. It is observed that the construction of new structures causes PCRRs to have new applications in ultra-compact PICs.

Goudarzi et al. (2016) proposed an all-optical structure based on two types of defect, the point defect and the line defect. The defects were created in a square lattice formed of silicon dielectric rods in contrast to air. The device design features two input ports with two output ports. The operating frequency range of the device is from 0 to 0.45 (a/λ), however it was adjusted to 0.419 for low dispersion condition, and the structure is implemented with an operational lambda equal to 1.55 μm. Regarding the performance presented after the simulations, the maximum contrast ratio reached was about 6.767 dB. According to the results, the authors reported that the device can act as an XOR logic gate and an OR logic gate.

More recently, Saranya and Anbazhagan (2020) proposed a trifurcation structure of logic gates based on two-dimensional photonic crystals composed of a square lattice of air holes in silicon. The plane wave expansion method (PWE) and the finite difference time domain method (FDTD) are used to analyze the behavior of the structure. The results obtained prove the functionality of OR, AND, NOR and NAND optical logic gates. Regarding the performance obtained by the device, specifically for AND, NAND and NOR gates, the contrast ratio was 6.15 dB, 5.79 dB and 2.97 dB, respectively. Furthermore, the bit rate and footprint were calculated for the simulated optical logic gates. The footprint for the proposed logic gate was around 424.7 μm. In order to improve the value of the contrast ratio, where certain logic functions imply a better output power, then some phase shifts were introduced in the launch field. Then, with a 180° phase shift, the contrast ratio obtained for the AND and OR logic gates, was 6.52 dB and 10.79 dB, respectively.

The previous works are some examples of studies that are characterized by the use of a numerical methodology in order to analyze the all-optical logic gates obtained for use in various applications in the scope of telecommunications.

The electromagnetic simulation has been performed through 2D finite-difference time-domain (FDTD) method (Taflove and Hagness 2005), which is used to simulate electromagnetic wave propagation in any kind of materials in the time domain. We present a new design of a very compact structure to be used as NAND logic gate, contributing to the density of component integration in optical communications systems.

Numerical simulation has been performed through 2D FDTD method (Johnson and Joannopoulos 2000; Yee 2004), which is used to simulate electromagnetic wave propagation in any kind of materials in the time domain.

2 Structure Design, Materials And Methods

In this paper, is presented a new design for obtaining the all-optical NAND logic gate based on photonic crystals. The schematic of this structure is shown in Fig. 1, and consists of a 19 × 19 square lattice, of silicon rods in 2D structure. The lattice constant, denoted by '*a*', is 0.5943 μm, which is a distance between the two consecutive rods, as shown in Fig. 2. The radius of rod is 0.2*a*, approximately 0.11886 μm. The relative permittivity of the cylindrical dielectric rods in the structure is ε_r = 11.56 which is equivalent to a 3.39 refractive index. A scatter rod is placed at the end of the input waveguide, shifted by a 0.707*a* with the same refractive index and radius, as shown in Fig. 2.

The structure of the proposed NAND gate is constructed using a non-linear PCRR inside, being incorporated into the structure by inserting some linear and non-linear defects for the formation of the PCRR. Point and line defects created in the structure are made with silicon (*Si*) dielectric rods, which are added or removed in the interior region of the structure, in the **XZ** plane. Two dielectric rods (*Si* rods) are added around the inner rods, configuring specific defects in the horizontal and vertical waveguides, respectively with radius $r_2 = 0.1a$ and $r_1 = 0.05$, responsible for switching the NAND logic gate, as shown in Fig. 2.

The silicon rod shown in the Fig. 1 and Fig. 2, whith of the radius 0.05 *μ*m, create a point defect that are responsible for the light confinement property. We propose a new structure for a all-optical switch composed of two waveguides (horizontal and vertical) and one central PCRR, as shown in the Fig. 1.

In addition, this structure consists of two input ports, (**A**, in green) and (**B**, in black), one reference signal port (**C**, in red) and one output port (**D**, in blue), in a square latice composed of silicon rods (*Si*) on an air wafer of only 12 *μ*m × 12 *μ*m, as shown in the Fig. 1. The wavelengths of the input signal and the signal at all ports in the structure are the same.

The structure is excited in port **C**, with control by port **A** and port **B**, and the output signal is verify in port **D**. Specifically, there is always a reference signal switched on the upper, in port **C** of the vertical waveguide. When no optical signal is applied on ports **A** and **B**, is verify output signal on port **D**. When an optical signal is applied to port **B** (and no signal is applied to port **A**), is verify output signal on port **D**. On the contrary, when an optical signal is applied to port **A** (and no signal is applied to port **B**), is verify output signal on port **D**. Now, when optical signal is applied on ports **A** and **B**, no output signal is verify in port **D** due to the coupling of PCRR in structure.

3 Results And Discussion

In Fig. 3. we have the representation of the band diagram of the proposed all-optical structure, based in two-dimensional photonic crystals. The band diagram was calculated by the plane wave expansion (PWE) method. The PBG for transverse electric (TE) polarization appears for the frequency range given by $0.2654 \leq a / \lambda \leq 0.3897$, corresponding to the wavelength range $1525 \leq \lambda$ [nm] ≤ 2239, with the propagation modes in the first Brillouin zone.

The numerical simulations of the propagation of electromagnetic waves in PhCs is characterized using Maxwell's equations. The PWE method is used to calculate the PBG and propagation modes of the PhC structure while that the 2D-FDTD method is used to calculate the spectrum of the power transmission and field distribution that is based on numerical solutions of Maxwell's equations.

The FDTD method is based on Yee's algorithm, to study the 2D-PhCs, because the computational time and memory requirements are reduced (Kumar et al. 2004; Robinson and Nakkeeran 2010).

It is assumed that the material is linear, isotropic, periodic with lattice vector and lossless. Therefore, the Maxwell's equations (Taflove and Hagness 2005; Yee 2004) are given by

$$\vec{\nabla} \times \vec{E} = -\mu \frac{\partial \vec{H}}{\partial t}$$

$$\vec{\nabla} \times \vec{H} = \varepsilon \frac{\partial \vec{E}}{\partial t}$$

$$\vec{\nabla} \cdot \vec{E} = \vec{\nabla} \cdot \vec{H} = 0$$

1

The normalized transmission spectra on port **D**, which is shown in Fig. 4, are obtained by performing the Fourier transform of the fields that are calculated by finite-difference time-domain method. The Maxwell's equations (Taflove and Hagness 2005; Yee 2004) for the 2D transverse electric (TE) mode FDTD used in this work is

$$\frac{\partial H_x}{\partial t} = \frac{1}{\mu_0} \frac{\partial E_y}{\partial z}$$

$$\frac{\partial H_z}{\partial t} = -\frac{1}{\mu_0} \frac{\partial E_y}{\partial x}$$

$$\frac{\partial E_y}{\partial t} = \frac{1}{\varepsilon} \left(\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} \right)$$

2

where$\varepsilon(r) = \varepsilon_0 \varepsilon_r$, $\mu(r)$ and $\sigma(r)$ are respectively, the permittivity, the permeability and the conductivity of the material, and all are in the function of position.

We have two types of logic states, referring to high transmission power ('ON' state) and low transmission power ('OFF' state).

In order to analyze the consequent performance of the implementation of NAND logic gate, a relation between these two power levels was calculated. This relation is defined as the ratio between the average power in the ON state and the average power in the OFF state, where P_{ON} is the power level of logic '1' and P_{OFF} is the power level of logic '0' (Areed et al. 2017; Shaik and Nakkeeran 2000).

This transmission factor is known as contrast ratio (CR), and the performance of the all-optical NAND logic gate is evaluated numerically taking into account this parameter, that is given by

$$\mathrm{CR} = 10 \cdot \log \left(\frac{P_{ON}}{P_{OFF}} \right)$$

3

In this work, the logic level high ‘1’ and level low ‘0’ are defined. The switching property between logic ‘1’ and logic ‘0’ of gate is achieved by the light confinement property of PhCs silicon rods. In logic ‘1’ state there should be maximum power transmitted as compared to the power transmitted in case of logic ‘0’.

The logic function of NAND gate is verified by two optical switches operation. In this simulation, the structure is surrounded by perfectly matched layer (PML), in all the sides. The perfectly matched layers are used as the absorbing boundary condition at the edges of the computational zone. The structure is excited with a Gaussian light source at the normalized resonant frequency of 0.3495*c*/*a*, whose corresponding wavelength is 1700 nm, where *c* is the speed of light in vacuum.

Reviewing the Fig. 4, we have: 4 - (a), when port **A** and port **B** be state ‘OFF’ (or bit 0), and port **C** is applied the pumping optical source, we can see that the optical signal can reach the port **D**, hence, the electric field propagation results show the switching capability. In Fig. 4 - (b), there is an optical signal output at port **D** (or bit 1) due the operation of central PCRR, where the optical channel in port **A** is turned ‘OFF’, in the state ‘OFF’ (or bit 0), and the optical channel in port **B** is on state ‘ON’ (or bit 1), while that in port **C** is applied the pumping optical source. In Fig. 4 - (c), there is also high power signal in port **D** when the **B** and **A** ports invert the status. So, in Fig. 4 - (d), when the port **A** and port **B** being in state ‘ON’ (or bit 1), and the optical pumping source on port **C** is continue turned in state ‘ON’, then due the operation of the single PCRR, is not verified signal in port **D**, or level very low of power signal (or bit 0).

The operation results for the proposed all-optical NAND logic gate are summarized in Table 1.

In this NAND logic gate, a high contrast ratio of 18.4509 dB was obtained, without optical amplifiers and nonlinear materials. The power in the ‘ON’ state (P_{ON}) is equal to 1.190 and the power to the ‘OFF’ state (P_{OFF}) is equal to 0.017. The Fig. 5 shows the symbol of NAND logic gate.

Table 1 Truth table of all-optical NAND logic gate.

Control signal **C**	Input signal **A**	Input signal **B**	Output signal **D**
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

4 Conclusion

The electromagnetic simulation results using the FDTD method show that the proposed all-optical NAND logic gate is a strong candidate to be used for ultrafast optical digital circuits being highly advantageous with high transmitting power and simple design. Furthermore, the results are highly beneficial shown that PCRR plays an important role in the switching capacity of the optical NAND logic gate.

The structure of gate implemented is simulated on the wavelength of 1700 nm using FDTD method and its lattice constant is given by 0.5943 μm. Furthermore, in comparison with conventional PhC-based optical gates, the structure of proposed NAND gate has very small size, of about 12 μm × 12 μm and can work with low power consumption. Because of their small size, this logic gate is suitable for using in photonic integrated circuits (PICs).

These performance parameters allows that the simulated structure is promising for the applications in optical integration circuits, on ultrafast optical operations in digital processing systems, among others.

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Figures

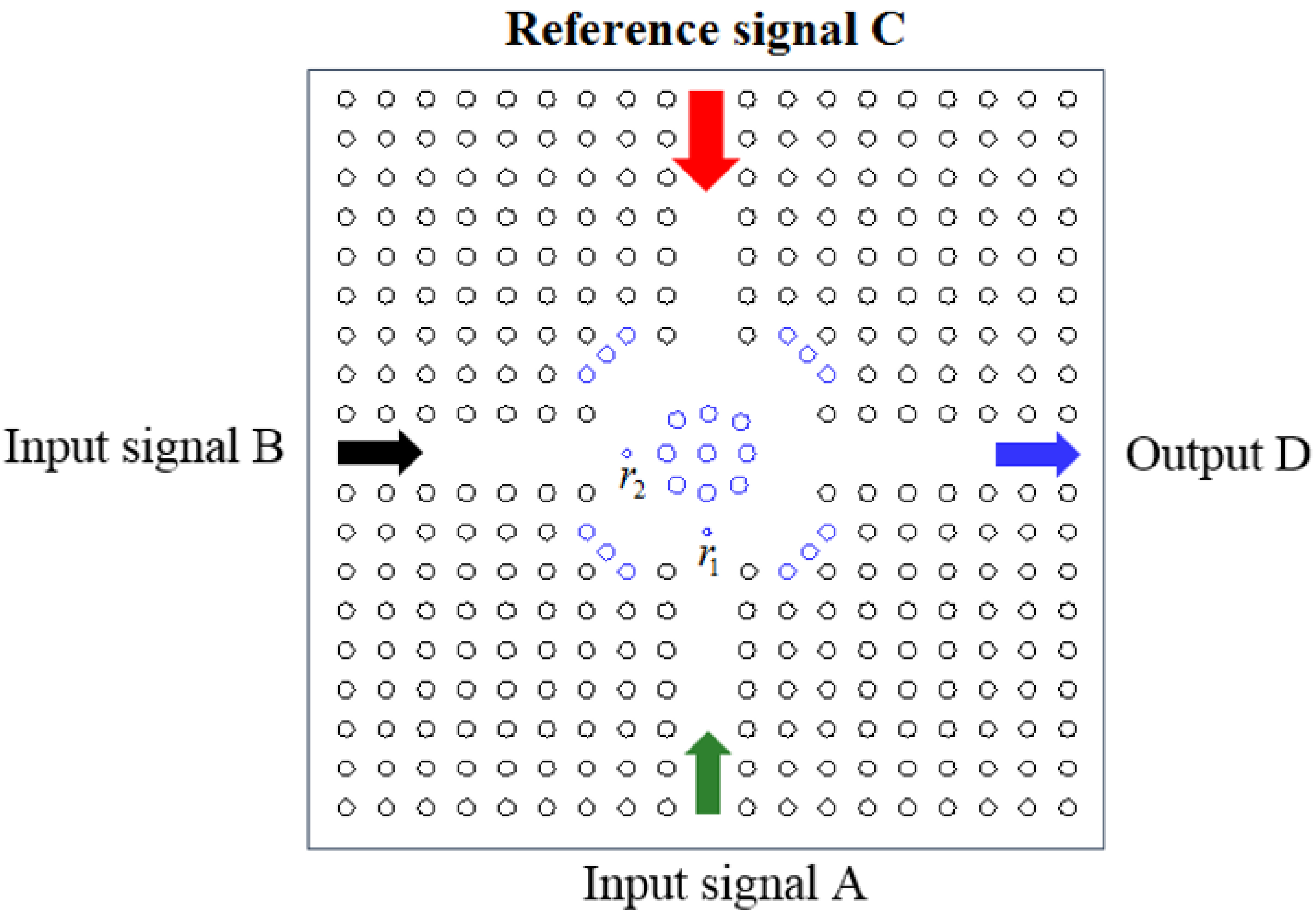

Figure 1

Simulation scheme of the square silicon structure of the all-optical NAND logic gate.

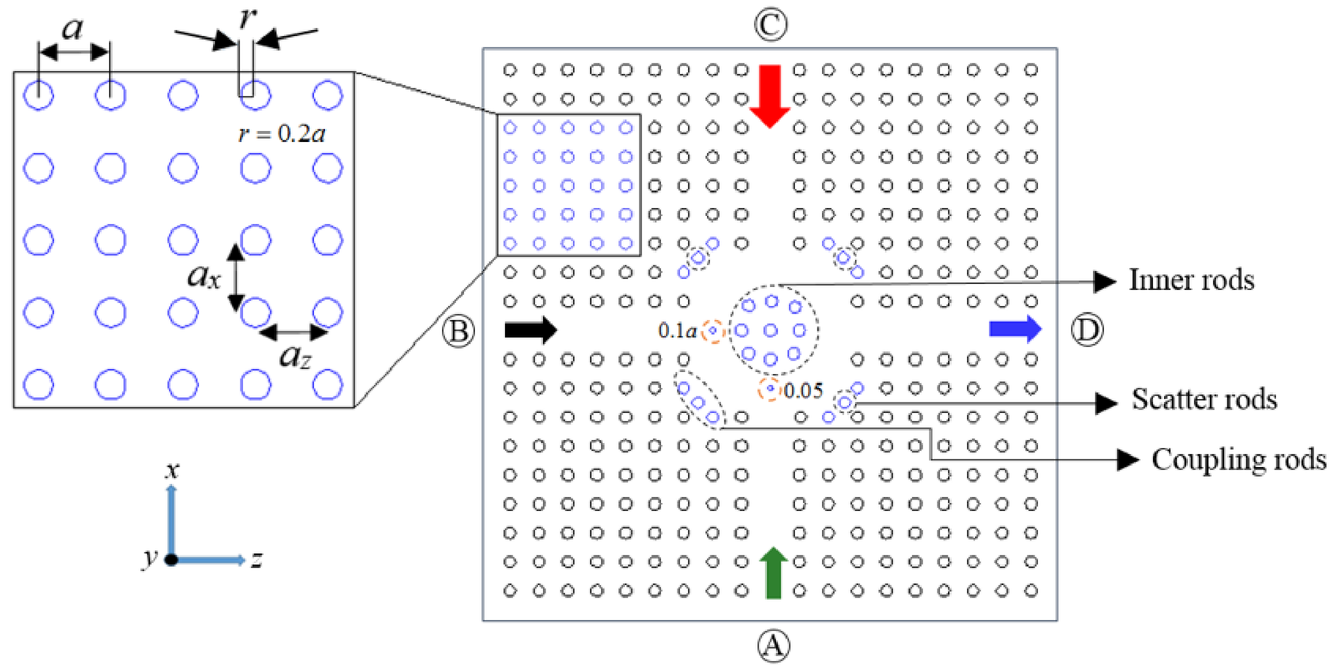

Figure 2

Schematic diagram of the proposed all-optical NAND logic gate device.

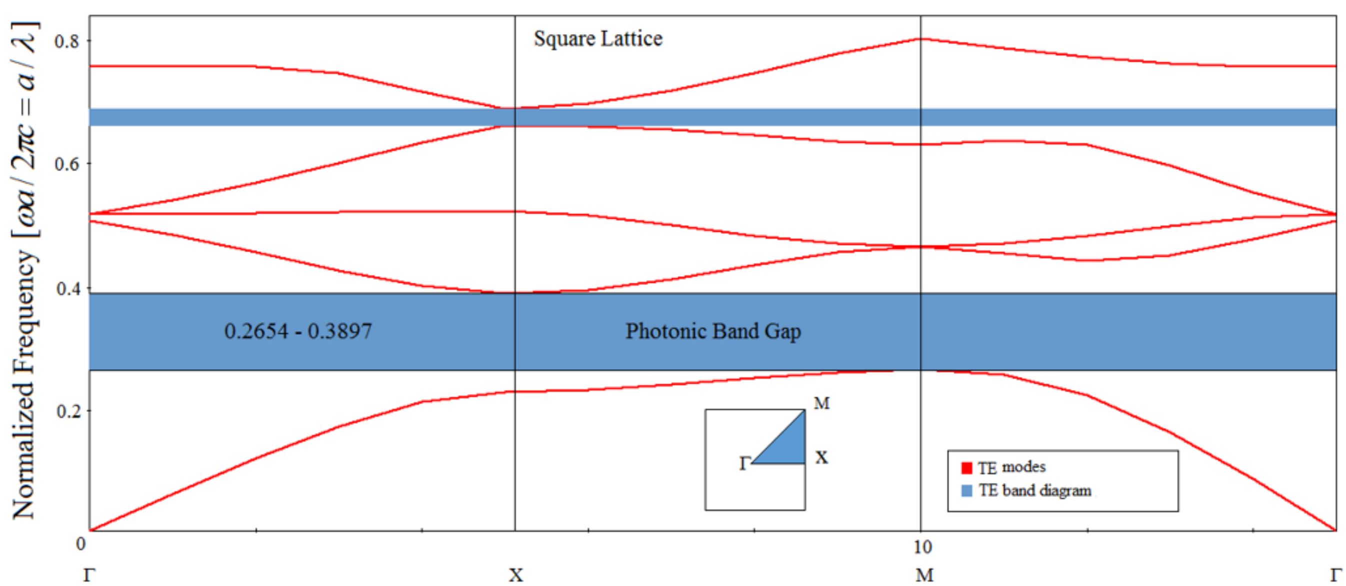

Figure 3

The band diagram of proposed all-optical structure.

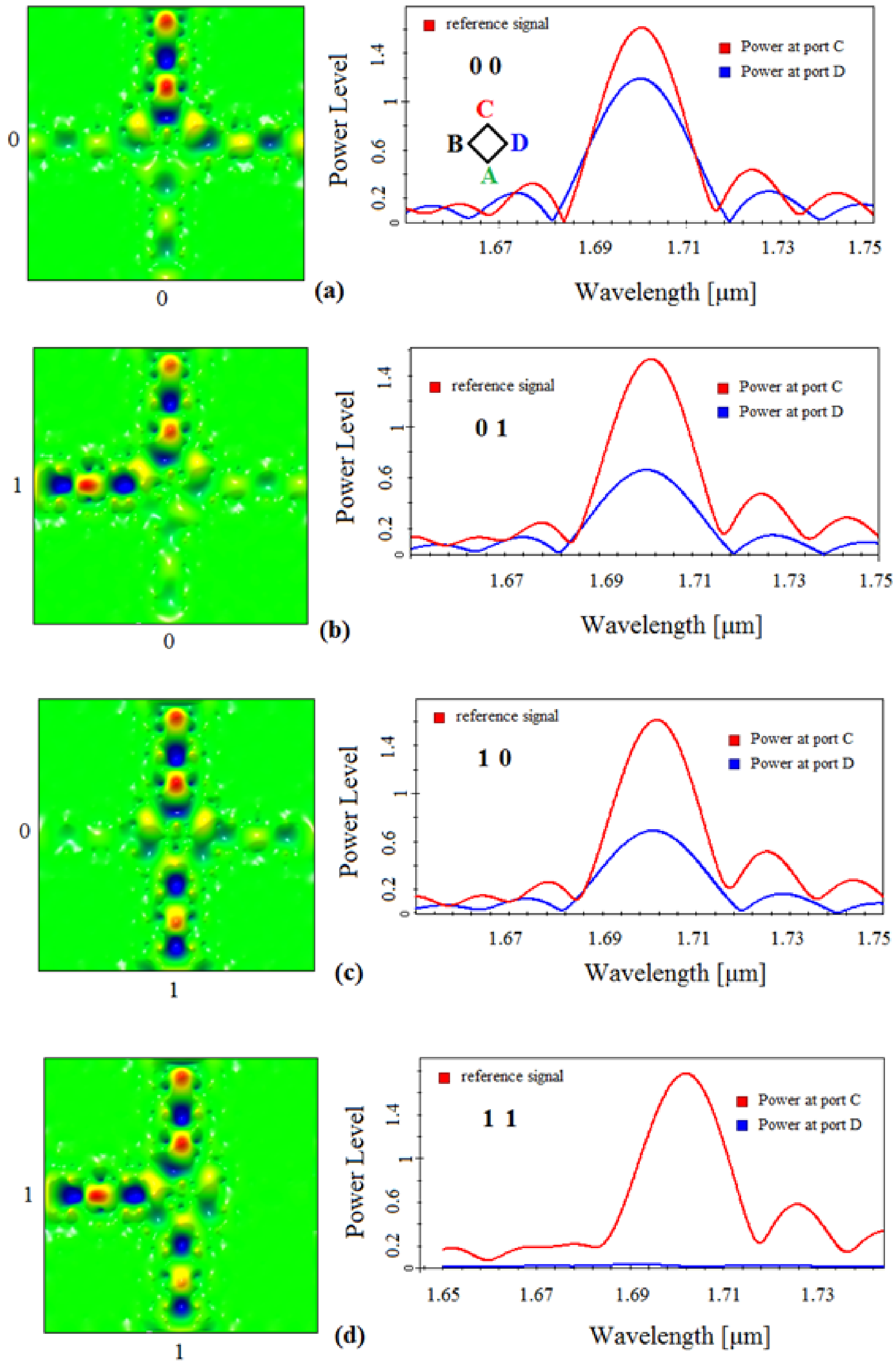

Figure 4

The electric field distribution of all-optical NAND logic gate and the power transmitted (W/m) in (a) 0 - 0; (b) 0 - 1; (c) 1 - 0, and (d) 1 - 1.

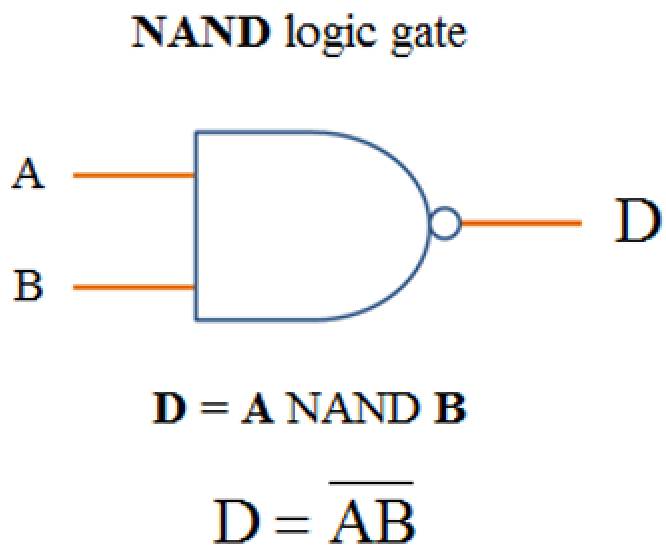

Figure 5

The symbol of NAND logic gate.