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2D MOSFET operation of a fully-depleted bulk MoS_2 at quasi-flatband back-gate

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In this paper, 2D MOSFET operation of a fully-depleted double-gate bulk MoS_2 is studied at a quasi-flatband of the back-gate for the first time. Several key device parameters such as equivalent oxide thickness (EOT), carrier concentration, flatband voltage, dielectric constant and carrier mobility were extracted from I-V and C-V characteristics and at room temperature. In a similar operation to the inversion-mode SOI MOSFETs in [1], the back-gate was used to keep a sheet of mobile charges on the flake back-side by its quasi-flatband operation at a fixed voltage (0 V). Afterward, the top-gate was used as the active gate to perform mobile charge accumulation or depletion in the channel. Fig. 1 shows the device architecture together with the high frequency R-C equivalent circuit model for this underlap gate architecture. Fig. 2 represents the top-view microscope picture of the fabricated MoS_2 bulk MOSFET with a flake thickness of 38 nm, measured by AFM. The fabrication steps include mechanical exfoliation of MoS_2 crystals on a 260 nm thick oxidized Si substrate, e-beam lithography to make S/D pads, 50 nm Ni by thermal evaporation and lift-off, gate patterning, high-k/metal-gate stack deposition (1 nm of SiO_x by thermal evaporation, 11 nm of ZrO_2 by ALD deposition at 105 °C, 30 nm of Ni by thermal evaporation) and lift-off. The measurements were done at room temperature using an Agilent B1500A Semiconductor Parameter Analyzer. Fig. 3 shows its I_d-V_g, reporting a subthreshold slope of 110 mV/dec. and I_{on}/I_{off} of ~1×10^5, both at V_{ds}=100 mV.

EOT, dielectric constant, flatband voltage: Fig. 4 depicts the C_g-V_g measurement between the top-gate and the source-drain electrodes (V_{ds}=0 V) at a high frequency regime (1 MHz). In strong accumulation, the EOT numeric value of the gate stack can be extracted from the maximum value of gate-channel capacitance, resulting an EOT value of 6.3 nm. In the partial depletion regime, between threshold and flatband, the gate-channel capacitance would vary by $1/C_{gc}^2=1/C_{ox}^2+2/(q.\varepsilon_{ch}.N_d).(V_{gs}-V_{fb})$ [2]. The flatband voltage can be extracted from the x-intercept of $1/C_{gc}^2-1/C_{max}^2$, reporting a flatband voltage of -0.45 V. The dielectric constant of the flake can be extracted from the difference in the gate-channel capacitance in strong accumulation and at the threshold voltage (-1.1 V, estimated from the linear onset of I_d-V_g in Fig. 3), reporting a numeric value of 7.8. This is almost in the range of the reported experimental dielectric constant numeric values in [3].

Carrier concentration: The carrier concentration can be extracted from the slope of $1/C_{gc}^2 - 1/C_{max}^2$ in the linear region between threshold and flatband, reporting a value of 2.1×10^{17} cm^{-3}. Note that this method can be applied to the devices with a flake thickness higher than the Debye length (~7.2 nm at this carrier concentration or doping regime).

Series resistance: The series resistance, similar to an inversion-mode MOSFET in [4], can be extracted from the y-intercept of $R_{tot}=V_{ds}/I_d$ vs. $1/(V_{gs}-V_{fb})$ in linear accumulation regime ($V_{ds}<V_{gs}-V_{fb}$), see Fig. 4, assuming accumulation as the dominant conduction mechanism in comparison to bulk conduction. This assumption is justified considering the channel accumulation conductance ($\mu.C_{ox}.W/L.(V_{gs}-V_{fb})$) of three times higher than the bulk conductance at flatband ($q.\mu.N_d.t.W/L$). An almost similar mobility assumption for bulk and accumulation conduction results a bias range of $V_{gs}-V_{fb}>0.60$ V. A series resistance of 434 kΩ is extracted in Fig. 4, while this fairy high value is due to the used underlap gate design to minimize the parasitic gate-source and drain capacitances. Note that Benzyl Viologen (BV) [5] or SiN_x [6] doping can be performed in the S/D extensions to suppress such resistances as well as minimize their gate-bias-dependencies especially above flatband and for shorter lengths [7].

Carrier mobility: The effective carrier mobility can be extracted using the split C-V method, similar to a junctionless/accumulation-mode device in [8]-[9], covering a wide gate voltage range from threshold to strong accumulation ($\mu_{eff}=I_d.L/(W.Q_n.V_{ds})$; $Q_n=\int_{off}^{V_g} C_{gc}.dV_g$). Q_n is the normalized mobile negative charges in the channel per unit area. Fig. 5 shows the numeric effective mobility values after the series resistance correction, reporting a maximum effective electron mobility value of 48 cm^2/V.s. For comparison, the effective mobility is also extracted from I-V characteristics, after a series resistance correction and from the g_m values in linear accumulation regime, $\mu_{eff}=g_m/(C_{ox}.W/L.V_{ds})$, reporting a maximum numeric value of 26 cm^2/V.s. The slight effective mobility underestimation using only I-V characteristics can be due to neglecting the bias-dependency of the gate-channel capacitance in strong accumulation regime.

Conclusion and further works: In this work, we extracted several device parameters in a double-gate bulk MoS_2 MOSFET using C-V and I-V characteristics. Such device extraction methodologies were done assuming a typical linear operation of an accumulation-mode MOSFET from depletion to accumulation. This parameter extraction platform can be used to investigate the possible bias-dependency of key material parameters e.g. dielectric constant and bandgap [10], in a high normal electric field considering a back-gate operation. This includes incorporation of photoluminescence measurement on direct bandgap 2D devices, monolayer e.g. MoS_2 and bulk e.g. ReS_2 [11] as well

as additional measurement methods e.g. Hall for comparison of e.g. mobility and carrier concentration values.
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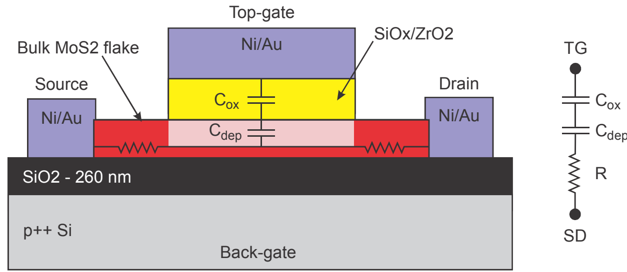

Fig. 1: The device architecture, showing a top-gate operation between threshold and flatband voltage (left) and a high frequency model of the device (right).

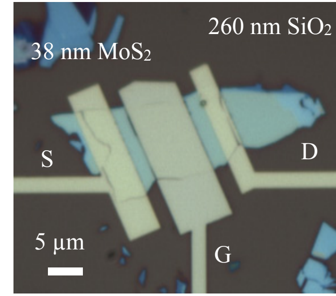

Fig. 2: The top-view microscope picture of the measured underlap top-gate MoS_2 MOSFET.

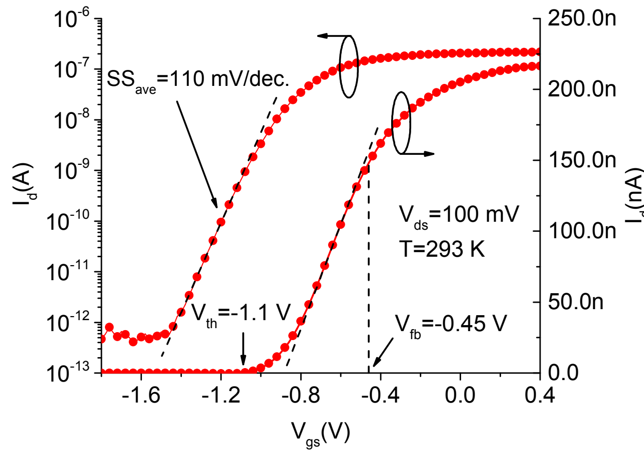

Fig. 3: I_d-V_g characteristics at V_{ds}=100 mV and V_{bg}=0 V.

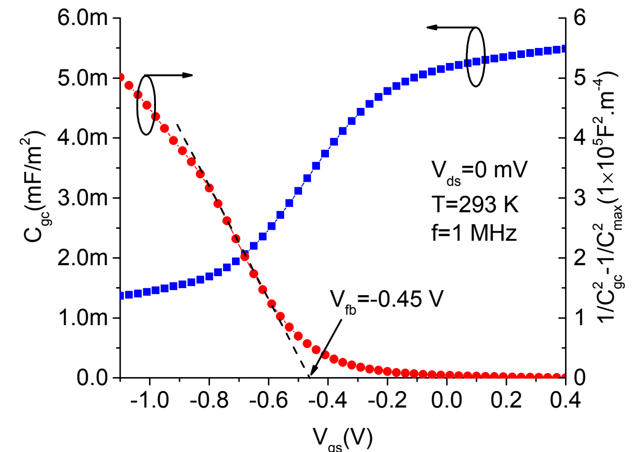

Fig. 4: C_g-V_g characteristics at 1 MHz and V_{ds}=0 V.

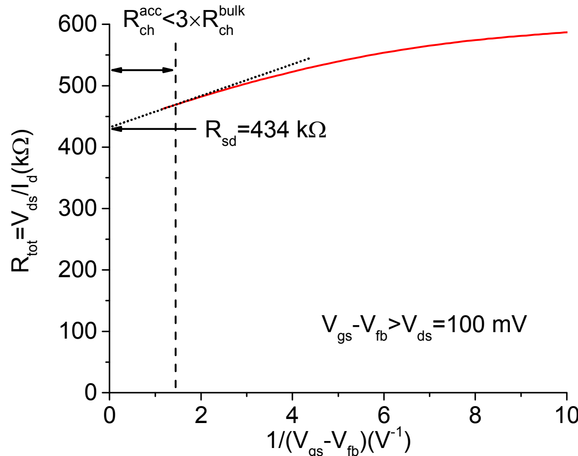

Fig. 5: Extraction of series resistance in linear accumulation regime from the total source-drain resistance vs. $1/(V_{gs}-V_{fb})$.

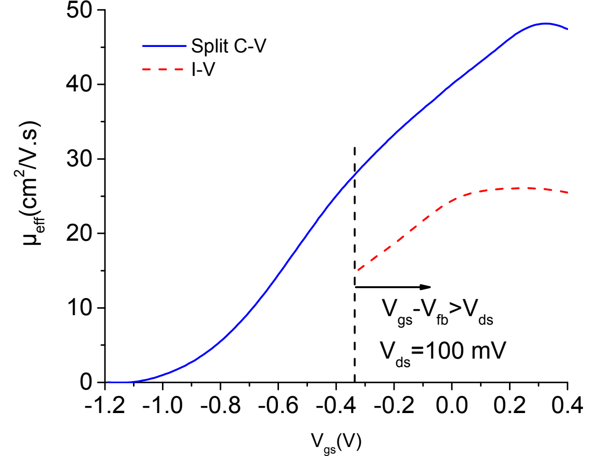

Fig. 6: Effective mobility extraction using split-CV and I-V, after series resistance correction.