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***Abstract*—Design For Test (DFT) of 3D stacked integrated circuits based on Through Silicon Vias (TSVs) is one of the hot topics in the field of test of integrated circuits. This is due to the hard test accessibility (especially for upper dies) and to the high complexity where each die can embed hundreds of IPs. In this paper we propose a DFT architecture based on IEEE P1687 to enable the test of 3D stacked ICs. The proposed test architecture allows the test at all 3D fabrication levels: pre-, mid-, and post-bond levels. We present a test pattern retargeting flow using IEEE P1687 languages ICL (Instrument Connectivity Language) and PDL (Procedural Description Language), which allows easy retargeting from 2D (die-level) to 3D (stack-level). Compared to IEEE 1149.1 based 3D test architecture, our proposed 3D test architecture is more flexible and enhances test concurrency without an additional area cost.**

Key words: 3D IC, DFT, pre-bond test, post-bond test, JTAG, IEEE 1149.1, IJTAG, IEEE P1687, ICL, PDL, test pattern retargeting

I. INTRODUCTION

The stacking process of integrated circuits using TSVs (Through Silicon Vias) is a promising technology that keeps the development of the integration more than Moore's law, where TSVs enable the tight integration of various dies in a 3D fashion. 3D stacking will allow a wide range of new applications thanks to smaller form factors, heterogeneous stacking (digital, memory, RF, MEMS), and interposers for multi-chip connection, which become similar to silicon boards. The first upcoming 3D applications are mainly the WideIO DRAM 3D memory interface for high throughput and low power memory-on-logic stacking [1].

Moreover, 3D Integrated Circuits (3D-ICs) present new test challenges related to the new fabrication process. Indeed the test must be performed at pre-, mid-, and post- bond levels to guarantee the production quality. Pre-bond test targets the individual dies at wafer level, by testing not only classical logic (digital logic, IOs, RAM, etc.) but also non bonded TSVs. Mid-bond test targets the test of partially assembled 3D stacks, whereas post-bond test targets the final circuit. It is generally admitted that a 3D test flow [2] should involve test procedures at all stacking levels of the 3D components. Many DFT architectures for testing 3D integrated circuits have been proposed in the past. The first papers treated pre-bond test of 3D processors using scan islands and the so-called Layer Test Controller (LTC) [3], scan chain optimization approaches [4], and other test issues like test cost optimization [5]. More recent works propose die level wrappers based either on IEEE 1500 [6] or IEEE 1149.1 [7] test standards that allow 3D test at all bonding levels. These test architectures have mainly three features: the use of dedicated probe pads on non-bottom dies for pre-bond testing, the usage of "TestElevators" to drive test signals up and down during post-bond test, and the use of a hierarchical WIR (Wrapper Instruction Register) chain to configure test interconnects. These features satisfy 3D circuits testing requirements in case of a homogenous 3D-ICs where all dies have an IEEE 1149.1 (or IEEE 1500) interface. We note that our proposal should be in line with the on-going 3D test access standard: the IEEE P1838 [8].

For better industrialization of 3D technologies, it is important to address the issue of the so called test pattern retargeting, which consists in 3D context on easy regeneration of test patterns from die level for pre-bond test to stack level for post-bond/final test. Such issue has been discussed in [9] for 2D integrated systems only. Recent test standards such as IEEE P1687 [10] and IEEE 1149.1-2013 [11] propose DFT architectures and dedicated languages allowing test pattern retargeting. There are no published works dealing with the application of these standards for 3D architectures while both of them can be adopted to perform test pattern retargeting. IEEE P1687 has a main advantage which is the use of a high level language ICL which allows better retargeting.

In this paper we present a 3D Design-For-Testability (DFT) architectures based on IEEE P1687 (IJTAG) where DFT is inserted using a commercial EDA tool using high level Instrument Connectivity Language (ICL) and Procedural Description Language (PDL). We show benefits of IJTAG over the classical JTAG in a 3D context, and give an example of test pattern retargeting from 2D to 3D.
The paper is organized as follows: In section II we give background on IEEE P1687 standard, which is the basis of the two proposed generic 3D DFT architectures based on IEEE P1687 presented in section III. Section IV presents benefits of IJTAG over JTAG for 3D-ICs. In section V we present a 3D DFT test flow using ICL and PDL and corresponding examples of test pattern retargeting for the two proposed architectures. Finally in section VI, we give conclusions and an outlook to future work.

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II. IEEE P1687 BACKGROUND

In this section we give some background on the IEEE P1687 standard describing the main features of IJTAG and the additional Gateway specific features that will be used for the proposed 3D DFT architectures in section III.

A. *IEEE P1687 Main Features*

The main purpose of the IEEE P1687 standard, also called IJTAG, is to develop a methodology for the access to embedded test and debug features. The Test Access Port (TAP) is mostly implemented as the one of the IEEE 1149.1, even if the standard does not mandate it [10]. This means that IEEE P1687 uses the same I/O interface (TRST*, TCK, TMS, TDI, and TDO) and structure logic (Instruction Register and associated decoder, TAP Controller, Data Registers) of the JTAG standard. Additional functions are added to enable the access to embedded DFT instruments [10]. An example of IEEE P1687 architecture is shown in Figure1, where SIBs (Segment Insertion Bits) and TDRs (Test Data Registers) are added to dynamically control the instruments. An instrument can be any device with a shift register (TDR) that can be included in the JTAG scan-path (e.g. sensors, BIST circuitry, etc). SIBs require to be configured either to open the path to the TDR or to close it. The configuration is done in 2 steps:

- The first step is to select an instruction allowing the selection of SIBs on the path between TDI and TDO, by shifting its corresponding op-code in the shift-IR state of the JTAG finite state machine [12].
- The second step consists in configuring SIBs to be opened or closed, by shifting the configuration sequence in the shift-DR state [10,12,13]

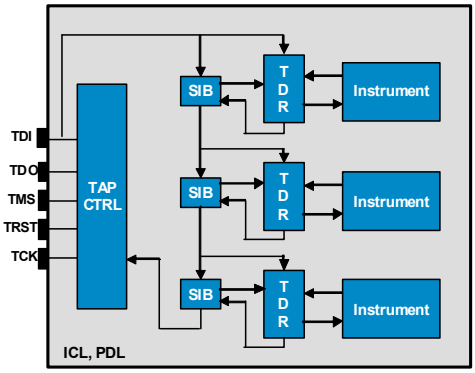

Figure 1. IEEE P1687 architecture definition

In addition to the DFT hardware, the IEEE P1687 standard proposal introduces two high level languages: ICL and PDL for portability of test patterns from one level to another; this is called test pattern *retargeting*. ICL is used to define the instrument interface and connection between instruments while PDL is used to define the syntax and semantics of operations. It is first written at instrument IOs level operations, and then an EDA tool can be used to translate these operations from the instruments up to the system top level through hierarchical logic described with the ICL. The standard ensures that a PDL description of an instrument can be used without modification even after embedding this instrument inside a design; it is the process of retargeting that translates this PDL sequence from the instrument level up to the top level of the system [14].

B. *IEEE P1687 Gateway Optional Feature*

A DFT proposal of an IEEE P1687 circuitry is to build upon JTAG logic and to use TAP controller to manage test sequencing. Details of the test logic architecture that will be considered in the remainder of the paper are shown in Figure 2 where the IEEE P1687 specific register is called Gateway register (GW). This register is added between TDI and TDO, and is selected when its associated instruction is loaded into the instruction register.

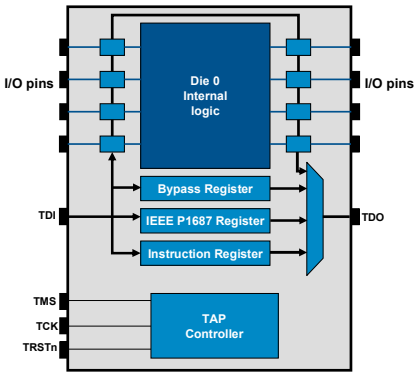

Figure 2. IEEE P1687 hardware architecture

The IEEE P1687 register GW is composed of many SIBs that are associated to TDRs. An example of such a register where SIBs are connected in series is shown in Figure 3.

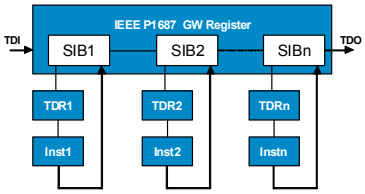

Figure 3. IEEE P1687 register composition

When the IEEE P1687 instruction is updated in the instruction register, a SIB configuration is required: to be either opened or closed. This is done at the shiftDR state of the IEEE 1149.1 finite state machine. An example of a SIB element is shown Figure 4.

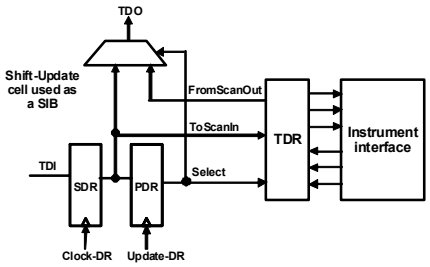

Figure 4. Example of a Segment Insertion Bit cell

If a logic '1' is updated into the SIB then the path to its associated instrument will be opened: *Select* signal enabled and the multiplexer is configured to select *FromScanOut* of the instrument. Otherwise the path is closed: *Select* signal is not enabled and the multiplexer selects the output of the *SDR* (Serial Data Register).

III. 3D DFT Architectures Based On IEEE P1687

The 3D DFT architecture heavily depends on the specifications of the 3D-IC including the number of stacked dies, the nature of the interposer if any: passive or active, and the test infrastructure of each die. We distinguish 2 types of IEEE P1687-based 3D test architectures in this paper:

- Uniform test architecture: a 3D-IC with all dies embedding a JTAG test interface.
- Heterogeneous test architecture: 3D-IC where dies relies on heterogeneous test interfaces.

A. *Uniform 3D DFT architecture*

The first type of 3D DFT deals with regular structures of 3D circuits as in [6,7]. The test architecture uses the new IEEE P1687 instead of IEEE 1149.1 as test standard in each die (see fig.5). Multiplexing logic between test pads and test TSVs is used for switching test paths sinks and sources after stacking. For instance, the TDI pad on the top die is used before bonding this tier on the stack, while test data are transported to this die from the die below after bonding.

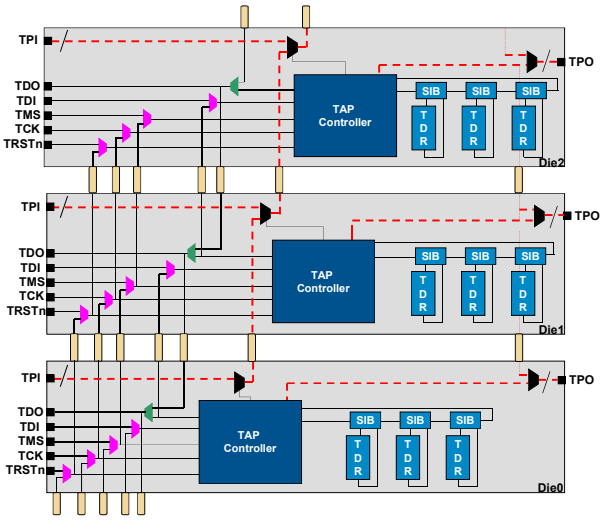

Figure 5. IEEE P1687 based 3D DFT architecture

Each individual die can embed a variety of DFT logic controlled from its TAP controller and associated TDRs. The proposed 3D DFT architecture requires that all stacked dies are equipped (1) with a JTAG interface as a test access mechanism in order to build the 3D DFT chain, and (2) a TAP controller to build around it IEEE P1687 circuitry: SIBs and associated TDRs.

In order to provide many-bit test data to the tiers after stacking, and thus shorten the test time thanks to concurrent testing of several IPs, each die must be equipped with parallel test inputs. A boundary scan solution with a parallel test access mechanism can be found in [15]. Another alternative is to add specific IEEE 1500 test pads WPI (Wrapper Parallel Input) and WPO (Wrapper Parallel Output) as proposed in [6,7]. This test scheme however requires the implementation of parallel test TSVs on every die for providing many-bit test data to the tiers after stacking (see dotted lines in fig.5).

The detailed control of the JTAG Multiplexers is out of the scope of this paper. It could be done with additional configurations registers as currently proposed in IEEE P1838 [8] or it could be optimized using an automatic die-detection mechanism as proposed in [16, 17] but with the limitation of having a static concatenated TAP serial chain.

B. *Heterogeneous 3D DFT architecture*

Stacked 3D-ICs may have an irregular test structure; i.e. dies do not embed the same test infrastructure. Such circuits are 2.5D circuits with dies stacked on an interposer using TSVs[18]. Figure 6 gives an example of such 2.5D circuit with 3 stacked dies: die_0 (left) is JTAG compliant, die_1 (middle) has a 3-bit test interface (test start, test enable, test result), and die_2 (right) has a IEEE 1500 wrapper.

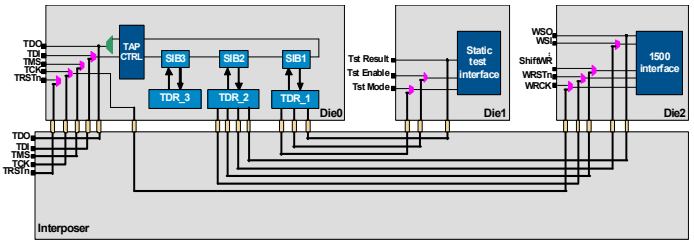

Figure 6. 3D DFT Architecture of a 3D circuit on passive interposer

Die_0 has been modified in order to manage the test of all the dies in the 2.5D system. A gateway register allows a dynamic configuration of the test infrastructure. Die_0, die_1 and die_2 can be concurrently or serially tested thanks to the SIBs. Die_0 embeds the IEEE P1687 infrastructure: the TAP controller, an IR and a decoder. Die_1 and Die_2 are considered as instruments. We note that the signals WSI and WSO of the IEEE 1500 interface of die_2 are connected directly to the active scan-path and not through latches of the TDR_2 [10].

C. *Comparison between both architectures*

As a summary, the first test architecture shown in Figure 5 manages the test of uniform 3D circuits where all stacked dies have the same IEEE 1149.1 test interface in our case. Test signals are transmitted from the bottom die to the top die using TSVs as elevators. Each die embed IEEE P1687 infrastructure which enables test pattern retargeting and enhance test time optimization which will be explained in more details in the next section.

The second test architecture shown in Figure 6 manages the test of heterogeneous 3D circuits such as 2.5D circuits where dies are stacked on passive interposer and have different test interfaces. One die should embed IEEE 1149.1 test interface and IEEE P1687 specific circuitry; this die will be considered as the master die. The other dies will be considered as slaves and are accessed through the master die as instruments.

The 2 proposed test architectures can be mixed for complex 3D circuits with multi-tower stacked dies: each tier should have an IEEE 1149.1 test interface and establish the serial connection to its adjacent tiers, and within the tier one die can be used as a master die to manage the test of its adjacent dies.

IV. BENEFITS OF IJTAG OVER JTAG IN 3D CONTEXT

The IEEE P1687 uses JTAG logic as test access mechanism with some additional test circuitry. This added circuitry is the key to improve flexibility and test concurrency with a negligible added area overhead. On the other hand the use of ICL and PDL allow test pattern retargeting.

A. *Improving test concurrency and flexibility*

The difference between JTAG and IJTAG in term of flexibility is that in IEEE P1687, the configuration of TDRs to be chained between TDI and TDO can be configured dynamically by the mean of SIBs. Conversely, with JTAG, the instructions for implementing test concurrency have to be chosen at design phase of the dies. Thus, to allow the same flexibility as IJTAG, the number of instructions **I** to be encoded in the JTAG instruction register is:

$$I = C_N^1 + C_N^2 + \ldots + C_N^{N-1} + C_N^N = 2^N - 1$$

where N is the number of instruments and C_N^p represents all possible combinations to launch concurrently p instruments amongst the N. This is unaffordable when the number of instruments (IPs) is quite large.

Secondly, from a different perspective, the set of IPs that can be tested concurrently may depend of the test phase (pre-, mid- or post-bond) because of power and/or thermal issues. With JTAG, the sets of concurrently tested IPs have to be chosen at design time and cannot be further modified. On the opposite, with IJTAG, these sets can be dynamically changed.

All this shows that the IEEE P1687 is more flexible than JTAG. Applied to our 2 proposed test architectures, this flexibility allows to improve test concurrency by launching many instruments (such as BISTs) within one single die, or to launch concurrent testing of many instruments in different dies at the same time.

As a conclusion, IEEE P1687 is more flexible than JTAG in 3D context thanks to the dynamic configuration of SIBs and hence IEEE P1687 improves test concurrency at intra-die and inter-die level.

B. *Test pattern retargeting*

Integrated circuits are becoming more and more complex with dozens of embedded instruments and associated test infrastructures such as Memory, logic or analog BIST engines for a variety of components , scan-chain reconfiguration logic (All-Scan, Domain-Scan), Speed Sense instruments, EFUSE Blocks, Temperature Sensors, PLLs, Clock Control Blocks, Power Mitigation circuits, Voltage Scaling modules. This leads to complicated DFT and test phases for test engineers and other product test specialists who are faced to develop chip-level test pattern sets for deeply embedded instruments [19]. This tendency will be even worse with the deployment of the 3D technology. Test pattern retargeting is thus an industrial need to optimize the test time and minimize DFT and test pattern generation time.

Retargeting takes care of the correct handling for test patterns and test benches from one level to another. This is one of the test challenges of 3D circuits: to cover test at all fabrication levels, including pre-bond test (die-level), mid-bond test (partial stack level) and post-bond test (final stack level) by supplying the corresponding test patterns for test and test benches to perform simulations.

As a summary, in 3D context test pattern retargeting means the retargeting of test patterns of a given instrument, which can be a BIST engine within one die, from pre-bond level to post-bond level for partial-stack or final-stack testing. This should be done under 3D hardware constraints: especially, serial TDI TDO chain between dies. This is too difficult to be done using classical JTAG test standard due to the lack of flow and high level languages for JTAG. Although there is the SVF (Serial Vector Format) [20] language that can be associated to BSDL (Boundary Scan Description Language), it is still not sufficient for complex circuits. A comparison between test pattern retargeting using BSDL associated to SVF and test pattern retargeting using IEEE P1687 ICL and PDL can be found in [9].

IEEE P1687 flow using ICL and PDL is more suitable to handle complex circuits with many instruments embedded within, especially for 3D integrated circuits. In the next section, we show the application of this flow to our 2 proposed 3D DFT architectures: the uniform and the heterogeneous approaches.

V. IEEE P1687 3D TEST PATTERN RETARGETING USING ICL AND PDL

To fully enable and automate the use of IJTAG, an EDA software is needed for generating the PDL at the top level of the design. While the IEEE 1149.1 standard is widely used and supported by many EDA tools, few EDA tools support the new IEEE P1687. An example of automated test creation for mixed signal IP using IJTAG is presented in [21] using a commercial EDA tool. We also did experiments with this tool to perform test pattern retargeting from 2D to 3D.

A. *Test pattern retargeting Flow using IEEE P1687*

For our approach we used the IJTAG tool in 3D context. The tool flow is shown in Figure 7, where input files are ICL, PDL, and user defined files. The use of such high level languages is very advantageous since it decreases considerably the development time and increases the reusability from 2D to 3D, especially when using the same flow and the same tool.

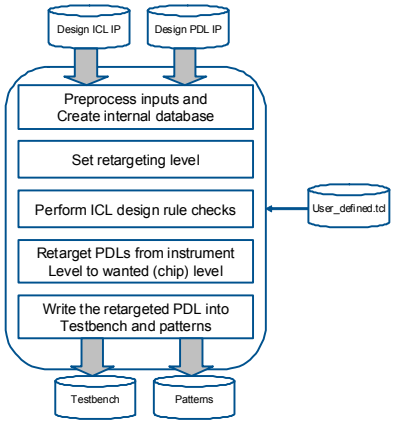

Figure 7. Tessent IJTAG flow

The EDA tool flow shown in Figure 7 consists of 5 major tasks: The first task reads all ICL and PDL descriptions of the design. The second is to set the retargeting level by changing a variable called *current_design*. The third task performs IEEE P1687 related design rule checks (DRCs) to validate the ICL description of the circuit. The fourth task retargets the PDL description of instrument to the chip's top level.

The final task is to translate the resulting retargeted 1687 PDL into IEEE Std 1364 Verilog testbench and standard test vector formats like WGL, SVF or STIL. [14]

B. Study of the uniform 3D DFT architecture

1) ICL description

The ICL description of the circuit shown in Figure 5 is given in List 1, where 3 instances constitute the module Stack_3D: bottom_die, middle_die and top_die.

```
Module Stack_3D {
TCKPort TCK;
ScanInPort TDI;
ScanOutPort TDO {Source top_die.TDO; }
TMSPort TMS;
TRSTPort TRST;
Instance bottom_die Of die_logic_bot {
InputPort TCK = TCK ;
InputPort TDI = TDI ;
InputPort TMS = TMS ;
InputPort TRST = TRST ;}
Instance middle_die Of die_logic_mid {
InputPort TCK = TCK ;
InputPort TDI = bottom_die.TDO ;
InputPort TMS = TMS ;
InputPort TRST = TRST ;}
Instance top_die Of die_logic_top {
InputPort TCK = TCK ;
InputPort TDI = middle_die.TDO ;
InputPort TMS = TMS ;
InputPort TRST = TRST ;}
}
```

List 1. Top level ICL file for uniform case

In each die, all components like SIBs, TDRs, instrument controllers are described in ICL in a way that all connections between instruments and their components are declared. The whole ICL code is not shown here due to lack of space.

2) Example of pattern retargeting using PDL

The purpose of 3D test pattern retargeting is to use the same flow for pattern generation at pre-bond and post-bond levels. An example showing the generation of test patterns corresponding to the launch of a BIST within die_1 (middle die), which has only 2 signals: BIST_start and BIST_result.

```
iProcsForModule BIST_controller
iProc start_BIST {  }  {
   iNote "Setting commands to launch the BIST"
   iWrite BIST_start 1
   iApply
   iRunLoop 20 -tck
   iNote "Reading BIST result"
   iRead BIST_result signature
   iApply
      }
```

List 2. PDL description of one BIST controller

To generate BIST test pattern for pre-bond, the variable *current_design* is set to *die_logic_mid*, and the procedure is called as follows: *iCall BIST_controller_0.start_BIST*.

For pos-bond, test patterns are easily retargeted by setting *current_design* to *Stack_3D*, and calling the procedure as follows: *iCall middle_die.BIST_controller.start_BIST*. The corresponding generated STIL patterns are shown in Figure 8.

```
Ann {* + TAP vector tdi..tdo (BIST_start.TDR[1:0]) *}
Ann {* +  Loading: 01 *}
Ann {* + Unloading: XX *}

Ann {* + TAP vector tdi..tdo (bottom_die.bypass middle_die.BIST_start.TDR[1:0] *}
Ann {* +                     top_die.bypass) *}
Ann {* +  Loading: 0_01_0 *}
Ann {* + Unloading: X_XX_X *}
```

Figure 8. Portion of generated STIL patterns for pre-bond (upper part) and post-bond (lower part) cases of the uniform architecture

The comparison of generated STIL patterns for both pre-bond and post-bond cases allows some conclusions:

- For pre-bond case, test pattern generates test signals to be used at the level of primary JTAG inputs of the middle. This fits pre-bond test requirements since the access is done through dedicated pads
- For post-bond case, test pattern is generates test signals to set automatically the bottom and top dies in bypass mode, and to launch the BIST within middle die.

C. Study of the heterogenous 3D DFT architecture

1) ICL description

In List 3, the ICL description of the circuit shown in Figure 6 is given. *Stack_2_5D* is the highest module in the stack where only 4 components are instantiated here (due to space limitation), which are *die_0_master* corresponding to die_0 in Figure 6, *SIB_1* and *TDR_1* corresponding to the segment insertion bit and test data register controlling die_1, and finally *die_1_interface* where only test signals are used to simplify the example. The SIB and TDR are controlled by the TAP controller of die_0 where capture, shift, and update signals are generated according to the JTAG state machine.

```
Module Stack_2_5D{
TCKPort TCK;
ScanInPort TDI;
ScanOutPort TDO {Source IR_DR_MUX; }
TMSPort TMS;
TRSTPort TRST;
Instance die_0_master Of die_logic {
InputPort TCK = TCK ;
InputPort TDI = TDI ;
InputPort TMS = TMS ;
InputPort TRST = TRST ;}
Instance SIB_1 Of SIB {
InputPort tdi = TDI;
InputPort enable = TAPC.en_sib_1;
InputPort shiftdr = TAPC.shiftDR;
InputPort clockdr = TAPC.captureDR;
InputPort updatedr = TAPC.updateDR;
InputPort TCK = TCK;}
Instance TDR_1 Of TDR_die_1_tst_interface {
InputPort rslt_from_bist = die_2.tst_result;
InputPort tdi = SIB_1.To_TDR_Scan;
InputPort enable = SIB_1.enable_TDR;
InputPort shiftdr = TAPC.shiftDR;
InputPort clockdr = TAPC.captureDR;
InputPort updatedr = TAPC.updateDR;
InputPort tck = TCK;
InputPort resetn = TRST;}
Instance die_1_interface Of die_1_test_interface{
InputPort tst_enable = TDR_1.tst_enable;
InputPort tst_mode = TDR_1.tst_mode;}}
```

List 3. Top level ICL file for heterogeneous case

The next example shows only how to generate a test pattern for *die_1* through *die_0* by the mean of *SIB_1* and *TDR_1* using the ICL and PDL languages. The same flow is used to generate test patterns for *die_2* which has an IEEE 1500 test access mechanism by the mean of *SIB_2* and *TDR_2*, as well as to generate test patterns for internal instruments of die_0 such as BIST engines by the mean of *SIB_3* and *TDR_3*.

2) Example of pattern retargeting using PDL

The PDL file in list 4 shows the test sequence wanted to be retargeted at from die level to stack level, where the two test signals *tst_enable* and *tst_mode* are set to logic 1.

```
iProcsForModule die_1_test_interface
iProc start_TEST {  }  {
   iNote "Configuring die_1 test inputs to
launch test mode"
   iWrite tst_enable 1
   iWrite tst_mode 1
   iApply
   iRunLoop 20 -tck
   iNote "Reading test result"
   iRead tst_result
   iApply
      }
```

List 4. PDL description of static test interface launch of die_2

To generate test patterns for pre-bond, the variable *current_design* is set to *die_1_test_interface* and the procedure is called iCall *start_TEST*. And for post-bond, test patterns are retargeted by setting the variable *current_design* to *Stack_2_5D* and calling the procedure as follows: iCall *die_1_interface.start_TEST*.

A part of the generated test patterns are shown in Figure 9: the upper part for pre-bond and the lower part for post-bond.

```
Ann {* +        tst_enable  =  1 *}
Ann {* +        tst_mode    =  1 *}
-------------------------------------------------------
Ann {* +        TDR_1.tst_enable  =  1 *}
Ann {* +        TDR_1.tst_mode    =  1 *}
Ann {* + TAP vector tdi..tdo (SIB_1.REG TDR_1.REG[1:0]) *}
Ann {* +  Loading: 1_11 *}
Ann {* + Unloading: X_XX *}
```

Figure 9. Portion of generated STIL patterns for pre-bond (upper part) and post-bond (lower part) cases of the heterogeneous architecture

The comparison of generated STIL patterns for both pre-bond and post-bond cases allows some conclusions:

- For pre-bond case, test pattern generates test signals to be used at the level of primary inputs of *die_1,* in a way that the generated test pattern can be used at wafer level test. This fits pre-bond test requirements since the access is done through dedicated pads.
- For post-bond case, test pattern generates test signals through the JTAG interface of die_0, *SIB_1* is configured to open the path to *TDR_1*, and data is shifted within *TDR_1* to launch the test of *die_1*.

In terms of area overhead, we have implemented an example of a 3D DFT architecture (as in Figure 5) with both JTAG and IJTAG and we compared synthesis results. As expected, the DFT architecture based on IJTAG (10960 μm^2) is more costly with only 1% of added DFT than JTAG (10700 μm^2). The slight additional cost corresponds to added SIBs and TDRs.

VI. Conclusion And Future Work

We have presented a 3D DFT architecture based on the IEEE P1687 test standard. Our proposed 3D DFT architecture enables the test of 3D components at all testing levels: pre-, mid- and post-bond levels by switching between test pads and test TSVs using die-detectors. We explore test architectures for uniform (all dies embedding JTAG test interface) and heterogeneous (dies have different test access mechanism) 3D-ICs. The proposed 3D DFT architecture should be in line with the ongoing IEEE P1838 standard definition. The IEEE P1687 allows test pattern retargeting from 2D to 3D thanks to high level languages ICL and PDL. Benefits of IJTAG over JTAG are the enhanced flexibility in test concurrency thanks to the dynamic selection of instruments through SIBs. Test pattern retargeting has been experimented with a commercial EDA tool. This work opens perspectives towards 3D test scheduling of various instruments "IPs" with physical constraints such as power and thermal issues.

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