3-D-Integrated RF and Millimeter-Wave Functions and Modules Using Liquid Crystal Polymer (LCP) System-on-Package Technology

Manos M. Tentzeris, *Senior Member, IEEE*, Joy Laskar, *Senior Member, IEEE*,
John Papapolymerou, *Senior Member, IEEE*, Stéphane Pinel, V. Palazzari, R. Li, *Senior Member, IEEE*, G. DeJean,
N. Papageorgiou, D. Thompson, R. Bairavasubramanian, S. Sarkar, and J.-H. Lee

***Abstract*—Electronics packaging evolution involves system, technology, and material considerations. In this paper, we present a novel three-dimensional (3-D) integration approach for system-on-package (SOP)-based solutions for wireless communication applications. This concept is proposed for the 3-D integration of RF and millimeter (mm) wave embedded functions in front-end modules by means of stacking substrates using liquid crystal polymer (LCP) multilayer and μBGA technologies. Characterization and modeling of high-Q RF inductors using LCP is described. A single-input-single-output (SISO) dual-band filter operating at ISM 2.4–2.5 GHz and UNII 5.15–5.85 GHz frequency bands, two dual-polarization 2x1 antenna arrays operating at 14 and 35 GHz, and a WLAN IEEE 802.11a-compliant compact module (volume of $75 \times 35 \times 0.2$ mm^3) have been fabricated on LCP substrate, showing the great potential of the SOP approach for 3-D-integrated RF and mm wave functions and modules.**

***Index Terms*—Dual-band antenna, dual-band filter, embedded functions, high-Q passives, inductors, liquid crystal polymer (LCP), μBGA, multilayer modules, RF and mm-waves front-end module, system-on-package (SOP), three-dimensional (3-D) integration.**

I. INTRODUCTION

EMERGING wireless communication and sensor applications in the RF/microwave/millimeter (mm) wave regimes require miniaturization, portability, cost, and performance as key driving forces in the electronics packaging evolution. The system-on-package (SOP) approach [versus the system-on-chip (SOC)] for module development [1] has become a primary focus of research due to the real estate efficiency, cost-saving, size reduction, and performance improvement contributed by its inherent capability for the easy integration of embedded functions, thus, simultaneously satisfying the specifications of the next generation wireless communication systems. Also, the three-dimensional (3-D) integration approach is an emerging and very attractive option for these systems. However, current 3-D RF module integration is still based on low-density hybrid assembly technologies [2], [3].

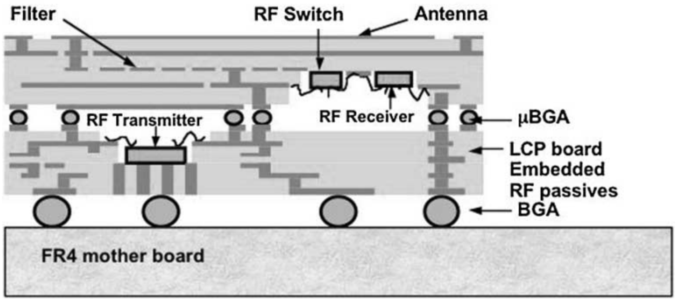


Fig. 1. 3-D-integrated module concept view.

In this paper, we present novel liquid crystal polymer (LCP) multilayer technologies, and stacking board technique using μBGA as the candidates of choice for the 3-D integration of RF front-end modules up to 35 GHz. Various figures of merit of the performance of high-Q RF inductor such as quality factor values up to 90 in C and X bands, using LCP are reported. A single-input-single-output (SISO) dual-band filter using the "dual-behavior resonators" technique is presented for WLAN operating frequency bands ISM 2.4–2.5 and UNII 5.15–5.85 GHz. The insertion loss and return loss at the central frequency are 2.4 and 15 dB for the 2.4-GHz band, respectively, and 1.8 and 8 dB for the 5-GHz band, respectively. Two dual-polarization 2×1 antenna arrays on LCP are also reported. The frequencies of operation are 14 and 35 GHz and and both integrated structures exhibit a high efficiency and a low cross-polarization level. Finally, one WLAN IEEE 802.11a-compliant compact module (volume of $75 \times 35 \times 0.2$ mm^3) has been fabricated on LCP substrate, showing the great potential of the SOP approach for 3-D-integrated RF and mm waves functions and modules.

II. 3-D-INTEGRATED MODULE CONCEPT

Fig. 1 illustrates the proposed multilayer module concept. Two stacked SOP multilayer substrates are used and board-to-board vertical transition is ensured by μBGA balls. Standard alignment equipment is used to stack the board and, thus, provide a compact, high-performance, and low-cost assembly process. Multistepped cavities into the SOP boards provide spacing for embedded RF active devices (RF switch, RF receiver, and RF transmitter) chipset and, thus, lead to significant volume reduction by minimizing the gap between

---

Manuscript received December 7, 2003; revised February 16, 2004. This work was supported in part by the NSF CAREER, ECS-9984761, the NSF ECS-0313951, and the Packaging Research Center, and NASA under Contract NCC3-1015.

The authors are with the Georgia Electronic Design Center, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: etentze@ece.gatech.edu).

Digital Object Identifier 10.1109/TADVP.2004.828814

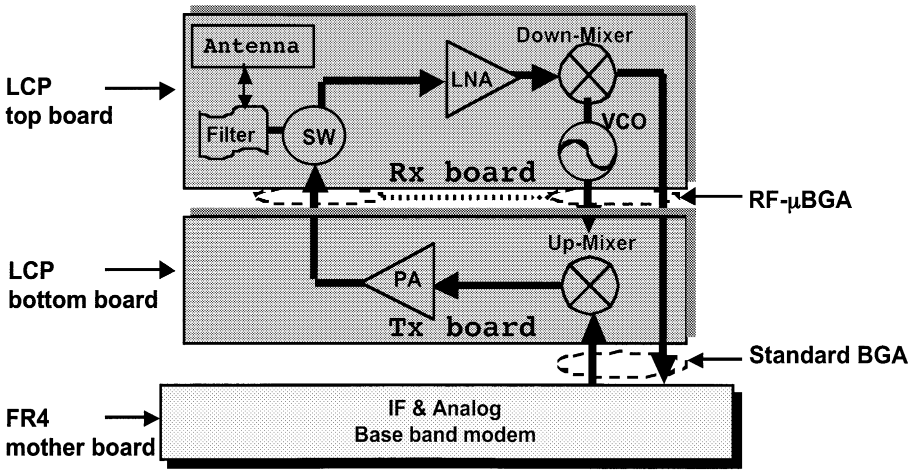


Fig. 2. Rx and Tx board block diagram.

TABLE I
COMPARAISON OF SUBSTRATE PROPERTIES

	FR4	LTCC	LCP
Dielectric constant	4.5@1MHz	5.6@20GHz	2.9-3.0@20GHz
Loss Tangent	0.02	0.0012	0.002
CTE	$15\text{-}20{*}10^{-6}$/K	$5.9{*}10^{-6}$/K	$3\text{-}17\ {*}10^{-6}$/K engineered
Cost	Very Low	Medium	Low

the boards. Active devices can be flip-chiped, as well as wire-bonded. Cavities also provide an excellent opportunity for the easy integration of RF MEMS devices, such as MEMS switches or tuners. Passive components, off-chip matching networks, embedded filter, and antennas are implemented directly into the SOP boards by using multilayer technologies [4]–[6]. Standard BGA balls ensure the effective broadband interconnection of this high density module with motherboards such as the FR4 board. The top and the bottom substrates are dedicated respectively to the receiver and transmitter building blocks of the RF front-end module.

Fig. 2 shows the RF block diagram of each board. The receiver board includes antenna, bandpass filter, active switch, and RF receiver chipset (LNA, VCO, and downconversion mixer). The transmitter board includes RF transmitter chipset (upconverter mixer and power amplifier) and off-chip matching networks. Ground planes and vertical via walls are used to address isolation issues between the transmitter and the receiver functional blocks. Arrays of vertical vias are added into the transmitter board to achieve better thermal management.

III. LCP MULTILAYER SUBSTRATE AND μBGA STACKING APPROACH FOR 3-D INTEGRATION

A. LCP Multilayer Substrate Properties

Multilayer substrates have been, and still are, of great interest for research in the area of the 3-D integration of RF and mm wave functions and modules using the SOP approach. Our presented results have been focused mainly on advanced multilayer organic substrates using FR4 material and advanced material such as LCP, in comparison with the more mature, but also more expensive ceramic-based platforms such as low-temperature cofired ceramic (LTCC). The choice of the most suitable technology depends on the application specifications such environment, frequency of operation, performance, volume, and cost.

LCP is a fairly new and promising thermoplastic material [7]. It can be used as a low-cost dielectric material for high-volume large-area processing methods that provide very reliable high-performance circuits at low cost. LCP has a unique combination of properties as follows [11].

— Excellent electrical properties up to mm waves, such as low dielectric constant of 3.0 @ 20 GHz and low-loss tangent of 0.002 @ 20 GHz comparable with ceramics (cf. Table I).

— Very good barrier properties, permeability (moisture absorption ~0.02%) comparable to that of glass and very close to that of ceramic.

— Low coefficient of thermal expansion (CTE) as low as $8-17\cdot10^{-6}$/K, adjustable through thermal treatments process coefficient of thermal expansion, and close to that of ceramic ($6\cdot10^{-6}$/K) (cf. Table I).

Material, electrical, and cost considerations make LCP a serious candidate for all multichip-module (MCM), SOP, and advanced packaging technologies led by a tremendously growing market of RF, sensor, digital,optical and mixed-signal applications.

B. Stacking Board Technique Using μBGA

To achieve significant volume reduction, 3-D integration approaches are a very attractive option for RF front-end module integration. The board-stacking technique has emerged as the most promising approach to simultaneously achieve size reduction, performance improvement, reliability, and cost-saving. In this paper, we presented a Georgia Tech developed process dedi-

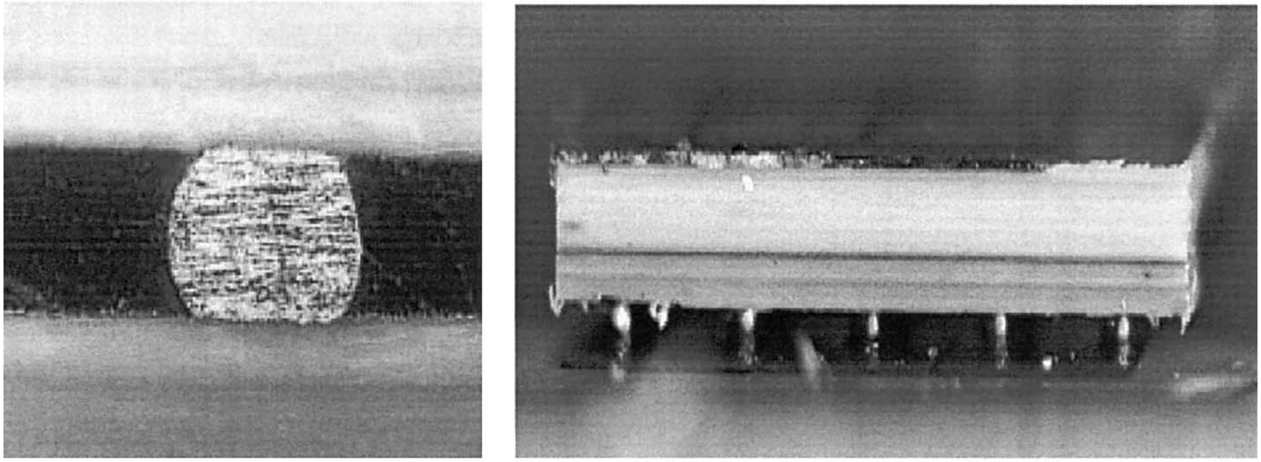

(a) (b)

Fig. 3. 4 mils solder ball transition. (a) Side view of fabricated test structures showing stacked LCP substrates; (b) μBGA transitions.

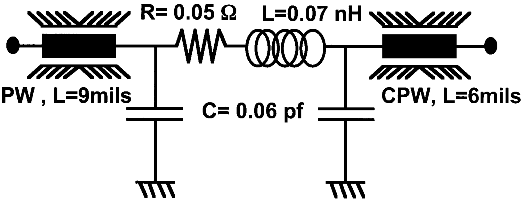


Fig. 4. Extracted μBGA hybrid model.

cated to board-to-board stacking and interconnection using preformed solder balls (Sn63Pb37–183 °C) and conventional reflow process. Fig. 3(a) shows a cross section of one 4-mils solder ball transition, and Fig. 3(b) shows a side view of a fabricated test structure with stacked LCP substrates and μBGA (4 mils in diameter) transitions.

A combination of an *RLC* $\prod$-network and a transmission-line model, shown in Fig. 4, is applied to model the μBGA vertical RF transition. The two transmission line sections are added to model accurately the phase responses of S11 and S21. Both measured and simulated results exhibit insertion loss less than 0.1 dB and return loss about −17 dB up to 10 GHz.

IV. CHARACTERIZATION AND MODELING OF HIGH-Q RF-INDUCTOR IMPLEMENTED USING LCP TECHNOLOGY

A. Inductor Physical Model

The key to optimize the performance of RF inductors is to identify the relevant parasitic and their effects. Physical modeling is the best approach leading to in-depth understanding of the devices [8], [9]. An associated physical hybrid model for a typical coplanar inductor is shown in Fig. 5. The inductance and the resistance directly associated with the inductive coil are modeled, respectively, by Ls and Rs. The parasitic coupling between the turns of the coil, as well as the overlap between the coil and the underpass, contribute to a direct capacitive coupling between the input and the output port. These parasitic coupling effects are modeled by the series capacitance Cs. Csub, Rsub are related to the dielectric capacitance, the substrate capacitance, and the substrate resistance, respectively.

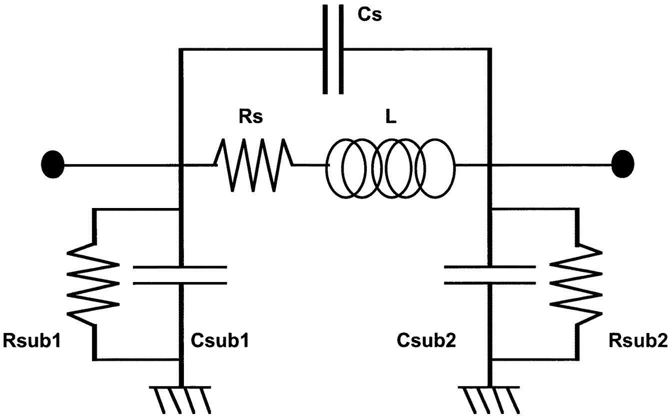


Fig. 5. Physical model of a 2-port RF inductor.

We carried out the self-inductance calculation using a formula based on the partial element equivalent circuit (PEEC) analysis method proposed by Ruehli *et al.*. Full wave simulations were performed to adjust the empirical coefficient to take in account the mutual inductance effect. Because of the current distribution across the cross section of the conductor, the skin depth effect, the metal roughness, and the crowding current effect, the evaluation of the series resistance is challenging. PEEC formulas were used, as well as measurement data to adjust empirical coefficients. Since at the very high frequencies of interest all conductors are subject to radiations losses, a polynomial frequency dependency was added to the expression of the series resistance to take into account those effects. The series capacitance has been directly calculated from the structure's topology. The substrate capacitance and resistance have been extracted from measurement results. The physical model described in Fig. 5 can be simplified in the one-port case as described in Fig. 6.

The most fundamental definition for the inductor quality factor is given by

$$Q = 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy lost in one oscillation cycle}}. \tag{1}$$

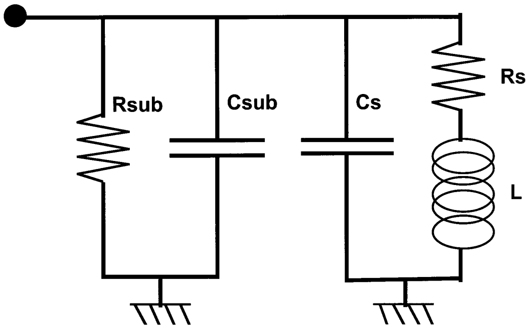


Fig. 6. Physical model of a 1 port RF inductor.

In the one port case, this can be expressed as follows:

$$Q = \frac{\omega L}{Rs} \cdot \text{substrate loss factor} \cdot \text{self}-\text{resonance factor}. \quad (2)$$

With

$$\text{substrate loss factor} = \frac{\text{Rsub}}{\text{Rsub} + [(\omega L/Rs)^2 + 1] \cdot Rs} \quad (3)$$

and

$$\text{self}-\text{resonance factor} = 1 - \frac{Rs^2(\text{Csub} + \text{Cs})}{L} - \omega^2 L \cdot (\text{Csub} + \text{Cs}). \quad (4)$$

B. Measurement Results

S-parameter measurements were performed with an HP8510B Network Analyzer, cascade coplanar ground-signal-ground probes, and a temperature- and humidity-controlled environment. Particular attention has been paid in order to perform a very accurate LRRM calibration for high-Q measurements. The fabricated inductor exhibits inductance values ranging from 1.1 up to 4 nH and self-resonance frequency from 8 to 16 Ghz. In Table II, we have reported typical measured performances of RF inductors fabricated on LCP multilayer substrate.

Table III shows parameter values extracted for a 1.1 nH inductor with a diameter of 20 mils that has been fabricated on LCP.

The physical based model we developed initially did not accurately model the degradation of the quality factor due to radiation losses. Therefore, a polynomial frequency dependency was added to the expression of the series resistance Rs to model radiations losses and led to better agreement with measurements for Q@5.8 Ghz with a value around 90. The total series resistance expression Rrad is described in (5).

$$Rrad = Rs \cdot \left[1 + 0.1 \left(\frac{f}{fc}\right)^5\right]$$
$$\text{with} \quad fc = 8\ \text{GHz}. \quad (5)$$

Fig. 7 shows measurement results compared with the model in the case of a high-Q RF inductor implemented on a LCP substrate.

TABLE II
SUMMARY OF TYPICAL MEASURED RF INDUCTOR PERFORMANCES USING LCP TECHNOLOGY

L nH	Quality Factor	SRF GHz
1.1	**90**@5.8GHz	**16**
1.5	**90**@4GHz	**15**
2	**80**@4GHz	**15**
4	**70**@2.4GHz	**8**

TABLE III
EXAMPLE OF EXTRACTED PHYSICAL BASED MODEL PARAMETERS OF RF INDUCTOR ON LCP

L (nH)	Cs (fF)	Csub (fF)	Rsub (kΩ)
1.132	**5**	**60**	**20**

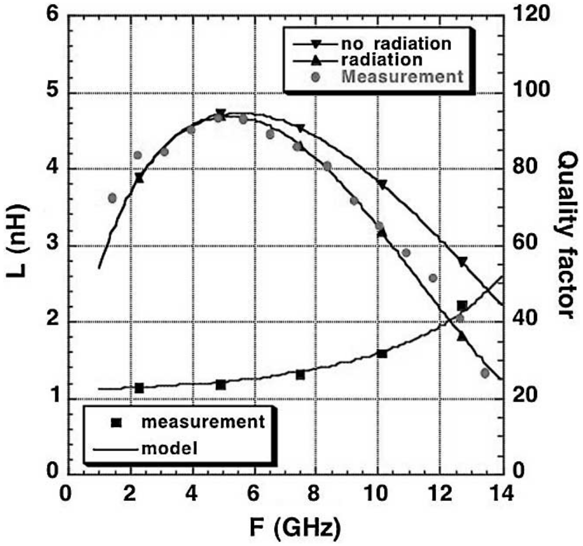


Fig. 7. Measurement performance compared with physical based model for a high-Q inductor fabricated on LCP.

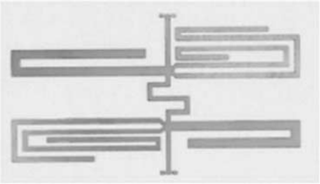


Fig. 8. Photograph of the fabricated SISO LCP dual-band filter.

V. SISO LCP DUAL-BAND FILTER

A SISO LCP dual-band filter has been synthesized based on the novel "dual-behavior resonator" technique. The WLAN operating frequency bands ISM and UNII around 5 GHz have been targeted because of the ever growing number of services allocated in this part of the spectrum, including Bluetooth, IEEE 802.11a/b/g, and the introduction of dual-band wireless systems. WLAN dual-band systems, in fact, allow the WLAN users the freedom of using their preferred frequency whenever they need it, operating on the recent 802.11a 5 GHz for high-speed resolution or the popular 802.11b/g 2.4 GHz for mass access. Most of the products that can be found in the market offer a dual-path architecture. The goal is to exploit the same RF path (SISO), providing support to multiple standards and multiple bands on a single integrated platform while maintaining performances and compactness.

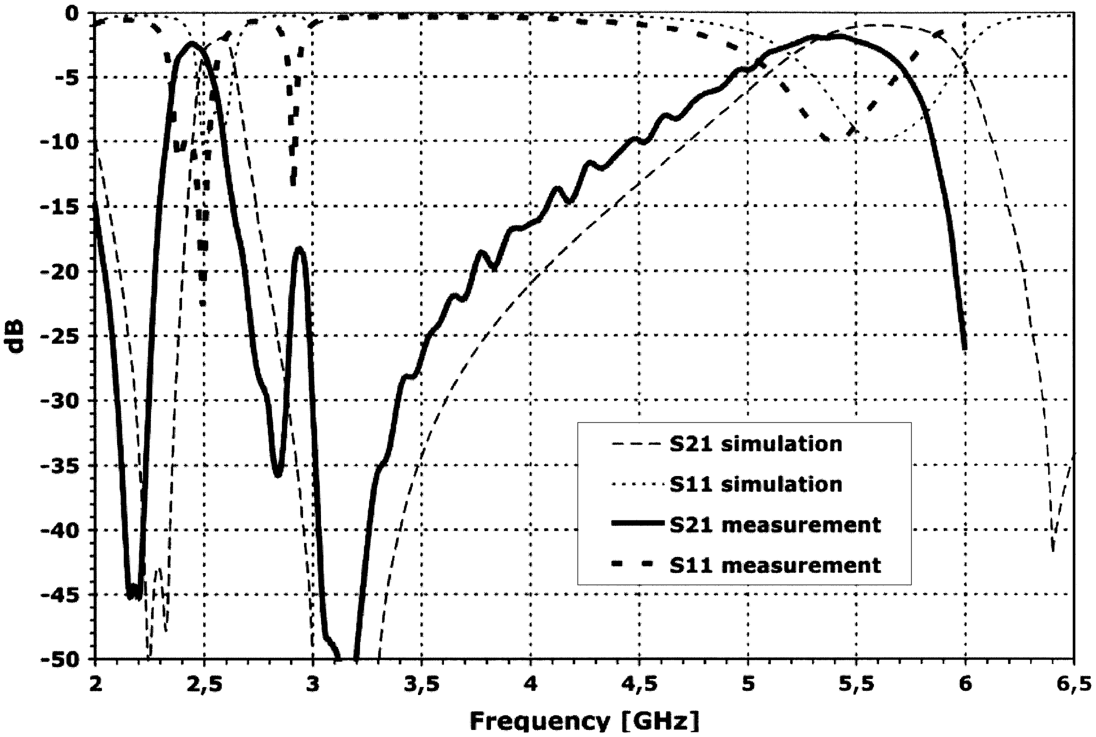


Fig. 9. Measurement compared with simulated performances of the SISO LCP dual-band filter.

The dual-behavior resonators (DBRs) technique is based on the parallel association of two open-ended stub resonators. The open-ended stub is, in fact, the simplest realization of a bandstop structure and demonstrates a dual behavior in the bandpass and stopband regions: using the open stub means inserting a transmission zero, whose resonance frequency can be easily controlled by adjusting the stub length, and by playing with the several degrees of freedom that a microwave design offers. If the stubs are properly connected under constructive recombination criteria, the result is a bandpass response created between the lower and the upper rejected bands. The same approach has been extended to obtain a dual-band narrow bandpass filter, simply adding a third resonator to create a third transmission zero. The procedure described in [10] has been applied to the design of the present filter to provide first guess values for lengths and characteristic impedances (widths). In this case, the location of the transmission zeros has been accurately chosen to control the width and the location of the desired bands, successfully exploiting the second resonance frequency. The frequency bands of interest between 2.4–2.5 and 5.15–5.85 GHz are, in fact, very different in terms of width (narrow band at 2.4 GHz, wide band at 5 GHz). Moreover, the channel spacing is wide and a good rejection is difficult to achieve with conventional approaches. On this basis, the stubs have been dimensioned to have transmission zeros at 2.2, 2.93, and 3.14 GHz. To realize the passband in the 5-GHz range, the second resonance frequency of the first stub has been successfully exploited, while the close transmission zeros at 2.9 and 3.14 GHz allow for a better rejection in the inner stopband. To achieve better selectivity, we designed and fabricated a second-order filter. The folded design has been chosen in order to avoid the impact of stub excessive lengths on the overall filter size. The prototype, shown in Fig. 8, has been fabricated in LCP substrate, characterized by er 2.9, tand 0.002, substrate thickness 275 μm, conductor thickness 9 μm.

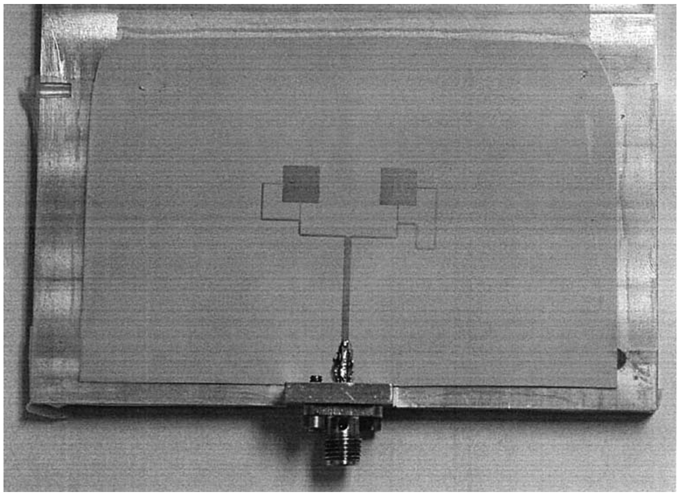
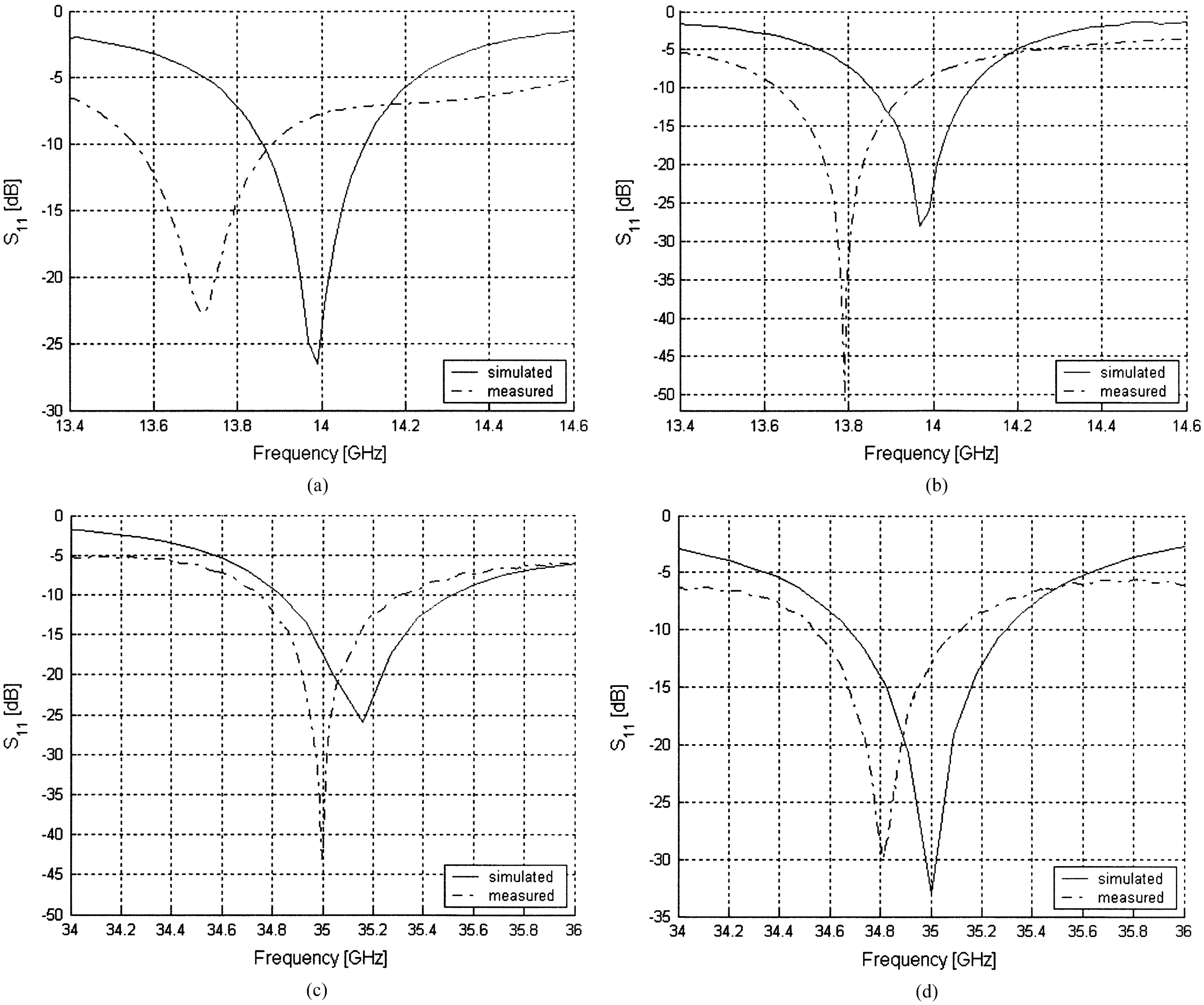


Fig. 10. Top view of the fabricated 2 × 1 array antenna.

Fig. 9 shows the good agreement between simulation and measurement. The insertion loss and return loss at the central frequency are -2.4 dB and -15 dB for the 2.4-GHz band, respectively, and -1.8 dB and -10 dB for the 5 GHz band, respectively. It exhibits also an out-of-band rejection as high as 45 dB between the L and C band.

VI. DEVELOPMENT OF DUAL-FREQUENCY/ DUAL-POLARIZATION MICROSTRIP ANTENNA ARRAYS ON LCP SUBSTRATES

Two dual-polarization 2×1 antenna arrays on LCP multilayer laminated substrates have been designed at operating fre-



(a) (b) (c) (d)

Fig. 11. Plot of the simulated and measured results for the return loss versus frequency of the 2 × 1 array for: (a) 14-GHz array, pol.X; (b) 14-GHz array, pol.Y; (c) 35-GHz array, pol.X; (d) 35-GHz array, pol.Y.

quencies of 14 and 35 GHz (mm-wave range) for precipitation remote sensing applications. The top view of the fabricated 2 × 1 antenna arrays is shown in Fig. 10. The metal was copper (Cu) and had a thickness of 18 μm. The total substrate thickness for the design was 425 μm, consisting of two LCP layers (each 200 μm thick) and a 25 μm bonding layer. The substrate thickness was chosen to achieve at least a 1.5% impedance bandwidth at -10 dB, while maintaining a compact structure. The 14-GHz antenna array was placed on the top layer of the LCP substrate (at the interface of LCP and air), while the 35-GHz antenna array was "sandwiched" between two embedded layers for compactness and crosstalk minimization reasons. The LCP layer under the 35 GHz antenna array had a thickness of 200 μm. Both arrays were fed by microstrip lines printed on the same layer as the corresponding array. To further prevent parasitic coupling between the two antenna arrays, the antennas in the 35-GHz array have a linear ("diamond") topology and the 14 GHz array maintains the "square" configuration. The control of the two orthogonal linear polarizations is achieved through the use of two small gaps in the feedlines for two perpendicular directions, which introduced a small capacitance in each gap. The small capacitance on the order of fFs in the gap represents high impedance values or an "almost ideal" electrical open circuit which prevents the mode excitation of the corresponding polarization. RF MEMS switches or pin diodes can be utilized to achieve this effect by turning on to excite a specific polarization and turning off to switch to the alternative polarization.

Simulations of both arrays were performed, separately, using the 3-D full-wave simulation programs EmPicasso and Micro-Stripes. Plots of the simulated and measured results for the return loss versus frequency of both polarizations at each frequency are shown in Fig. 11. The simulated results show a return loss of approximately -26 dB at a center frequency $(\mathrm{f_c})$ of 13.99 GHz for polarizations X ("horizontal" x-axis feed) and -27 dB at $\mathrm{f_c} = 13.97$ GHz for polarization Y ("vertical" y-axis feed) for the 14-GHz structure. Additionally, the 35-GHz structure exhibits at return loss of approximately -25 dB at $\mathrm{f_c} = 35.15$ GHz for polarization X and -32 dB at $\mathrm{f_c} = 35$ GHz for polarization Y. The measured results for the return loss are as follows: the 14-GHz array has a return loss of approximately

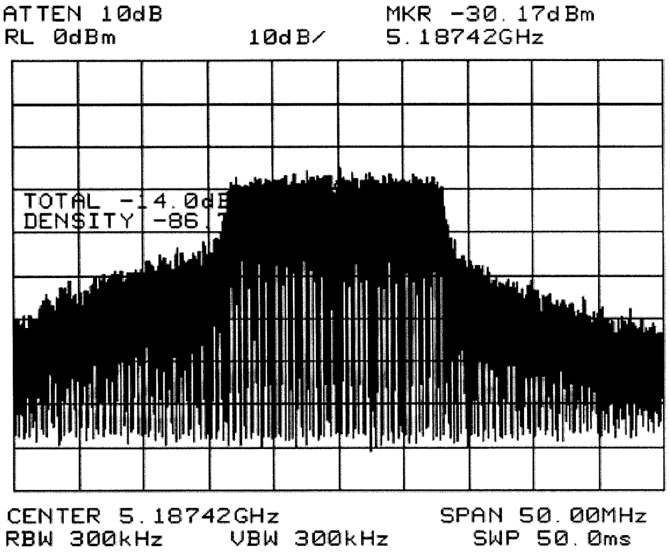


Fig. 12. OFDM signal with carrier frequency = 5.18 GHz and channel power = −14 dBm.

−23 dB at f_c = 13.72 GHz and −51 dB at f_c = 13.79 GHz for polarizations X and Y, respectively, while the 35-GHz array has a return loss of approximately −44 dB at f_c = 35 GHz and −30 dB at f_c = 34.81 GHz for polarizations X and Y, respectively. It can be seen that a good agreement is observed between the simulated and measured results for the return loss versus frequency plots for the 2 × 1 subarray. The −10 dB return loss percent bandwidths for the measured results are approximately as follows: 2.41% and 2.47% for polarizations X and Y, respectively, for the 14-GHz array and 1.57% and 1.72% for polarizations X and Y, respectively, for the 35-GHz array. The simulated results demonstrated an efficiency of better than 85% for all array antenna designs.

The variation in the simulated and measured results of the return loss for the 14-GHz polarization Y array and the 35-GHz polarization X array can possibly be attributed to a a relatively small number of frequency points used in the simulations. The use of more time steps may show a lower return loss for the simulated plots. A finer discretizaton of cells in the simulations can also possibly lead to a lower return loss values but at the expense of increased computational time. The difference in return loss for the measured results for both polarizations at 14 and 35 GHz can be attributed to the effect of fabrication tolerances. The slight increase in the impedance bandwidth for the measured results in comparison to the simulated results is a result of the substrate thickness in fabrication being about 7 μm greater than that used in the simulations. The frequency shifts in the measured results can also be attributed to fabrication tolerances. This frequency shift in the measured results for both polarizations of the 35-GHz design may be the cause of the difference in relative bandwidth, while in the 14-GHz designs, measurements inaccuracies are the probable cause of the difference in realtive bandwidths.

VII. WLAN MODULE IMPLEMENTATION

The system-level benchmarking structure for the SOP multilayer LPC/μBGA technology was a functional RF compact module (volume of $75 \times 35 \times 0.2$ mm^3) compliant with the IEEE 802.11a WLAN applications, incorporating LCP board technology (Fig. 14). The architecture demonstrated is a superheterodyne Tx/Rx system. Two passive mixers, achieving higher linearity, upconvert the low IF (20 MHz) OFDM signal to the 5.x GHz frequency band (Fig. 12) and two BPF operations cancel the unwanted images after each mixing.

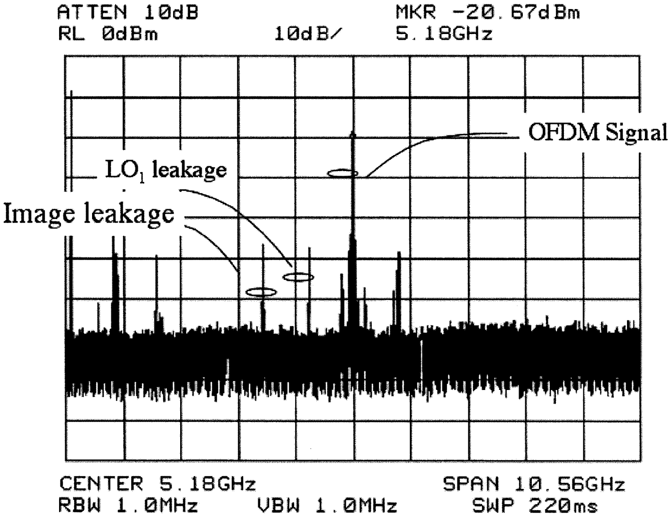


Fig. 13. Image and LO1 cancellation.

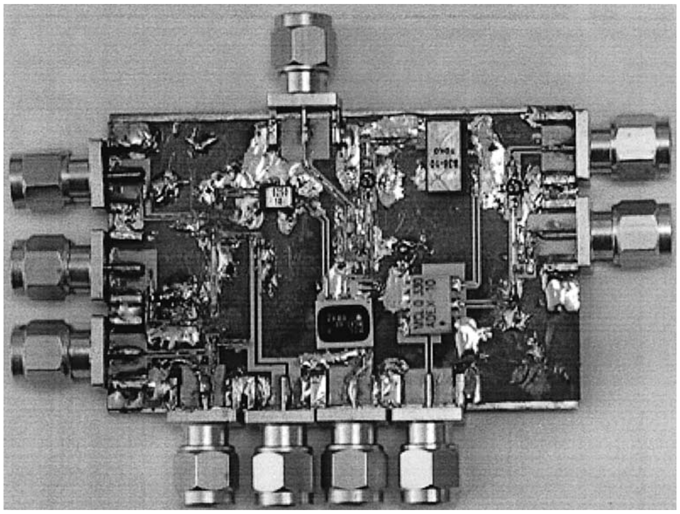


Fig. 14. Photo of the WLAN module.

Driver stages provide the gain needed to balance out the losses due to the passives, while the PA module demonstrating a P1 of 30 dBm enables the operation at a backoff of 6 dB, which is a prerequisite for OFDM transmission. The receiver utilizes variable-gain LNA for linearity considerations. Inspection of the frequency spectrum of the signal at the output of the Tx module (Fig. 13) shows that the leakage of the local oscillator signal is efficiently suppressed to 48 dBm, as well as the leakage of the unwanted image at LO2-LO1. The receiver's overall NF is lower than 8 dB to enable the proper RF reception and then demodulation of signals as low as −70 dBm.

VIII. CONCLUSION

In this paper, we presented the novel LCP multilayer technology and stacking board technique using μBGA as the leading candidates of choice for the 3-D integration of RF and m-wave functions and modules. An accurate modeling and design of high-performance RF inductors (Q in excess of 90) in LCP has been reported. A SISO dual-band filter using the novel "dual-behavior resonators" technique operating at the WLAN frequency bands ISM 2.4–2.5 GHz and UNII 5.15–5.85 GHz has been developed. The insertion loss and return loss at the central frequency are 2.4 and 15 dB for the 2.4-GHz band, respectively, and 1.8 and 8 dB for the 5-GHz band, respectively. Two dual-polarization 2x1 antenna arrays on LCP have been shown for operation at 14 and 35 GHz with an efficiency around 85% and low levels of cross polarization.

Finally, a WLAN IEEE 802.11a-compliant compact module (volume of $75 \times 35 \times 0.2$ mm^3) has been fabricated on LCP substrate, with an excellent performance verifying the great potential of the SOP approach for 3-D-integrated RF and mm-wave functions and modules.

REFERENCES

[1] K. Lim, S. Pinel, M. Davis, A. Sutono, C.-H. Lee, D. Heo, A. Obatoynbo, J. Laskar, M. Tantzeris, and R. Tummala, *RF-SOP Wireless Commun.*: Microwave Mag., Mar. 2002.

[2] R. Sturdivant, C. Ly, J. Benson, and J. Hauhe, "Design and performance of a high density 3D microwave module," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, 1997, pp. 501–504.

[3] P. Monfraix, P. Ulian, P. Drevon, C. George, A. C. Vera, C. Tronche, J. L. Cazaux, O. Llopis, and J. Graffeuil, "3D microwaves modules for space applications microwave," in *IEEE MTT-S Int. Symp. Dig.*, vol. 3, Dec. 2000, pp. 1289–1292.

[4] K. Lim, A. Obatoyinbo, A. Sutuno, S. Chakraborty, C. Lee, E. Gebara, A. Raghavan, and J. Laskar, "A highly integrated transceiver module for 5.8 Ghz OFDM communication system using multi-layer packaging technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, 2001, pp. 65–68.

[5] M. F. Davis, A. Sutono, A. Obatoyinbo, S. Chakraborty, K. Lim, S. Pinel, J. Laskar, S. Lee, and R. Tummala, "Integrated RF function architectures in fully-organic SOP technology," in *EPEP2001—IEEE Proc. Electrical Performances of Electronic Packaging Conf.*, vol. 29–31, Oct. 2001, pp. 93–96.

[6] W. Diels, K. Vaesen, K. Wambacq, P. Donnay, S. De Raedt, W. Engels, and M. Bolsens, "A single-package integration of RF blocks for a 5 GHz WLAN application," *IEEE Trans. Comp., Packag., Technol. Adv. Packag.* , pt. B, vol. 24, pp. 384–391, Aug. 2001.

[7] K. Brownlee, S. Bhattacharya, K.-I. Shinotani, C. P. Wong, and R. Tummala, "Liquid crystal polymer for high performance SOP applications," in *Proc. 8th Int. Symp. Advanced Packaging Materials*, 2002, pp. 249–253.

[8] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. Wong, "A physical model for planar spiral inductor on silicon," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 1996, pp. 155–158.

[9] S. Pinel, F. Cros, S.-W. Yoon, S. Nuttinck, M. G. Allen, and J. Laskar, "Very high Q inductor using RF-MEMS technology for system-on-package wireless communication integrated module," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, Philadelphia, PA, June, 2003, pp. 1497–1500.

[10] C. Quendo, E. Rius, and C. Person, "Narrow bandpass filters using dual-behavior resonators," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 734–743, Mar. 2003.

[11] D. C. Thompson, O. Tantot, H. Jallageas, G. E. Ponchak, M. M. Tentzeris, and J. Papapolymerou, "Characterization of Liquid Crystal Polymer (LCP) Material and Transmission Lines on LCP Substrates from 30-110 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1343–1352, Apr., 2004.

Manos M. Tentzeris (SM'02) received the Diploma Degree in electrical and computer engineering from the National Technical University of Athens in Greece and the M.S. and Ph.D. degrees in electrical engineering and computer science from the University of Michigan, Ann Arbor, MI.

He is currently an Associate Professor with School of ECE, Georgia Institute of Technology (Georgia Tech), Atlanta, GA. He has helped develop academic programs in Highly Integrated Packaging for RF and Wireless Applications, Microwave MEMs, SOP-integrated antennas and Adaptive Numerical Electromagnetics (FDTD, MultiResolution Algorithms) and heads the ATHENA research group. He is the Georgia Tech NSF-Packaging Research Center Associate Director for RF Research and the RF Alliance Leader. He is also the leader of the Novel Integration Techniques Subthrust of the Broadband Hardware Access Thrust of the Georgia Electronic Design Center (GEDC) of the State of Georgia. He was a Visiting Professor with the Technical University of Munich, Germany, during the summer of 2002. He has published more than 140 papers in refereed journals and conference proceedings and eight book chapters.

Dr. Tentzeris was the recipient of the 2003 and 2004 IBC International Educator of the Year Awards, the 2003 IEEE CPMT Outstanding Young Engineer Award, the 2002 International Conference on Microwave and Millimeter-Wave Technology Best Paper Award (Beijing, China), the 2002 Georgia Tech-ECE Outstanding Junior Faculty Award, the 2001 ACES Conference Best Paper Award, the 2000 NSF CAREER Award and the 1997 Best Paper Award, International Hybrid Microelectronics and Packaging Society. He was also the 1999 Technical Program Co-Chair of the 54th ARFTG Conference, Atlanta, GA and he is the Vice-Chair of the RF Technical Committee (TC16) of the IEEE CPMT Society. He is a member of URSI-Commission D, an Associate Member of EuMA and a member of the Technical Chamber of Greece.

Joy Laskar (S'84–M'85–SM'02) received the B.S. degree in computer engineering with math/physics minors (highest honors) from Clemson University, Clemson, SC, in 1985. He received the M.S. and the Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, in 1989 and 1991, respectively.

Prior to joining Georgia Tech in 1995, he has held faculty positions at the University of Illinois and the University of Hawaii. At the Georgia Institute of Technology (Georgia Tech), he holds the Joseph M. Pettit Professorship of Electronics, is currently the chair for the Electronic Design and Applications Technical Interest Group, the Director of Georgia's Electronic Design Center, and the System Research Leader for the NSF Packaging Research Center. His research has focused on high frequency IC design and their integration. At Georgia Tech, he heads a research group with a focus on integration of high frequency electronics with optoelectronics and integration of mixed technologies for next generation wireless and optoelectronic systems. He has authored or co-authored more than 200 papers, several book chapters (including three textbooks in development), numerous invited talks, and has more than 20 patents pending. He is the faculty advisor for the 2000 IEEE MTT IMS Best Student Paper award. His research has produced numerous patents and transfers of technology to industry. Most recently his work has resulted in the formation of two companies. In 1998, he co-founded an advanced WLAN IC Company, RF Solutions, which is now part of Anadgics. In 2001, he co-founded a next generation interconnect company, Quellan, which is developing collaborative signal processing solutions for enterprise applications.

Dr. Laskar is a 1995 recipient of the Army Research Office's Young Investigator Award, a 1996 recipient of the National Science Foundation's CAREER Award, the 1997 NSF Packaging Research Center Faculty of the Year, the 1998 NSF Packaging Research Center Educator of the Year, the 1999 co-recipient of the IEEE Rappaport Award (Best IEEE Electron Devices Society Journal Paper), 2001 Georgia Tech Faculty Graduate Student Mentor of the year, recipient of a 2002 IBM Faculty Award, the 2003 Clemson University College of Engineering Outstanding Young Alumni Award, and the 2003 recipient of the Outstanding Young Engineer of the Microwave Theory and Techniques Society. For the 2004-2006 term, Professor Laskar has been appointed an IEEE Distinguished Microwave Lecturer for his seminar entitled "Recent Advances in High Performance Communication Modules and Circuits."

John Papapolymerou (SM'04) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1993, and the M.S.E.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1994 and 1999, respectively.

From 1999 to 2001, he was a faculty member with the Department of Electrical and Computer Engineering, University of Arizona, Tucson, and was a visiting professor with The University of Limoges, France, during the summers of 2000 and 2003. In August 2001, he joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, where he is currently an Assistant Professor. His research interests include the implementation of micromachining techniques and MEMS devices in microwave, mm-wave and THz circuits, and the development of both passive and active planar circuits on Si, GaAs, LTCC, and organic materials for high-frequency applications. He has authored or coauthored more than 70 publications, numerous invited talks, and also holds one U.S. patent.

Dr. Papapolymerou was the recipient of the 2004 Army Research Office's Young Investigator Award, the 2002 NSF CAREER Award, the 2002 Best Paper Award presented at the Third International Conference on Microwave and Millimeter-Wave Technology, China, and the 1997 Outstanding Graduate Student Instructional Assistant Award presented by the American Society for Engineering Education (ASEE), The University of Michigan Chapter.

Stéphane Pinel received the B.S. degree from Paul Sabatier University, Toulouse, France, in 1997, and the Ph.D. degree in microelectronics and microsystems from the Laboratoire d'Analyze et d'Architecture des Systemes, Centre National de la Recherche Scientifique, Toulouse, France, in 2000.

He has worked on an UltraThin Chip Stacking (UTCS) European Project for three years. He is currently a Research Engineer with the Georgia Institute of Technology, Atlanta, within the Microwaves Applications Group. He has authored and coauthored more than 70 journal and proceeding papers. His research interests include advanced 3-D integration and packaging technologies, RF packaging and RF-MEMS, SOP for RF front-end module, and SOI RF circuit design.

Dr. Pinel was the recipient of the First Prize of the SEE 1998 Award, the Second Prize of the IMAPS 1999 Award, and the 2002 International Conference on Microwave and Millimeter-Wave Technology Best Paper Award (Beijing, China).

V. Palazzari received the "Laurea" degree in electronic engineering and the Ph.D. degree from the University of Perugia, Italy, in 2000 and 2003, respectively.

She is currently a Research Engineer at DIEI, University of Perugia, Italy. Her research interests include the analysis and design of RF integrated circuits on silicon based (CMOS, SiGe BiCMOS) technologies, focusing on passive devices and medium power amplifers with application in modern telecommunications; advanced 3-D RF subsystems integration on packaging technologies in cooperation with the Georgia Institute of Technology, Atlanta, GA.

R. Li (M'02–SM'03) received the B.S. degree in electrical engineering from Xi'an Jiaotong University, China, in 1983, and the M.S. and Ph.D. degrees in electrical engineering from Chongqing University, in 1990 and 1994, respectively.

From 1983 to 1987, he worked as an electrical engineer in Yunnan Electric Power Research Institute, China. From 1994 to 1996, he was a Postdoctoral Research Fellow at Zhejiang University, China. In 1997, he was with Hosei University, Japan, as an HIF (Hosei International Fund) Research Fellow. Since 1998, he was a Professor at Zhejiang University, China. In 1999, he served as a Research Associate at the University of Utah, Salt Lake City, UT. In 2000, he was a Research Fellow at Queen's University of Belfast, U.K. Since 2001, he has been with the ATHENA group as a Research Scientist at the Georgia Institute of Technology, Atlanta, Georgia. His latest research interests include computational electromagnetics, modeling of antennas and microwave devices, and RF packaging design.

G. DeJean, photograph and biography not available at the time of publication.

N. Papageorgiou, photograph and biography not available at the time of publication.

D. Thompson received the B.S. and M.S. degrees in electrical engineering from Santa Clara University, Santa Clara, CA, in June 2001 and June 2002, respectively.

He is currently serving as a graduate research assistant and working toward his Ph.D. degree in electrical and computer engineering at the Georgia Institute of Technology. His research interests include RF front-ends on multi-layer organic substrates including antennas, filters, passives, MEMS, and packaging structures.

R. Bairavasubramanian received the B.E. (EEE) degree from Anna University, Chennai, India, in May, 2001 and the M.S.E.E. degree from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA, in December 2002. He is currently pursuing the Ph.D. degree in electrical engineering at Georgia Tech.

His research interests include development of reconfigurable phased antenna arrays on multilayer LCP substrates, as well as design and fabrication of compact RF filters and passives on organic substrates.

S. Sarkar, photograph and biography not available at the time of publication.

J.-H. Lee, photograph and biography not available at the time of publication.