3-D Thin Film Interposer Based on TGV (Through Glass Vias): An Alternative to Si-Interposer

Michael Töpper, Ivan Ndip, Robert Erxleben, Lars Brusberg, Nils Nissen, Henning Schröder,
Hidefumi Yamamoto[#], Guido Todt* Herbert Reichl

Fraunhofer Institute for Reliability and Microintegration (Fraunhofer IZM),
Gustav-Meyer-Allee 25, 13355 Berlin/Germany,
[#]NEC SCHOTT Components Corporation
3-1 Nichiden, Minakuchicho, Koka-shi, Shiga 528-0034, Japan
*SCHOTT Electronic Packaging GmbH
Product Division Automotive, Landshut, Germany

michael.toepper@izm.fraunhofer.de

Abstract

Interposers for SiP will become more and more important for advanced electronic systems. But through substrate vias are essential for the 3-D integration. Being a standard for laminate based materials this is much more complex for Si-wafers: High speed etching has to be combined with complex electrical isolation, diffusion barriers and void-free Cu-filling. Without doubt this can be solved in lab-scale but for high production scale cost is a tremendous barrier. Glass wafers with W-plugs have been intensively investigated in this paper. A new acronym has been posted to high-light this technology: TGV for Through Glass Vias. The results of modeling and simulation of TGV at RF/Microwave frequencies showed a very good compromise between wafer thickness, TGV-shape and via diameter for vertical metal plugs with 100 µm diameters in 500 µm thick glass wafer still very stable for thin film wafer processing without costly temporary wafer bonding processes. Therefore the HermeS® from Schott was chosen as the basis for a prototype of a bidirectional 4 x 10 Gbps electro-optical transceiver module. Thin film RDL and bumping of these wafers was possible without any modifications to Si-wafer. First thermal cycles showed very promising results for the reliability of this concept.

1. Introduction

Electronic packaging and assembly is the basic technology to link the small dimensions of the IC to an interconnecting substrate - usually the Printed Circuit Board (PCB) [1]. The substrate combines a number of ICs and passive components to build the final microelectronic system for the users. New applications with their expanding performance and functionality in conjunction with new device technologies are pushing the requirements and innovation for electronic packaging. Milestones for this progress have been Surface Mount Technology (SMT), Flip Chip in Package (FCIP), Flip Chip on Board (FCOB) and Wafer Level Packaging (WLP) which is evolving to System in Package (SiP) and Heterogeneous Integration (HI) by 3-D packaging.

Interposer are always used for very high-pin-count ICs like microprocessors having thousands of I/Os for the assembly on the board. Mostly these interposers are based on laminates due to cost reasons. Ceramics are only used for high reliability applications anymore. Such multilayer ceramics with multiple thin wiring layers were standard for IBM processors in the 90ties. Placing bare dies or WLPs directly on the boards requires high density wiring on the board-side. Therefore sub-module for the interchip wiring is an attractive alternative to use low cost mother boards. The idea is to have high cost technology for wiring only at the area where it is needed. This was the basis for the MCM-concept over twenty years ago [2]. The main reasons for not having success with MCM were the issue of known good die (KGD), cost and missing infrastructure like wafer bumping facilities etc. Now with the need for further integration density this idea is coming back as SiP with one important difference: The through substrate vias are required now for this interposer for 3-D stacking. This is a standard for laminate-based interposers but not for Si or other substrate materials like glass or metal. There have been hundreds of papers published in the last 10 years describing Through Silicon Vias (TSV). The reason for using Si as an interposer is the perfect match of the CTE to the ICs, the availability of the Si wafers and the wide availability of equipment for wafer processing and related infrastructure. A qualified WLP process can be used for the wiring of an interposer.

The MEMS industry has developed high speed etching processes for Si called the BOSCH-Process [3, 4]. This can be used for etching vias in Si with a wide variation of size keeping in mind to have similar via diameter on one wafer to keep the etching rate constant over the wafer. In addition the process was modified for tapered side walls now already in production for 3-D WLP of image sensors [5]. Electrical isolation and the deposition of diffusion barriers are very important for the reliability and the electrical performance of the interposer based on Si. Sputtering processes have to be modified using ionized plasma to have a reliable seed layer for the electroplating process of Cu. A void-free via filling plating process is necessary for high reliability. The plating rate is therefore limited. In addition the mechanical properties of the materials used for Si-interposer are not well fitting to each other (Table 1):

Table 1: Properties for Materials used for TSV in comparison to glass i.e. Borofloat™

Mat.	CTE [ppm/K]	E Modulus [GPa]	Poisson`s Ratio
Al	20	70	0.35
Cu	17	110	0.35
Ni	13	207	0.31
W	4.4	400	0.28
Si	2.3	130	0.28
Borofloat	3.3	64	0.2

Therefore reliability of the TSV is also a point of concern. Professor Ho from U Texas in Austin, has published that stresses inside the TSV can result in plastic deformation, stress induced voiding and stress migration [6, 7]. Maximum thermal stress is shown in Figure 1 for different materials used for TSV:

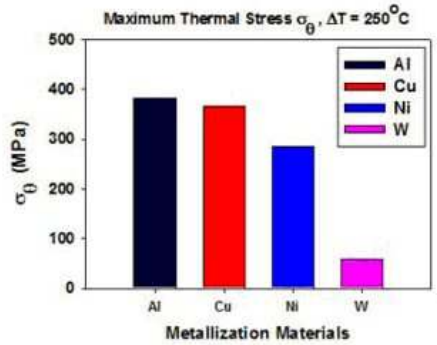


Figure 1: Maximum thermal stress of TSV [7]

Therefore the three main issues for using Si is the nature of Si itself not to be a good conductor or isolator, the large difference in CTE between Cu or Ni and Si and the contradiction that thick Si is needed for a stiff interposer but thin Si is preferred for cost reasons. After studying the cost of ownership models of IMEC, Sematech and EMC-3D, Qualcomm derived its own preliminary economics and determined that the overall cost is dominated by post-fab backside processing [8]. One of the technical conclusions the company reached from its cost modeling is that "thinner is better" — going from 50 µm to 20 µm thick layers could reduce the TSV module portion of the total cost by as much as 25% if the added thin wafer handling costs were not substantial.

Therefore Si as an interposer is only an option if thousands of TSV per module is needed. In addition passive components have to be integrated using thin film technology to valid the high processing cost [9]. For lower amount of interconnects to the board glass wafer as an interposer can be a very interesting alternative. The function of such an interposer should be a sub-module reducing the number of interconnects to the board by interconnecting several active and passive components to each other.

The main advantage of glass as a material is the excellent high frequency properties which will be discussed in this paper together with options for Through Glass Vias (TGV). The advantages will be highlighted in a demonstrator (a parallel optoelectronic transceiver) which will be discussed more in details by Brusberg et al. [10].

2. Characterization of Glass types

Glass wafers can be made out of different materials and different processing capabilities to meet custom specific requirements [11]. Different materials are necessary for different physical and chemical requirements which are required by different applications. For example glasses which have to be combined with a silicon wafer (wafer bonding or FC) require a CTE of around 3.2 ppm K^{-1} to avoid a CTE mismatch. Glass wafers are fully compatible to WLP-Lines. There is no difference between processing Si-Wafers compared to Glass-Wafers except the lower thermal conductivity which requires optimization for hot-plate processes. The wafers are available with edge treatment with C- or facet shape. Down draw material can be used without additional surface treatment, while the other glass types require a surface treatment (grinding, lapping, polishing) to meet surface quality requirements. 500 µm thick wafer of down draw material with fire polished surface have typically 300 µm warp, < 10 µm TTV and surface roughness below 1 nm. Lapped and polished quality can go down to 80 µm warp, 2 µm TTV and < 1nm surface roughness [11].

Borofloat33 has a low specific weight in comparison with soda-lime glass. In addition the CTE matches to silicon ICs which is beneficial to high reliability of solder joints. The integration of optical functions inside the substrate using the ion-exchange technology requires a high alkaline content (D263™T eco, B270™). The properties of the glass types used in this project are summarized in Table 2 [11]:

Table 2: Properties of glass types used in this project

Name	Lithosil	BORO-FLOAT 33	D 263 T	B 270	AF 32 eco
Type	fused-silica	boro-silicate	boro-silicate	crone glass	al-boro-silicate
Process	SiO_2 Ingot produced by a flame-hydrolytic process	micro-float	down-draw	up-draw	down-draw
Alkaline content	alkali-free	4 wt%	13 wt%	17 wt%	alkali-free
CTE [ppm/K]	0.5	3.3	7.2	9.4	3.2

All glass types are available as wafers (100 mm to 300 mm) in easy-to-handle thickness of 400 to 500 µm or even thicker. In addition AF32, AF45 and D263 can go down to 50 µm which would require temporary bonding to handling wafers. In this paper we will focus on an interposer concept which is using wafers having enough mechanical stability. Therefore we have chosen 500 µm thick glass wafers with 100 mm diameter to reduce R&D cost for the mask sets.

3. Via formation in Glass

Glass vias can be made using the following technologies [12]:

a) ultra sonic drilling
b) ultra sonic high speed drilling (USHD)
c) sand blasting

d) wet etching
e) dry etching
f) laser drilling

The mechanical processes for opening the glass vias in 500 µm thick wafers are mostly not suitable for dimensions in the range of 100 µm diameter or below. Foturan is a photo-structurable glass ceramic (PSGC) manufactured by Schott Glass Corp and distributed by Invenios [13]. The PSGC is exposed using mask aligner or laser followed by a high temperature treatment (600°C). The UV-light induces crystallization in the exposed area which have a much higher etch rate in HF-solutions. Similar glasses are available from Corning (Fotoform) and von Hoya (PEG-3). The required dimensions for TGV are hard to reach for 500 µm thick glass wafers. Dry etching using DRIE is also not suitable for thick wafers due to the much slower etching rate of glass compared to Si. An optimized process using a SF_6 plasmas showed a glass etch rate of only ≅750 nm/min which is not an option for interposers with 500 µm thickness [14].

Xiaoyun Cui et al from Loughborough University, UK [15] published excimer laser drilling of the glass and electroless copper plating together with direct bonding experiments to bond the different thin glass layers onto each other.

Opening the glass via is of course only part of the TGV process. The metallization has to be done afterwards. There are two technologies which use a totally other approach which are compared to the other alternatives mentioned above (Figure 2):

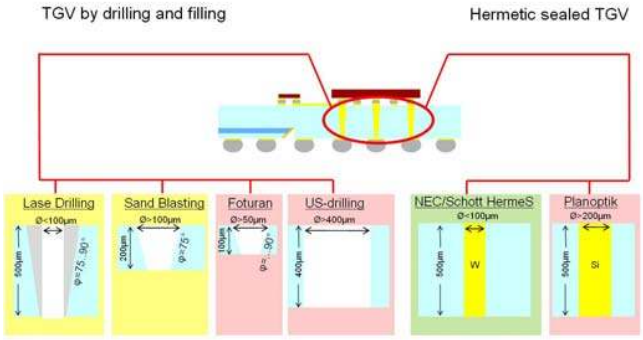


Figure 2: Technologies for TGVs

The process of PlanOptik is using highly doped silicon inside borosilicate glass [16]. Examples are shown in Figure 3:

Dimensions of the TGV are:

Minimum pin dimension: 50 microns
Minimum insulation width: 50 microns
Wafer thickness: 200...500 microns

The resistance of the TGV is in the range of 3 x 10^{-3} ohm cm.

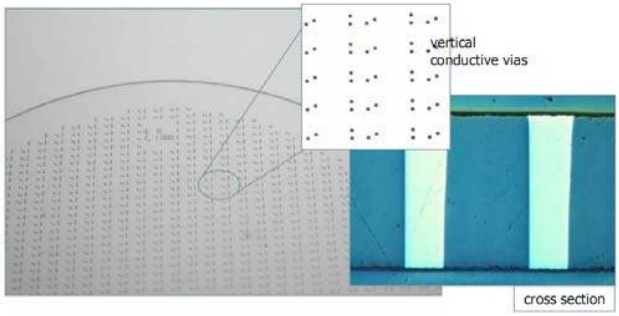


Figure 3: TGV done by a Si/Glass process (courtesy of PlanOptik AG)

A technology using metal as a conductive material for the wiring through the glass has been published by Schott/NEC [17]. The approach from Schott is an additive technology: Glass is melted over W-plugs which eliminate all drilling and filling processes. The technology is currently available as 4-inch and 6-inch wafers. 200 mm is under progress. The metal vias are made of tungsten that can be 100 µm in diameter with a spacing of 250 µm. Finer pitch is under development. An example of such a wafer is shown in Figure 4:

Figure 4: An example of a glass wafer with TGV using W-plugs (courtesy of Schott)

	fs-Laser	Foturan	Powder plasting	US drilling	Thermal sheet molding	HermeS
Size	standard	standard	Max. 400x400mm²	standard	Max squares 700mm & 8"-wafers	4", 6", 8"
Structuring angle	free	Ca. 90°	75° ± 5°	Ca. 90°	between 2° and 90°	-
Shape	Holes and cavities	Holes and cavities	Holes and cavities	Holes only	Holes and cavities	Contact pin
Outline shape	Free shape (holes, squares, lines, etc.)	Free shape (holes, squares, lines, etc.)	Free shape (holes, squares, lines, etc.)	Round shape only	Free shape (holes, squares, lines, etc.)	Contact pin
Min structure @ max. thickness	75µm @ 500µm	50µm @ 100µm	100µm @ 200µm	0.4 mm @ 400µm	100µm @ 500µm	100µm @500µm

Figure 5: Comparison of forming TGVs

The positioning accuracy is approximately ±50 micrometers. Theoretically, this allows for substrates with several 10,000s of TGVs. In addition the wafer with the W-plugs are hermetically sealed (< 1 x 10^{-8} mbar m^3/s). The electrical resistivity of the metal plugs corresponds to W: 5.5. x 10^{-6} ohm cm. The technology is commercialized under the trade name HermeS.

The different technologies are summarized in Figure 5:

To select the right technology a simulation at RF/Microwave frequencies for different via geometries was done.

4. Modeling and Simulation of TGV at RF/Microwave Frequencies

The formation of through holes vias is essential for an interposer. To provide an optimal via configuration, the influence of the geometrical properties on the signal transmission were investigated. The investigated geometrical parameters are the substrate thickness, the via diameter and the shape of the via (conical or cylindrical). Due to the complicated configuration of the via, the analysis was performed using 3D full-wave electromagnetic simulations.

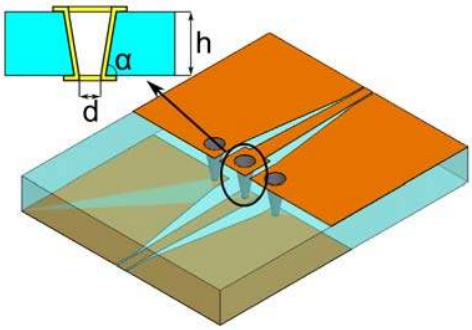


Figure 6: 3D Model of Coplanar Via Configuration

In Figure 6, the 3D model of the via configuration used in the simulations is shown. In the upper left hand corner the three most important parameters of the single via are depicted.

To account for the via length, the substrate thickness was varied in three steps (100 µm, 200 µm and 500 µm) . The via diameter and the via angle were kept constant d = 50 µm and α = 90°. The transmission coefficient shows no significant difference. Only resonances due to the overall transmission path length shift to lower frequencies for thicker substrates.

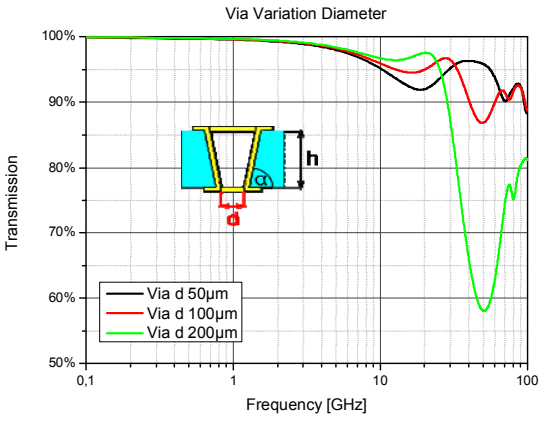


Figure 7: Relative transmission simulation results versus frequency for three different TGV diameter d (50 µm, 100 µm and 200 µm)

To investigate the impact of the via diameter d, three values (50 µm, 100 µm and 200 µm) were assigned while the other variables were kept constant at h = 500 µm and α = 90°. The results (Figure 7) reveal that this variation in via diameter has no significant impact on the insertion loss of the via up to 10 GHz. Beyond this frequency, the insertion loss of the 200 µm via degrades severely (approx. 60% of power is transmitted @ 50 GHz). The transmission coefficients of the 50 µm and the 100 µm via remain above 85% over the whole bandwidth.

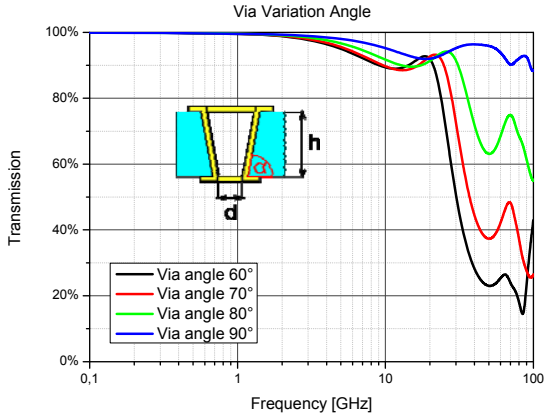


Figure 8: Relative transmission simulation results versus frequency for three different TGV angle α (□□60°, 70°, 80° and 90°)

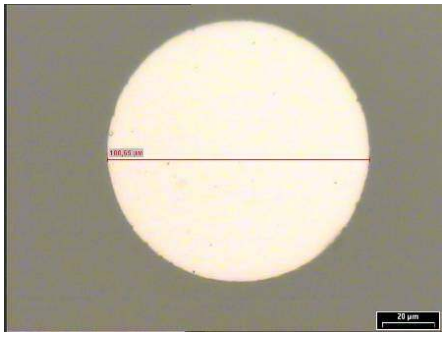


Figure 9: Video photo of a W-plug inside a glass wafer

The via angle α was varied in four steps (60°, 70°, 80° and 90°). The via diameter and the substrate thickness are d = 50 µm and h = 500 µm. Below 20 GHz the dependence on the transmission behavior is low. Above this frequency the transmission decreases for decreasing angle (approx. 23% of power is transmitted @ 40 GHz for α = 60°).

Therefore straight vertical vias are strongly preferred over tapered vias.

The optimal compromise for all requirements of a glass interposer is therefore the approach from Schott using W-plugs sealed into glass wafers. In the following this technology will be used for our further investigations.

5. Glass Interposer with TGV

Inspection of the W-plugs of each HermeS wafer was done using optical inspection (Figure 9).

The diameter of the pins was very uniform. Mean value was 100 µm with a variation below 1 µm. Next the surface step between plug and glass wafer was investigated using surface profilometer (Figure 10):

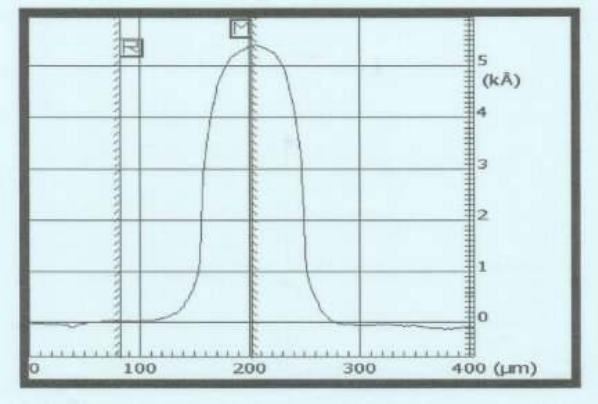


Figure 10: Altitude difference between plug surface and glass wafer

Altitude difference between glass and pin surface is 500 nm. This low altitude difference of HermeS pin and glass surface is not a limiting factor for thin film processing. No modification of the thin film wiring process of Fraunhofer IZM has to be done.

First measurements of the positions of the 100 µm pins result in a 50 µm tolerance. To ensure that is all pins are covered by the wiring of the front side and the UBM at the back-side we used capture pads being a bit larger than the pins. With a CD-measurement tool from Nikon the all positions of the wafers (both sides) were check with respect to the design file. The positions of 20 pins are shown in Figure 11 in comparison to the design file of 200µm capture pads:

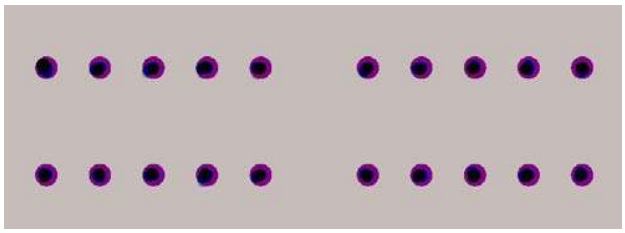


Figure 11: Run-Out measurement of pin location compared to design file (blue pads)

Of course increasing the capture pad size reduces the integration density, but a full coverage of the pins with a sputtered metallization is necessary to avoid any corrosion or other leakages during thin film processing.

The connection to the W-plugs and the rewiring metallization consist of electroplated gold or copper traces to achieve a low electrical resistivity. A sputtered layer of Ti:W-Cu (200/300nm) or TiW-Au serves as an adhesion barrier to the glass and as a plating base. A positive acting photo resist is used to create the plating mask. The thickness of the plated metal was 10 µm. After metal deposition the plating base is removed by a wet etching. We compared sputtered Cr and TiW as an adhesion layer to glass using the stud pull tester ROMOLUS III from Quad Group. Both sputtered layers had a better adhesion than the expoxy used to fix the pull tester to the metal surface (70 - 90 MPa). Therefore we used TiW due to the better etching process of the plating base.

6. Wafer bumping

Bumping of the glass interposer is essential for the next level of interconnection to the board. For reliability reasons the bumps should have a diameter of > 200 µm. Two technologies are therefore possible: Solder paste printing and ball drop. We have evaluated the ball drop process using a combination of flux printing and ball placing through a stencil (Figure 12):

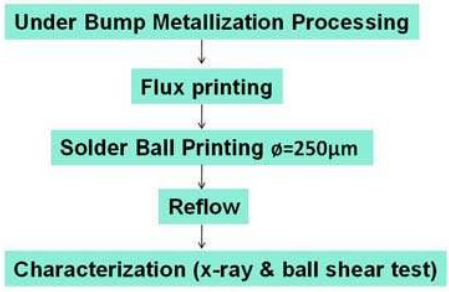


Figure 12: Process flow for wafer bumping of glass interposers with TGVs

The UBM has been deposited using sputtering Ti:WCu and plating Ni with a flash of Au. No modifications for the ball drop has to be done compared to CMOS wafer bumping for WLP. Results are shown in Figure 13:

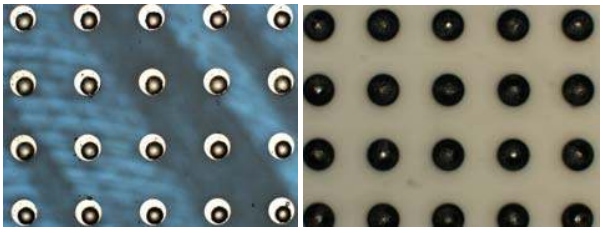


Figure 13: Printing flux on UBM TiW/Cu/Ni of glass wafer with TGV (left) and ball placing (right)

Bump quality was checked using SEM and FIB (Figure 14) and x-ray analysis (Figure 15:)

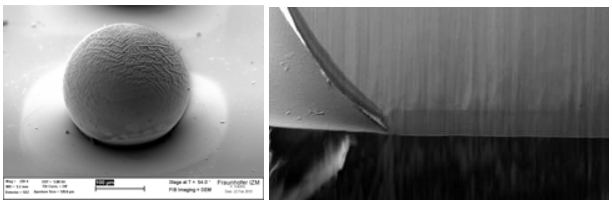


Figure 14: SEM (left) and FIB (right) of ball on glass interposer with TGV

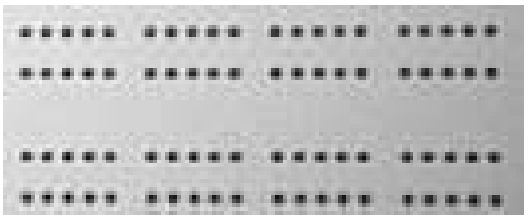
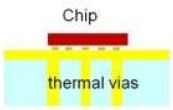


Figure 15: X-Ray inspection of bumped glass wafer with TGV

Adhesion of the bumps on the W-plugs with the UMB was tested using shear testing. Shear height was 15 µm (well above the UMB of 5 µm Ni). Shear force was in a range between 250 gForce to 320 gForce. Shear mode was always shearing through the bump. The UBM was very stable on the W-plug. Mean shear force after 250 cycles (-55°C/+125°C) was 215 gForce. Further results will be presented at the conference.

7. Thermal calculation

The thermal conductivity of glass is less than for silicon or ceramics. Therefore, even with high efficiency components the removal of heat is a challenge for such interposer concepts based on glass. A very high efficient heat spreading has to be considered. To achieve a usable level of heat spreading the top metallization needs to be thick enough and should be designed to have as much metal as possible under and around the ICs. In addition thermal vias, either below the large ICs or in a fan-out configuration has to be considered. This approach has merit, if a thermal sink can be accessed below the mounting area of the glass module. A brief calculation of the thermal vias is summarized in Figure 16:



Via	Thermal resistance [K/W] 1 Via	Thermal resistance [K/W] 10 Vias
∅500µm with 10µm thick Cu	85	8.5
∅100µm HermeS W-Plugs	381	38.1
∅500µm HermeS W-Plugs	15	1.5

Figure 16: Brief calculation of thermal TGVs

Metal plugs with larger diameter are necessary for components with higher thermal dissipation on such glass interposers. A potential layout of such a configuration is shown in Figure 17:

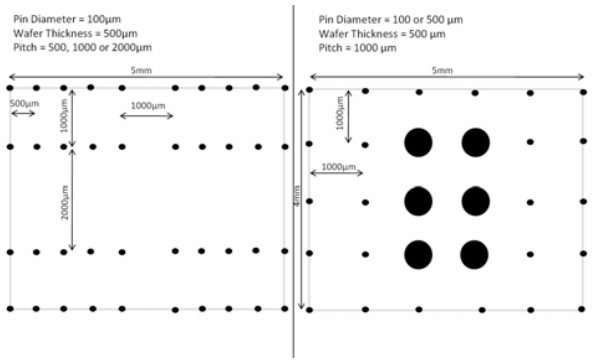


Figure 17: Layout of an interposer with thermal TGV having different diameter

The coexistence of W-plugs with different diameter like 100 µm and 500 µm would be highly beneficial und is under development. For low power components this would be not necessary.

It should be mentioned here that TSV with a large difference in diameter are difficult to etch in Si due to the relation of etching speed (DRIE) to via diameter.

8. Demonstrator for the glass interposer with TGV

The demonstrator was a four channel bi-directional optoelectronic transceiver module. The transceiver operates with 10 Gbps per channel and has an extremely low power consumption of 592 mW. The module is mounted on a printed circuit test board and the performance is characterized by bit error rate testing. The layout of the module and the processed 3-D glass interposer with TGVs (pitch 475 µm) is shown in Figure 18 and Figure 19:

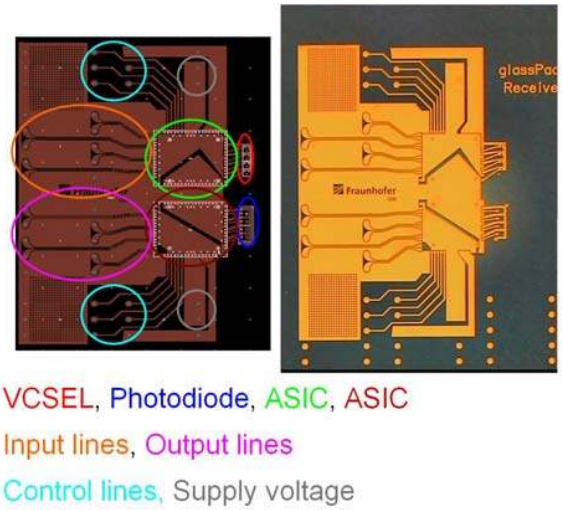


Figure 18: Design and processed 3D-Glass-Interposer

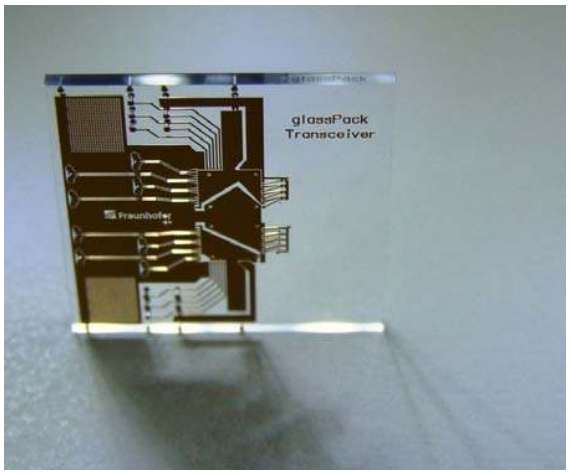


Figure 19: Singulated glass interposer with TGVs

After thin film processing the Hemes® wafer were diced. The ICs and optoelectronic components were stud bumped and thermal compressive (TC) bonded on the glass interposer. For testing purposes, the electrical circuit on the glass interposer was bonded by anisotropic conductive adhesive (ACA) onto the test board. The test board material was Rogers 4350B with a metallization of 35µm Cu and e-less. Ni/Au. Board size was 81.90 x 173.60 mm². (Figure 20). In a parallel process, the optical layer was processed by ion-exchange waveguide integration and micro-polishing of the optical mirror. The MT-connector was attached and the optical layer actively aligned and adhesively bonded below the electrical layer [10].

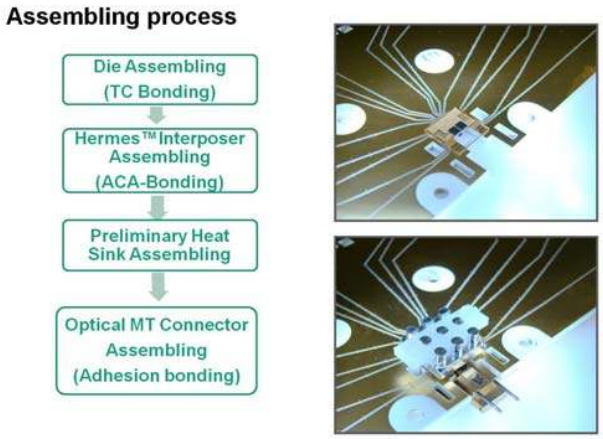


Figure 20: Assembly process of the 4x10Gbps bidirectional electro-optical transceiver module

For bit error rate testing, we used an Opnext XFP transceiver module which was optically interconnected by a pair of fiber to the MT-connector of our demonstrator. For electrical interconnection to signal, control and power supply the interposer was mounted on the test board by ACA bonding as described above. The bit error rate testing was performed at a data rate of 10 Gbps. The data transfer of all four channels of the transmitter as well as for all four channels of the receiver could be successfully performed.

9. Conclusion

The feasibility of glass interposers with TGVs has been demonstrated. Glass is available in wafer quality comparable to Si. Via formation through the glass should be done in a process avoiding drilling and metal filling. Therefore the glass interposers HermeS have been successfully tested for a 4 x 10 Gbps bidirectional electro-optical transceiver module. The thin film processing was done according to WLP standards.

A further step to higher integration will be the combination of glass wafers with TGVs and a fully polymer-free multi-layer metallization. The electrical isolation between the metal-layers will be also thin glass. The deposition of the glass can be done by a plasma-assisted e-beam evaporation process [18]. It is a high rate deposition process with deposition rates above 200 nm/min and at the same time low substrates temperature. With the high deposition rate typical film thicknesses of 3 – 10 µm can be achieved easily and production can be run as a cost effective batch process depending on the required uniformity. The glass layer can be microstructured by lift-off. Since the deposition process is working at low temperatures standard photo resists can be used for masking. An example of such a multilayer is shown as a cross cut in Figure 21:

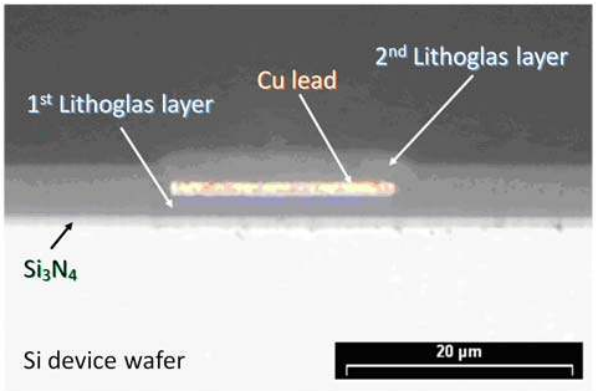


Figure 21: Multilayer Cu/Glass [18]

The final step for a fully hermetic SiP using glass interposers with TGVs is the soldering of a glass cap on top shown in Figure 22:

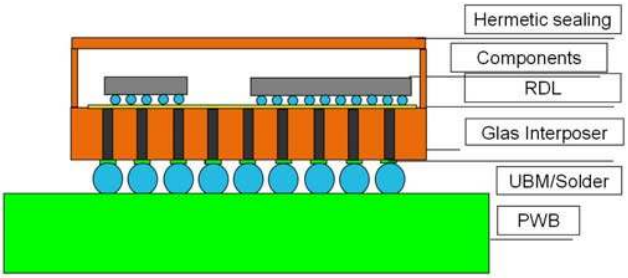


Figure 22: Fully hermetic SiP based on glass interposer

Such a structure is under development at Fraunhofer IZM. The advantage is the lack of any temperature sensitive materials for the built-up. Therefore it can be used for harsh

environment applications even at higher temperatures (>150°C).

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