30–100-GHz Inductors and Transformers for Millimeter-Wave (Bi)CMOS Integrated Circuits

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***Abstract*—Silicon planar and three-dimensional inductors and transformers were designed and characterized on-wafer up to 100 GHz. Self-resonance frequencies (SRFs) beyond 100 GHz were obtained, demonstrating for the first time that spiral structures are suitable for applications such as 60-GHz wireless local area network and 77-GHz automotive RADAR. Minimizing area over substrate is critical to achieving high SRF. A stacked transformer is reported with S_{21} of −2.5 dB at 50 GHz, and which offers improved performance and less area ($30\ \mu\text{m} \times 30\ \mu\text{m}$) than planar transformers or microstrip couplers. A compact inductor model is described, along with a methodology for extracting model parameters from simulated or measured y-parameters. Millimeter-wave SiGe BiCMOS mixer and voltage-controlled-oscillator circuits employing spiral inductors are presented with better or comparable performance to previously reported transmission-line-based circuits.**

***Index Terms*—Inductors, millimeter wave, mixer, self-resonance frequency (SRF), stacked inductors, transformers, voltage-controlled oscillator (VCO).**

I. Introduction

RECENTLY, silicon technologies have become a viable option for millimeter-wave and high-speed digital circuits with data rates above 40 Gb/s. The potentially large consumer markets have attracted considerable interest in 60-GHz wireless local area network (WLAN) and 77-GHz collision avoidance automotive RADAR, resulting in 60-GHz low-noise amplifiers (LNAs), power amplifiers, and mixers [1], and 80-GHz voltage-controlled oscillators (VCOs) [2] implemented using SiGe HBT technologies. Furthermore, the demonstration of very high-speed SiGe HBT digital building blocks [3] paves the way for highly integrated serial communication transceivers with data rates exceeding 100 Gb/s. Wireless and wireline building blocks reported to date that operate in the millimeter-wave regime rely on microstrip transmission lines for on-chip matching networks and inductive peaking. However, this approach proves to be area intensive, as quarter-wavelengths in silicon dioxide at 60 and 80 GHz are approximately 630 and 470 μm, respectively. Given the prohibitive mask and fabrication costs in the deep-submicrometer technologies at which silicon becomes commercially feasible for millimeter-wave circuits, area consumption should be minimized if inexpensive components are to be realized. While monolithic spiral inductors and transformers have been very popular in silicon-based technologies at microwave frequencies, their application in millimeter-wave circuits has not been investigated. Mutual coupling in spiral coils allows for larger inductance in less area than transmission-line structures. Furthermore, the increasing number of metal layers available in (Bi)CMOS technologies facilitates the design of three-dimensional (or stacked) inductors and transformers reminiscent of discrete components found at lower frequencies.

This paper reports inductors and transformers suitable for millimeter-wave applications [4]. Design guidelines for planar and stacked millimeter-wave inductors are described in Section II. Section III examines planar and stacked millimeter-wave transformer structures. A stacked transformer is introduced that is ideal for single-ended-to-differential conversion above 40 GHz. A wide-band inductor model is presented in Section IV, along with a methodology for model parameter extraction. Finally, as examples of millimeter-wave circuits employing spiral inductors, the first dc-to-50-GHz broad-band mixer and the first inductor-based 40-GHz VCO are reported in Section V.

II. Inductors

A. Millimeter-Wave Design Considerations

For silicon-based inductors in the millimeter-wave regime, loss in the silicon substrate is the dominant mechanism for degradation in the quality factor [5]. We propose that, to minimize these losses, an inductor footprint be made as small as possible. This involves reducing outer diameter, as well as metal linewidth. While inductor design at radio frequencies emphasizes the use of wide metal lines to reduce series resistances, this approach increases capacitance to substrate and reduces the self-resonance frequency (SRF). Circuits employing inductors should operate below the peak-Q frequency of the inductor in order to ensure proper behavior, which emphasizes the need for high SRF. In our designs, reliability concerns due to dc electromigration effects set the lower limit on linewidth. Turn-to-turn spacing is made roughly equal to the dielectric thickness to substrate to lessen the impact of interwinding capacitances and further improve SRF. Wide metal spacing also diminishes

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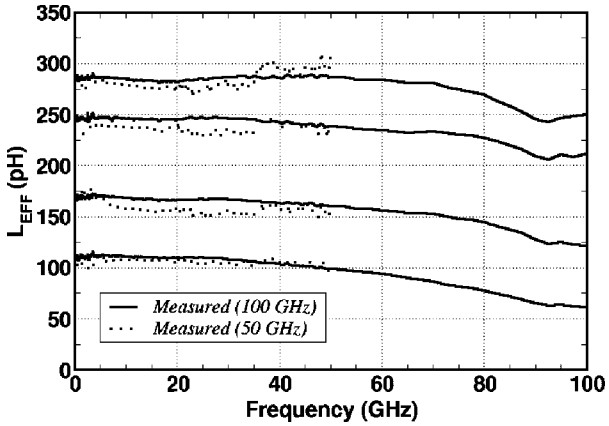

Fig. 1. $L_{\rm EFF}$ for planar millimeter-wave inductors measured using 50- and 100-GHz network analyzers.

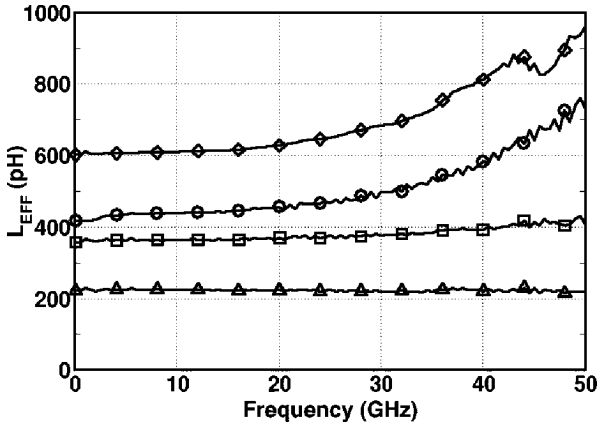

Fig. 2. Measured $L_{\rm EFF}$ versus frequency for 200-, 370-, 400-, and 600-pH millimeter-wave stacked inductors.

TABLE I
DESIGNED VERSUS MEASURED PLANAR INDUCTOR PERFORMANCE

DUT	Outer Diameter	L_{EFF} @ 40 GHz (Measured/ASITIC)	SRF (ASITIC)
D1	49 μm	290 pH / 270 pH	159 GHz
D2	46 μm	168 pH / 156 pH	221 GHz
D3	39 μm	239 pH / 241 pH	170 GHz
D4	30 μm	115 pH / 101 pH	334 GHz

the frequency dependence of the inductance set forth by the proximity effect [6].

B. Planar Inductors

Based on the discussion in Section II-A, a family of square and symmetric [7] planar inductors was designed using ASITIC [8] and implemented in a six-layer copper CMOS back-end [9]. Inductance values range from 100 to 300 pH with outer diameters between 30–50 μm. Inductors were measured up to 100 GHz in Crolles, France, and up to 50 GHz in Ottawa, ON, Canada. Cable and probe losses are corrected using load-reflect match (LRM) calibrations with the network analyzer. Furthermore, y-parameters for open and short test structures are measured and deembedded to correct for pad capacitances, lead inductances, and lead resistances, which can add on the order of 40 fF, 50 pH, and 1 Ω, respectively, to each port. Fig. 1 demonstrates the effective inductance measured using the 50- and 100-GHz network analyzers and extracted as

$$L_{\rm EFF} = \frac{\mathrm{Im}\left\{y_{11}^{-1}\right\}}{\omega}. \tag{1}$$

In all cases, the measured inductance was within $\sim$5% of the target value, as summarized in Table I. Slight dips in $L_{\rm EFF}$ are seen close to 90 GHz in all cases, which underscore the difficulty in measuring and deembedding such small inductance values at very high frequencies. Measurements indicate that the SRF is well beyond 100 GHz in all cases. To the authors' best knowledge, this marks the first verification of ASITIC in the millimeter-wave regime.

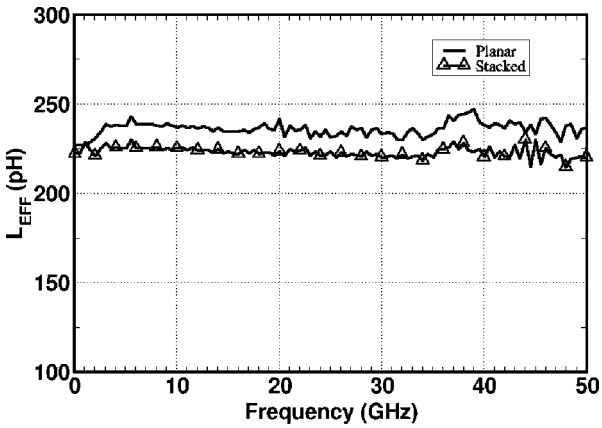

Fig. 3. Measured $L_{\rm EFF}$ for 220-pH planar and stacked millimeter-wave inductors.

C. Stacked Inductors

Further reduction in area is achieved using three-dimensional structures [10]. These structures benefit from strong mutual coupling between vertically adjacent metal layers, and can generate the same inductance in less area as compared with planar inductors. Stacked inductors implemented in two or three metal layers were designed with inductance values between 200–600 pH and with outer diameters ranging from 20 to 40 μm. $L_{\rm EFF}$ extracted from measured 50-GHz data is presented in Fig. 2.

Effective inductances for a planar and stacked inductor with respective outer diameters of 36 and 18 μm are shown in Fig. 3. In both cases, self-resonance is beyond the measurement capability. Results indicate that comparable inductance ($\sim$220 pH) in the millimeter-wave regime can be obtained using stacked inductors with significant area reduction over planar inductors. A die photograph of the 220-pH stacked inductor, with two turns in metal 6 and two turns in metal 5, is presented in Fig. 4.

As with planar inductors, reducing area over substrate is paramount in increasing the SRF of stacked inductors. Two stacked inductors of similar inductance were designed, the first using the top two metal layers with an outer diameter of 30 μm and the second using the top three metal layers with a 21-μm diameter. The smaller inductor footprint results in an improved SRF,

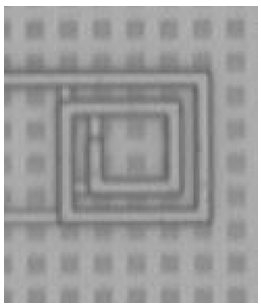

Fig. 4. Die photograph of 220-pH two-metal stacked inductor. Inductor is formed with two turns in metal 6 and two turns in metal 5. The outer diameter is 18 μm.

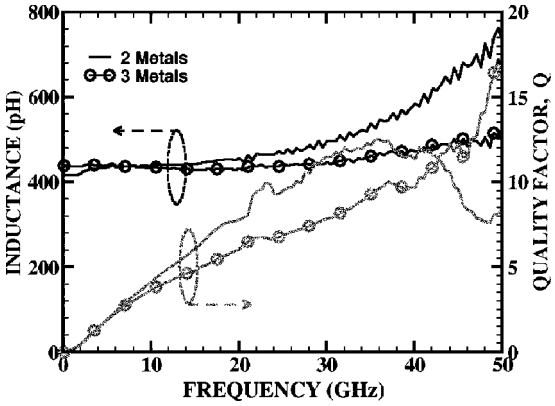

Fig. 5. Measured $L_{\rm EFF}$ and Q of 420-pH stacked inductors implemented in two and three metal layers.

as seen in the measured $L_{\rm EFF}$ of Fig. 5. The nearly 50% reduction in total area with more metal layers yields higher SRF, even though the bottom metal layer is slightly closer to the substrate. The effective inductor quality factor is extracted as

$$Q_{\rm EFF} = \frac{\rm Im\{-y_{11}\}}{\rm Re\{y_{11}\}} \tag{2}$$

It is noted that attempts to implement stacked inductors at lower frequencies (below 10 GHz) have resulted in low quality factors, on the order of 2–3 [11] due to additional via resistance. However, as seen in Fig. 5, the quality factor for millimeter-wave inductors is actually improved by adding more metal layers. While the two-metal inductor has a peak Q of approximately 13, the Q of the three-metal inductor exceeds 15 and has yet to peak at 50 GHz. This underscores the importance of minimizing substrate losses, not series losses, to improve inductor performance at frequencies above 10 GHz.

D. Impact of CMP Integrity Fill

In sub-0.18-μm production technologies with multimetal backends, dummy metal patterns (as seen from the die photograph in Fig. 6) are required to preserve chemical mechanical planarization (CMP) integrity. While placement of these structures is usually automated by computer-aided design (CAD) tools, the layout designer can often specify an exclusion region to prevent dummy fill from being generated in or around inductors. Test structures were designed to assess the impact of varying the spacing of dummy fill from a 160-pH square inductor. Less than 5-pH variation, well within the measurement

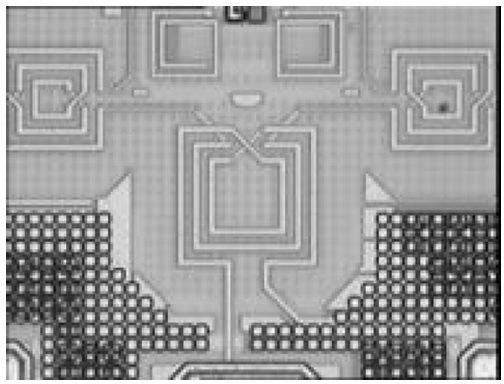

Fig. 6. Metal fill patterns for chemical–mechanical planarization integrity near millimeter-wave inductors and transformers in a production 0.13-μm SiGe BiCMOS technology.

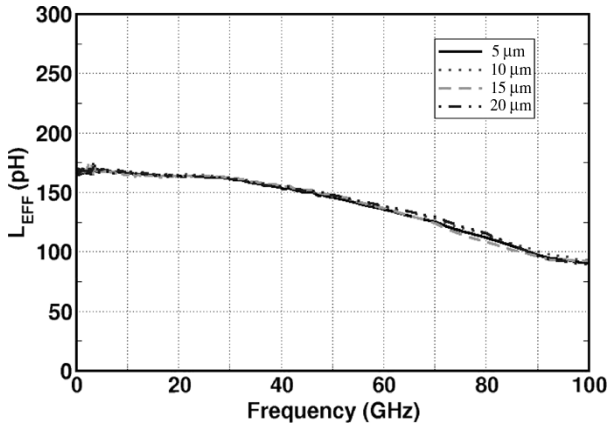

Fig. 7. Effect of fill pattern proximity on measured $L_{\rm EFF}$.

accuracy, is observed (Fig. 7) as the distance from inductor edge to fill pattern is changed. Reducing fill proximity eases layout requirements for circuits employing inductors in state-of-the-art silicon technologies.

III. Millimeter-Wave Transformers

While differential circuit topologies are vital to improve noise immunity in integrated circuits, they often call for the generation of differential signals from single-ended sources. High-speed current-mode logic (CML) or emitter coupled logic (ECL) digital circuits require differential clocks, but only single-ended signal generators are available above 40 GHz. In a wireless system, a single-ended-to-differential converter between a single-ended LNA and a doubly balanced mixer must have low loss to mitigate its impact on the noise figure of a receiver. At lower frequencies, conversion can be achieved via an active balun, or a differential pair with the unused input terminated off chip. However, at millimeter-wave frequencies, poor common-mode rejection renders this approach ineffective, as the differential outputs exhibit amplitude mismatch and phase misalignment. While other approaches have relied on a rat-race coupler for conversion at 80 GHz [12], the area occupied by such a coupler is substantial $(250\ \mu{\rm m} \times 800\ \mu{\rm m})$. An on-chip transformer is ideal for single-ended-to-differential conversion, but has not been attempted in the millimeter-wave regime.

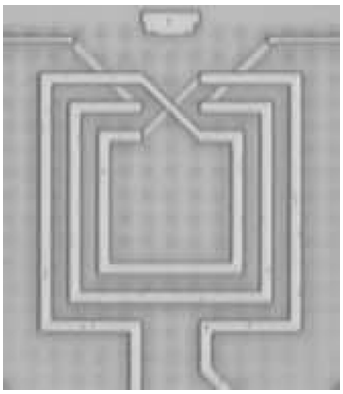

Fig. 8. Die photograph of millimeter-wave planar transformer. Outer diameter is 45 μm.

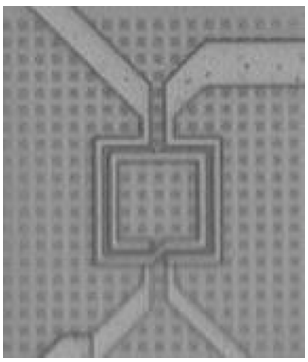

Fig. 9. Die photograph of millimeter-wave stacked transformer. The primary is formed in metal 6 with metal 5 crossovers, while the secondary is formed in metal 4 with metal 3 crossovers. Outer diameter is 30 μm.

Two transformer structures have been investigated for millimeter-wave applications. The first, a planar transformer, employs symmetrical inductors for the primary and secondary, as seen in the die photograph of Fig. 8. Both windings are formed in metal 6 with metal 5 crossovers. To ensure adequate SRF in the primary and secondary, the design follows the guidelines set forth in Section II. This transformer, with an outer diameter of 45 μm, has been utilized to generate differential 43-GHz clocks from a single-ended signal source in a 43-Gb/s decision circuit [13]. However, the coupling coefficient predicted by ASITIC is only 0.5.

Higher coupling can be achieved through the use of stacked structures. A second transformer was implemented by vertically stacking two symmetrical inductors, each with two turns. The primary is formed in metal 6 with metal 5 crossovers, while the secondary is formed in metal 4 with metal 3 crossovers. The outer diameter of the stacked transformer shown in Fig. 9 is 30 μm, making it more area efficient than the planar structure while achieving a higher ASITIC-predicted coupling coefficient $(k = 0.75)$. While test structure layout prevents a comparison of differential transformer outputs, excellent phase and amplitude matching is expected due to the perfect symmetry of the layout. Fig. 10 compares the measured and simulated input–output coupling S_{21} of both transformers. The stacked transformer has approximately 5-dB better coupling than the planar transformer over the measured frequency range. Furthermore, the low loss

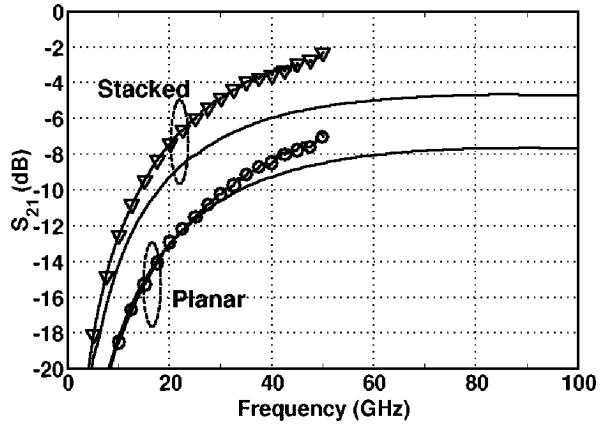

Fig. 10. Measured (symbols) and ASITIC-simulated (lines) coupling of millimeter-wave stacked and planar transformers.

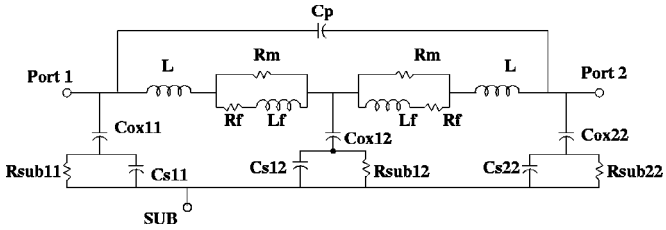

Fig. 11. Compact broad-band inductor model.

(−2.5 dB at 50 GHz) makes this structure well suited for wireless applications.

IV. Compact Modeling

A. Inductor Equivalent Circuit

Accurate inductor and transformer modeling is essential to successful millimeter-wave circuit design. It is imperative that a model not only capture all relevant energy loss mechanisms, but also accurately represent the equivalent capacitances. Inadequate capacitance modeling leads to poor prediction of the SRF and, when applied to millimeter-wave *LC* tuned circuits, can shift center frequencies by at least 10%. A single-π equivalent circuit is inadequate, as half of the capacitance to substrate is artificially neglected in simulations if one terminal of the inductor is connected to a small-signal ground. Instead, the distributed nature of the spiral structure is better described by the double-π equivalent circuit of Fig. 11 [6].

For the model to be applicable over wide bands, the frequency dependence of the various loss mechanisms must be accurately captured. At millimeter wavelengths, the substrate must be modeled as a distributed *RC* network, as the period of the wave is less than the dielectric relaxation time of the substrate. This is true for all frequencies above approximately 15 GHz on a 10-$\Omega \cdot$ cm silicon substrate. Furthermore, the skin effect confines carriers to the surface of the conductor, leading to increased loss at high frequencies. This can be modeled by a ladder network consisting of L_f and R_f shunting R_m. Additionally, series losses are exacerbated by current crowding due to the proximity effect. As mentioned in Section II, turn spacing is increased in millimeter-wave inductors to lessen the impact of the proximity effect.

Model parameters for the double-π equivalent circuit are obtained by direct extraction from ASITIC simulations, or from measurements, as follows. At low frequencies (less than 1 GHz), series inductances and resistances are extracted from y_{12} as

$$L_{\rm DC} = \frac{\rm Im\left\{-y_{12}^{-1}\right\}}{\omega} \tag{3}$$

and

$$R_{\rm DC} = \rm Re\left\{-y_{12}^{-1}\right\}. \tag{4}$$

Oxide capacitances and substrate resistances for a single-π equivalent circuit are extracted as

$$C_{\rm OX1} = \frac{\left[\rm Im\left\{\frac{1}{y_{11}+y_{12}}\right\}\right]^{-1}}{\omega} \tag{5}$$

$$C_{\rm OX2} = \frac{\left[\rm Im\left\{\frac{1}{y_{22}+y_{21}}\right\}\right]^{-1}}{\omega} \tag{6}$$

$$R_{\rm SUB1} = \rm Re\left\{\frac{1}{y_{11}+y_{12}}\right\} \tag{7}$$

and

$$R_{\rm SUB2} = \rm Re\left\{\frac{1}{y_{22}+y_{21}}\right\}. \tag{8}$$

The corresponding double-π parameters can then be readily determined as follows:

$$C_{\rm OX11} = \frac{C_{\rm OX1}}{2} \tag{9}$$

$$C_{\rm OX22} = \frac{C_{\rm OX2}}{2} \tag{10}$$

$$C_{\rm OX12} = C_{\rm OX11} + C_{\rm OX22} \tag{11}$$

$$R_{\rm SUB11} = 2 \cdot R_{\rm SUB1} \tag{12}$$

$$R_{\rm SUB22} = 2 \cdot R_{\rm SUB2} \tag{13}$$

$$R_{\rm SUB12} = 2R_{\rm SUB1} // 2R_{\rm SUB2}. \tag{14}$$

The substrate capacitances C_{S11}, C_{S12}, and C_{S22} are determined from the dielectric relaxation time of the substrate and their associated substrate resistances $R_{\rm SUB11}$, $R_{\rm SUB12}$, and $R_{\rm SUB22}$, respectively, such that

$$R_{\rm SUB}C_S = \varepsilon_r \varepsilon_0 \rho_{\rm SI} \tag{15}$$

where ε_r is the relative permittivity of the substrate (11.7 for silicon), ε_0 is the permittivity of free space, and $\rho_{\rm SI}$ is the substrate resistivity in $\Omega \cdot$ m [5].

Series inductance and skin-effect parameters L, L_f, R_f, and R_m are optimized to obtain broad-band agreement between the equivalent circuit and ASITIC-generated or measured y-parameters. The resulting y_{12} of the double-π model should produce the low-frequency inductance and resistance given by (3) and (4). C_P can be optimized concurrently with these parameters. However, if the total line length is less than approximately one-tenth of a wavelength, the difference in potential along the line is small, as is the electrical energy stored by C_P. Hence, it does not play a significant role in the inductor model. This does not apply to a differential inductor, as large potential differences can be observed between the two terminals of the inductor.

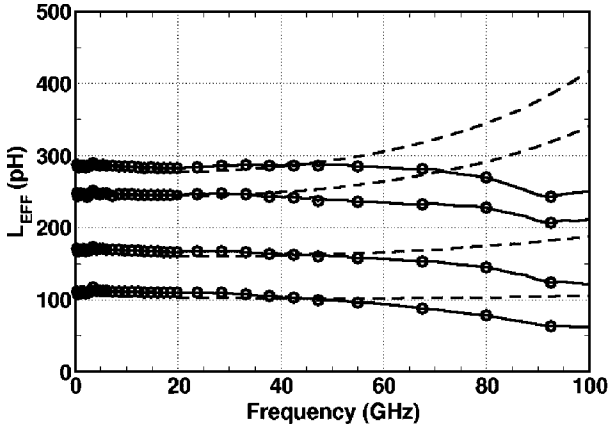

Fig. 12. Measured (solid lines) and modeled (dashed lines) $L_{\rm EFF}$ as a function of frequency up to 100 GHz.

B. Model Verification

The compact inductor model is applicable to both planar and stacked millimeter-wave inductors. Models were extracted from ASITIC simulations up to 100 GHz for the family of planar inductors presented in Section II, and are compared with 100-GHz measurements in Fig. 12. While the ASITIC-based models concur with measured data at lower frequencies, discrepancies are noticed above 50 GHz. In all cases, the dc resistance predicted by ASITIC is less than 3.5 Ω, which calls for careful layout of open and short deembedding structures to minimize lead resistance. Further investigations focusing on deembedding techniques and measurement error above 40 GHz are needed to conclude whether measurements or simulations are responsible for disparities.

ASITIC simulations of the 400-pH three-layer stacked inductor introduced in Section II are compared in Fig. 13 with measured data. Simulations were performed at two extreme process corners to illustrate the impact of $+/-10\%$ variability in backend processing. The first process corner includes low metal sheet resistances and via resistances, along with thicker interlevel dielectrics to represent a "high-Q" process corner, while the "low-Q" corner uses high resistances and thinner dielectrics such that the inductor is closer to the substrate. It is noted that the high-Q process corner results in $\sim$10 GHz better SRF and a significant (40%) improvement in Q.

Equivalent circuit parameters for a two-metal 400-pH stacked inductor were extracted from y-parameters measured up to 50 GHz. Excellent agreement between measured and modeled effective inductance and quality factor is shown in Fig. 14 and demonstrates the applicability of the compact inductor model at millimeter waves.

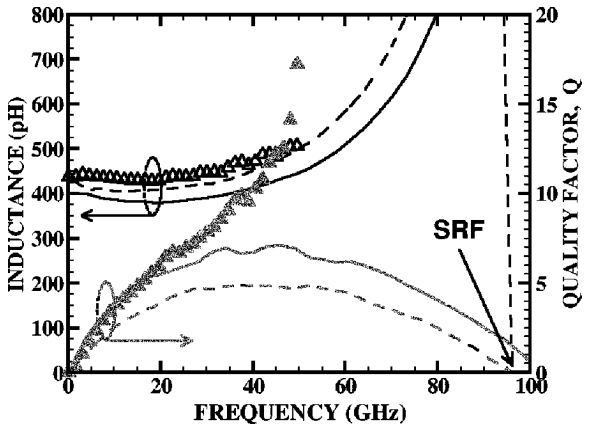

Fig. 13. Measured (symbols) and ASITIC-simulated $L_{\rm EFF}$ and Q for a 400-pH inductor implemented by stacking three metal layers in series. Simulations for a "high-Q" low metal and via resistance, thick dielectric process corner (solid), and a "low-Q" high metal and via resistance thin dielectric process corner (dashed) are shown.

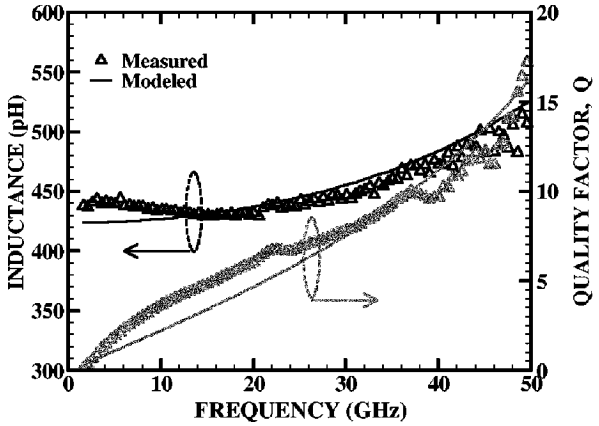

Fig. 14. Measured (symbols) and modeled (lines) $L_{\rm EFF}$ and Q for a 400-pH multimetal inductor implemented by stacking two metals in series.

V. Millimeter-Wave Circuits

While common in lower frequency RF designs, inductors have not been considered to date in millimeter-wave applications. However, both broad- and narrow-band circuits can benefit from their use. In broad-band applications, peaking inductors can extend the bandwidth of resistively loaded amplifiers by up to approximately 40%. For a given bandwidth, current consumption can be traded off for inductance, which aids in the design of low-power transceivers. Furthermore, given the need to reduce inductor footprint to maximize inductor performance at millimeter-wave frequencies, the additional area occupied is not as exorbitant as it is at RF frequencies. In millimeter-wave tuned circuits, a number of silicon-based designs presented to-date (e.g., [1], [2]) make extensive use of transmission-line resonators. However, replacing transmission lines with inductors can reduce chip dimensions and facilitate the production of low-cost components. This paper demonstrates for the first time that inductors can be used in these applications without degrading performance.

To further prove the applicability of these inductors and transformers at millimeter-wave frequencies, a variety of millimeter-wave circuits have been designed and fabricated in a

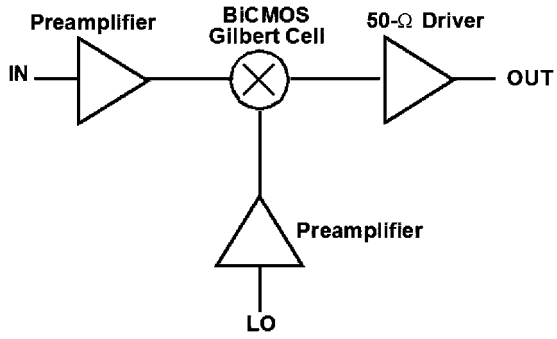

Fig. 15. Block diagram of a dc-to-50-GHz broad-band mixer with transimpedance preamplifiers and BiCMOS Gilbert multiplier.

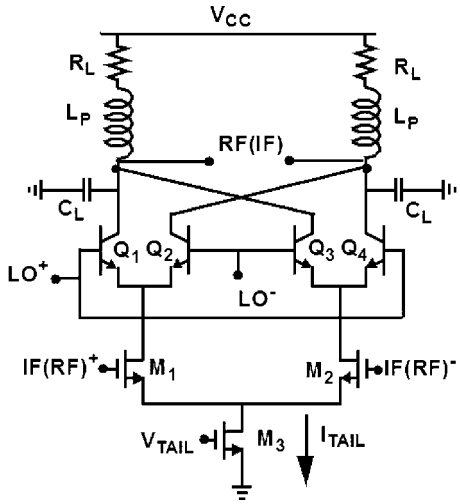

Fig. 16. Circuit schematic of BiCMOS Gilbert multiplier cell, with n-MOS transconductors and SiGe HBT mixing quad.

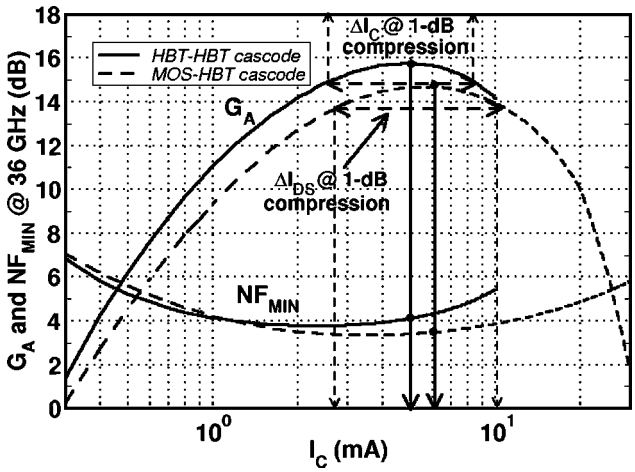

Fig. 17. Available gain and minimum noise figure versus current at 36 GHz for an SiGe HBT cascode (solid) and MOS-HBT cascode (dashed line). Device sizes are 0.2 μm $\times$ 5 μm for the SiGe HBTs, and 12 $\times$ 2 μm $\times$ 0.13 μm for the n-channel MOSFETs. Selection of the bias point for maximum gain is illustrated for both cascodes, along with the current variation that can be tolerated before 1-dB compression occurs.

production 0.13-μm SiGe BiCMOS technology with 150-GHz f_T SiGe HBT from STMicroelectronics, Crolles, France [9]. From these, the first dc-to-50-GHz broad-band mixer and the first inductor-based VCO at 40 GHz are discussed below as

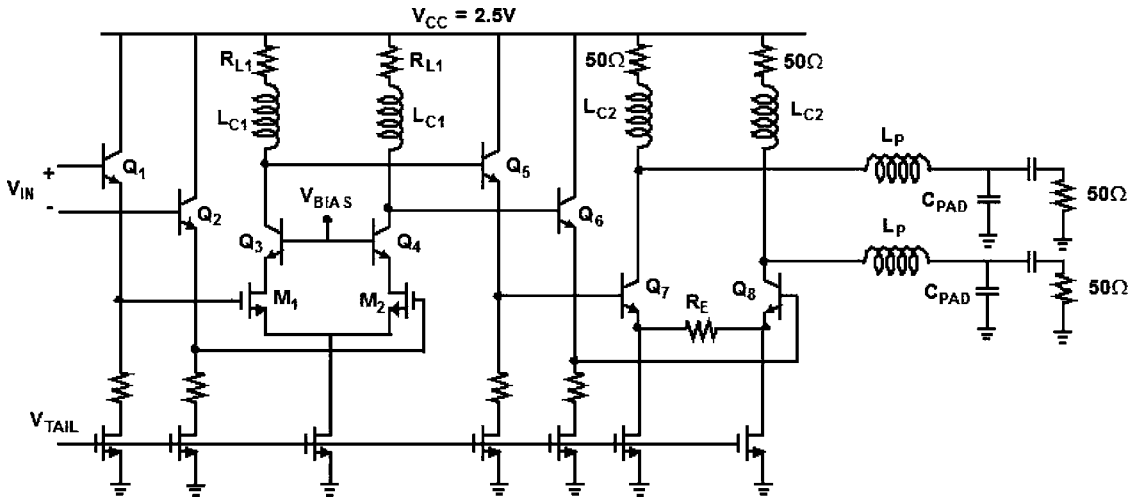

Fig. 18. Circuit schematic of a broad-band BiCMOS 50-Ω output driver employing millimeter-wave spiral inductors.

typical broad- and narrow-band millimeter-wave circuits that benefit from the reduced area afforded by the use of inductors. Additionally, an application of the planar millimeter-wave transformer presented in Section III can be found in [13].

A. Broad-Band Mixer

Fig. 15 shows a block diagram of a novel dc-to-50-GHz broad-band mixer, which can be used both as an upconverter or downconverter. The circuit consists of a BiCMOS Gilbert multiplier-cell low-noise transimpedance preamplifiers with broad-band 50-Ω impedance match on the input and local oscillator (LO) paths [12], and a 50-Ω output driver with 50-GHz bandwidth.

The BiCMOS Gilbert cell, shown in Fig. 16, expounds upon a novel BiCMOS cascode, which has been shown to have excellent performance for millimeter-wave applications due to the low gate resistance of the MOSFET and low-output capacitance of the SiGe HBT [13] while operating with lower supply voltages. The topology consists of MOS transconductors and an SiGe HBT switching quad, the latter of which reduces the required LO power. As will be proven, this BiCMOS topology is ideal for satisfying low-noise and high-linearity requirements simultaneously.

To illustrate the design methodology for the mixer, the available gain (G_A) and minimum noise figure $(\mathrm{NF}_{\mathrm{MIN}})$ of the HBT and BiCMOS cascodes as a function of the collector/drain current are compared in Fig. 17. The bias current is selected such that the gain is maximized at 36 GHz, as shown in this figure. This results in lower noise when a MOS transconductor is employed since $\mathrm{NF}_{\mathrm{MIN}}$ is minimized at approximately the same current density at which f_T peaks for this device [14]. Additionally, larger current variations can be tolerated in the BiCMOS cascode before the gain is reduced by 1 dB, indicating better linearity. To optimize the linearity and bandwidth, the MOS transistors are biased at the peak-f_T current density, with transistor gatewidth (W) given by

$$W = \frac{I_{\mathrm{TAIL}}}{2J_{\mathrm{P}fT}}. \tag{16}$$

The peak-f_T current density of the n-channel MOSFET $J_{\mathrm{P}fT}$ is approximately 0.25–0.3 mA per micrometer of gatewidth, irrespective of technology for CMOS generations below the 0.5-μm technology node [15]. For high-speed large-signal operation, SiGe HBT differential pairs are biased at a tail current corresponding to roughly 1.5 times the peak f_{T} current density for the device [15]. In a mixing quad, the appropriate emitter length is then related to the tail current of the Gilbert multiplier as

$$l_e = \frac{I_{\mathrm{TAIL}}}{3J_{\mathrm{P}fT}w_e}. \tag{17}$$

Here, the peak-f_T current density $(J_{\mathrm{P}fT} = 7\ \mathrm{mA}/\mu\mathrm{m}^2)$ of the SiGe HBT is technology dependent.

The frequency-dependent voltage conversion gain of the inductively-peaked mixer is given by

$$A_C = -\frac{2}{\pi}g_{m,M1}\frac{R_L + j\omega_{\mathrm{OUT}}L_p}{(j\omega_{\mathrm{OUT}})^2L_pC_L + j\omega_{\mathrm{OUT}}R_LC_L + 1} \tag{18}$$

where the load capacitance C_L includes the transistor output capacitance and external loading. The peaking inductance L_P can be chosen to give maximum bandwidth extension [16]

$$L_P = \frac{R_L^2C_L}{\sqrt{2}}. \tag{19}$$

It is noted that this choice of L_P will result in gain peaking. While the mixer is broad-band in the sense that it can operate as an upconverter or downconverter from dc to 50 GHz, the input and output signals are relatively narrow-band (less than 10 GHz) and the peaking in frequency response can be tolerated as long as the signal bandwidth is within the 3-dB bandwidth of the mixer. Inductively peaking the output node allows for bandwidth extension without increasing power consumption.

Expounding on the novel BiCMOS cascode topology, a differential output driver (Fig. 18) has been designed to have 50-GHz bandwidth while driving an external 50-Ω load. Although originally intended as an output driver in broad-band serial communication circuits, the driver was applied to the mixer test circuit. The output swing can be adjusted by varying

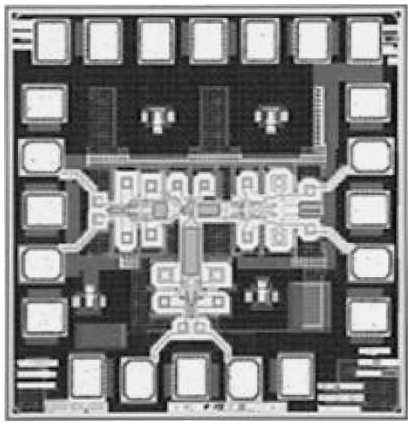

Fig. 19. Die photograph of the broad-band mixer with preamplifiers and output driver. The circuit employs 20 millimeter-wave inductors, each smaller than a 55 μm $\times$ 70 μm pad, and occupies a total area of 720 μm $\times$ 720 μm.

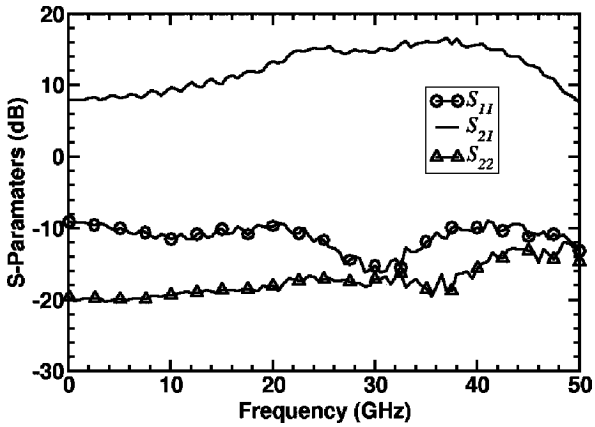

Fig. 20. Measured single-ended s-parameters of the mixer operating as an amplifier. The amplifier has 8 dB of gain at 50 GHz.

the bias current in the driver. Using a BiCMOS cascode as the first stage of the driver enables high bandwidth while operating from a lower supply voltage than can be attained in pure-bipolar topologies [13]. Furthermore, unlike the SiGe HBT, the MOSFET input capacitance is not strongly dependent on the bias point and, hence, the current can be widely varied without degrading bandwidth. The second stage requires a 50-Ω load resistance for broad-band output matching. This, along with the desired output swing, dictates the bias current in the second stage. To maximize output swing, a bipolar inverter output stage is used instead of a cascode. Resistive degeneration is employed to lessen the gain and input capacitance variation with bias current. Inductive peaking is added to the BiCMOS cascode inverter to improve its bandwidth. Additionally, shunt-series peaking at the output prevents the $\sim$40-fF parasitic pad capacitance from limiting bandwidth [14].

As seen from the die photograph in Fig. 19, each of the 20 millimeter-wave inductors is smaller than a 55 μm $\times$ 70 μm bond pad. Despite the large number of inductors, the circuit occupies an area of only 720 μm$\times$720 μm, and is pad limited. The measured small-signal single-ended s-parameters of the mixer operating as an amplifier are illustrated in Fig. 20. Input and output return loss is better than -9 dB up to 50 GHz, and the single-ended gain is better than 8 dB over the measured range.

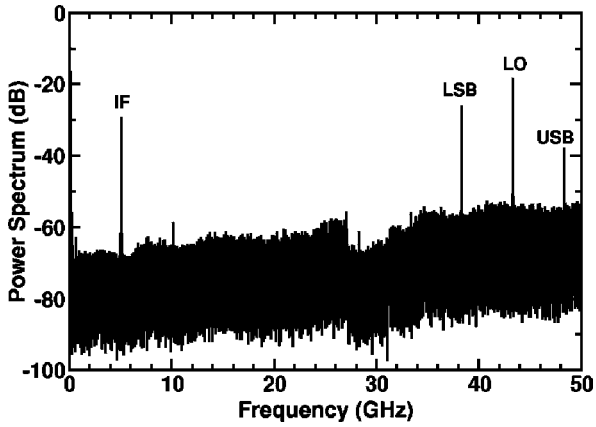

Fig. 21. Measured output spectrum of the mixer operating as an upconverter with -40-dBm 5-GHz IF input and 43-GHz LO. Cable and probe losses have not been deembedded.

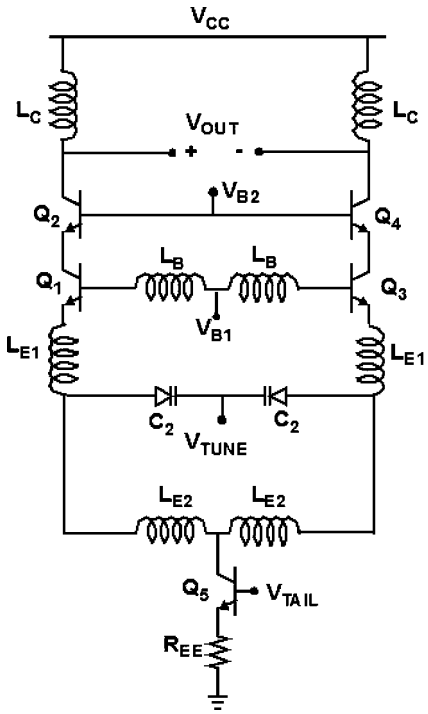

Fig. 22. Circuit schematic of 40-GHz Colpitts VCO. Inductors L_B, L_C, and L_{E2} are implemented with on-chip spiral inductors.

The measured output spectrum of the mixer working as an upconverter with a -40-dBm 5-GHz input signal and 43-GHz LO signal is shown in Fig. 21. As seen in Fig. 20, there is a 5-dB difference in measured gain between the lower sideband (LSB) frequency of 38 GHz and the upper sideband (USB) frequency of 48 GHz. This, combined with the additional 7 dB of cable and probe losses at 48 GHz, accounts for the higher spectral power observed in the LSB of Fig. 21. The mixer with input preamplifier, LO buffer, and output driver consumes 195 mW from a 2.5-V supply, including only 15 mW from the mixer core. Even though MOSFETs, with a lower f_T than either SiGe or InP HBTs, are used as transconductors in the Gilbert cell, the mixer still has higher bandwidth than the fastest reported dc-to-40-GHz InP HBT mixer and operates from a lower supply voltage [17].

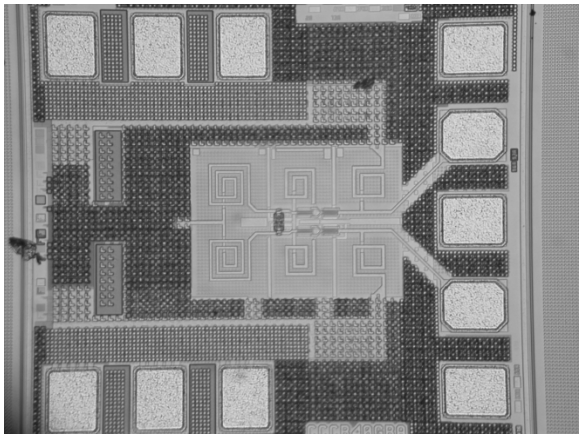

Fig. 23. Die photograph of the 40-GHz Colpitts VCO. The total chip area is 540 μm $\times$ 490 μm, and the VCO core occupies an area of 250 μm $\times$ 180 μm.

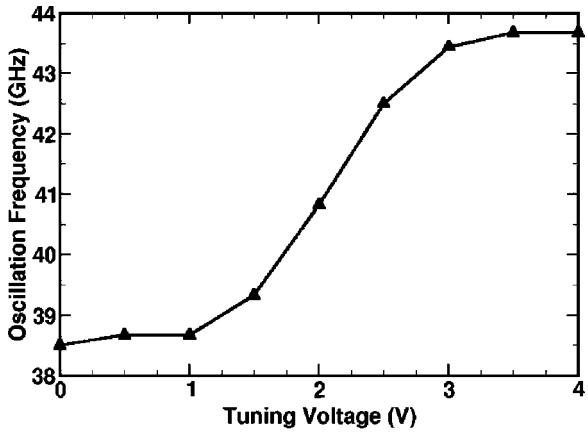

Fig. 25. Measured tuning range of the 40-GHz VCO. The oscillator is tunable over a 5-GHz band.

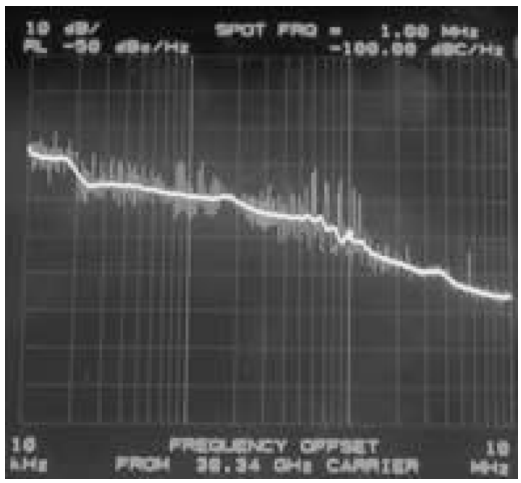

Fig. 24. On-wafer measured SSB phase noise of the 40-GHz VCO. The phase noise is -100.0 dBc/Hz at a 1-MHz offset.

B. Millimeter-Wave VCO

A Colpitts VCO was also designed to prove the advantage of using inductors to reduce area and power dissipation while maintaining low phase noise. The schematic of a varactor-tuned Colpitts VCO is shown in Fig. 22. The differential 40-GHz VCO uses eight planar inductors, including tank inductor L_B, which has an ASITIC-predicted Q of 15 at 40 GHz. The addition of degeneration inductor L_{E1} reduces phase noise systematically by 3–4 dB [18]. Consequently, power consumption can be reduced if bias current is traded for inductance to achieve a target phase-noise specification. Inductor L_{E2} prevents the injection of high-frequency noise from current source Q_5 into the tank, thus improving phase noise [19].

A die photograph of the VCO is shown in Fig. 23. It occupies an area of 540 μm $\times$ 490 μm, which is less than half the area of a similar 40-GHz VCO employing transmission-line resonators [2]. Moreover, the chip area is limited by the spacing between bias and high-frequency pads, which was dictated by the probes available for measurements. The VCO core area is only 250 μm $\times$ 180 μm. The measured single-sideband phase noise of -100.0 dBc/Hz at a 1-MHz offset from a 38-GHz fundamental (Fig. 24) is comparable to that achieved in transmission-line based VCOs [2], [20]. Phase-noise measurements were performed on-wafer using standard power supplies. From circuit simulations, the expected phase noise was -101.0 dBc/Hz. The measured center frequency of 41 GHz is in excellent agreement with the value of 40.5 GHz predicted by SPECTRE simulations. The VCO has a 5-GHz tuning range, as seen in Fig. 25, with a VCO gain of 3 GHz/V. The tuning range is less than the expected 7-GHz value, and is attributed to the lower capacitance ratio of the MOS accumulation-mode varactor than that given by the model. The VCO delivers -1 dBm (including cable, probe, and dc blocking capacitor losses) to a 50-Ω load while consuming 85 mW from a 4.3-V supply. These results demonstrate that tuned circuits utilizing spiral inductors yield well-predicted behavior in the millimeter-wave regime without post-fabrication tuning, as in [2].

VI. Conclusion

For the first time, inductors and transformers have been reported with adequate SRF for millimeter-wave applications in silicon-based integrated circuits. The inductor footprint must be minimized to obtain high SRF, making these inductors much more area efficient than transmission-line resonators for use in deep submicrometer technologies. A compact inductor model has been presented, along with a methodology for model extraction based on measured or simulated y-parameters. Their small size allows for the integration of a large number of millimeter-wave inductors to extend circuit bandwidth while reducing power dissipation and chip area. Measured results of the first dc-to-50-GHz broad-band mixer and 40-GHz VCO with integrated inductors demonstrate the applicability of spiral structures in the millimeter-wave range. The mixer operates over a wider frequency range than previously reported broad-band mixers while being biased from a lower supply voltage. Furthermore, the Gilbert cell employed in the broad-band mixer demonstrates for the first time the benefits of a true BiCMOS topology for high-linearity, low-noise, and low-power millimeter-wave circuits. Measured VCO results are comparable to those reported in transmission-line VCOs while occupying less chip area and requiring no post-fabrication tuning.

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