30-nm InAs PHEMTs With f[subscript T] = 644 GHz and f[subscript max] = 681 GHz

30-nm InAs PHEMTs With $f_T = 644$ GHz and $f_{\max} = 681$ GHz

Dae-Hyun Kim and Jesús A. del Alamo

***Abstract*—We present 30-nm InAs pseudomorphic HEMTs (PHEMTs) on an InP substrate with record f_T characteristics and well-balanced f_T and $f_{\max}$ values. This result was obtained by improving short-channel effects through widening of the side-recess spacing ($L_{\rm side}$) to 150 nm, as well as reducing parasitic source and drain resistances. To compensate for an increase in R_s and R_d due to $L_{\rm side}$ widening, we optimized the ohmic contact process so as to decrease the specific ohmic contact resistance (R_c) to the InGaAs cap to 0.01 $\Omega \cdot$ mm. A 30-nm InAs PHEMT with $t_{\rm ins} = 4$ nm exhibits excellent $g_{m,\max}$ of 1.9 S/mm, f_T of 644 GHz, and $f_{\max}$ of 681 GHz at $V_{\rm DS} = 0.5$ V simultaneously. To the knowledge of the authors, the obtained f_T in this work is the highest ever reported in any FET on any material system. This is also the first demonstration of simultaneous f_T and $f_{\max}$ higher than 640 GHz in any transistor technology.**

***Index Terms*—Cutoff frequency (f_T), InAs, maximum oscillation frequency ($f_{\max}$), pseudomorphic HEMTs (PHEMTs), short-channel effects, side-recess spacing ($L_{\rm side}$).**

I. Introduction

THE OUTSTANDING carrier transport properties of III–V compound semiconductors, coupled with sophisticated sub-100-nm device manufacturing technology, have yielded III–V microelectronic devices with outstanding high-frequency characteristics [1]–[5]. Among them, III–V HEMTs in the InGaAs/InAlAs material system have emerged as particularly promising for terahertz applications [1]–[3]. Recent reports of record high-frequency characteristics of InGaAs/InAlAs HEMTs, as assessed by current-gain cutoff frequency (f_T) and maximum oscillation frequency ($f_{\max}$), have been published [1], [2]. These remarkable results stem from the combination of harmonious size scaling, parasitics reduction, and an increase of InAs composition in the channel that improves carrier transport properties.

In FETs, it is known that short-channel effects and parasitics deteriorate the high-frequency characteristics [6], [7]. It is of great importance to pay close attention to these effects as the gate length (L_g) scales down to very small dimensions; otherwise, the benefits of L_g scaling are not realized. In this work, we show that careful attention to reducing parasitic source and drain resistances, as well as improving short-channel effects through cap recess engineering, yields outstanding and well-balanced frequency response in scaled InAs pseudomorphic HEMTs (PHEMTs) on an InP substrate. This should make this technology of great interest to a multiplicity of applications.

II. Process Technology

The epitaxial layer structure used in this work is the same as in [2] and [3]. At its heart, this heterostructure contains a composite channel with a 5-nm pure InAs core, and two 2- and 3-nm $In_{0.53}Ga_{0.47}As$ cladding layers. Device fabrication took place broadly along the lines of previous reports from our group [2]. In essence, this is a triple-recess process that results in an InAlAs barrier layer thickness $t_{\rm ins}$ of about 4 nm. The T-shaped gate with a Ti/Pt/Au (20/20/350 nm) metal stack is fabricated through a SiO_2-assisted process with a stem height of 150 nm to minimize parasitic capacitance [3], [8]. The device has a T-type gate layout. We estimated the gate length and the insulator thickness from cross-sectional TEM of a 30-nm gate [2]. Taking into account the rounding shape at both edges of the gate, L_g was estimated to be 30 ± 2 nm.

In this work, we have paid particularly close attention to reducing parasitic resistance and capacitance and to improving short-channel effects. The last two items are accomplished by widening the side-recess spacing ($L_{\rm side}$) to 150 nm. Our earlier work that yielded $f_T = 628$ GHz and $f_{\max} = 331$ GHz (at the same bias point) [2] used an $L_{\rm side}$ value of 80 nm. It is well known that increasing $L_{\rm side}$ decreases parasitic capacitance [9], [10], increases $f_{\max}$ [9], and improves short-channel effects [11], but it also decreases f_T [9], [12]. The degradation in f_T arises mainly from an increase in the parasitic source (R_s) and drain resistances (R_d). We have worked to compensate for this by reducing the source–drain spacing from 2 [2] to 1.5 μm and by cutting down the ohmic contact resistance (R_c). This was achieved through a systematic optimization of the ohmic fabrication process. Our new process includes a surface pretreatment step consisting of diluted HF solution for 30 s, an optimized thickness of the Ni/Ge/Au ohmic stack (10/45/150 nm), and an optimized RTA contact annealing step at 320 °C for 30 s. The new process yielded an ohmic contact resistance of 0.01 $\Omega \cdot$ mm to the n^+-InGaAs cap, as obtained through standard TLM characterization. This is a quarter of the value of our previous technology [2]. As a consequence, we have reduced the values of R_s and R_d from 0.21 and 0.24 $\Omega \cdot$ mm in [2] to 0.19 and 0.21 $\Omega \cdot$ mm, respectively, as measured by the gate current injection technique [13], even while widening $L_{\rm side}$.

Manuscript received April 1, 2010; revised May 12, 2010; accepted May 13, 2010. Date of publication July 12, 2010; date of current version July 23, 2010. This work was supported in part by Intel Corporation and in part by the Focus Center Research Program on Materials, Structures and Devices at the Massachusetts Institute of Technology. The work of D.-H. Kim was supported in part by Korea Research Foundation Fellowship KRF-2004-214-D00327. The review of this letter was arranged by Editor G. Meneghesso.

D.-H. Kim was with the Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, MA 02139 USA. He is now with Teledyne Scientific Co., Thousand Oaks, CA 91360 USA.

J. A. del Alamo is with the Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2051133

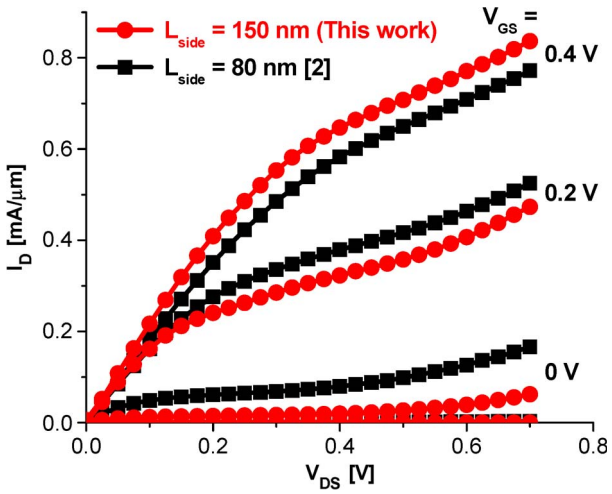

Fig. 1. DC output characteristics of $L_g = 30$ nm InAs PHEMTs, together with those in [2].

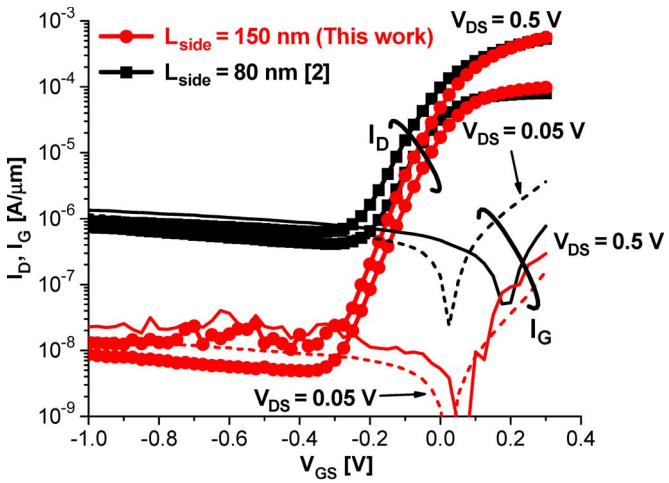

Fig. 2. Subthreshold characteristics of $L_g = 30$ nm InAs PHEMTs at $V_{\rm DS} = 0.05$ and 0.5 V, together with those in [2]. The figure also includes gate leakage current I_G (dashed lines at $V_{\rm DS} = 0.05$ V and solid lines at $V_{\rm DS} = 0.5$ V).

III. Results and Discussion

Fig. 1 shows the output characteristics of representative InAs PHEMTs with $L_g = 30$ nm and $W_g = 2 \times 50$ μm, together with our previous device having the same geometry, except for a value of $L_{\rm side} = 80$ nm [2]. Even though $L_{\rm side}$ was enlarged in this work, we obtain a higher drain current density (I_D) and lower $R_{\rm ON}$. These are mainly the consequence of the improvement in ohmic contact resistance. The maximum transconductance $(g_{m,\max})$ of the $L_g = 30$ nm device is 1.9 mS/μm at $V_{\rm DS} = 0.5$ V, which is about 12% higher than that of [2].

Fig. 2 shows a semi-log plot of the drain (I_D) and gate currents (I_G) as a function of $V_{\rm GS}$ for the present device at a $V_{\rm DS}$ of 0.05 and 0.5 V, together with those in [2]. The V_T of the present devices, defined as the value of $V_{\rm GS}$ that yields $I_D = 1$ mA/mm, is -0.15 V at $V_{\rm DS} = 0.5$ V. In particular, widening $L_{\rm side}$ results in a remarkable improvement in the subthreshold characteristics. The present device exhibits far better short-channel effects as manifested by a subthreshold swing (S) of 80 mV/dec and drain-induced barrier lowering (DIBL) of 80 mV/V at $V_{\rm DS} = 0.5$ V when compared with the device in [2] which had $S = 93$ mV/dec and $DIBL = 130$ mV/V. In addition, we find about 100× lower gate leakage current (lines in Fig. 2). This is another well-known benefit of increasing $L_{\rm side}$ [9], [10].

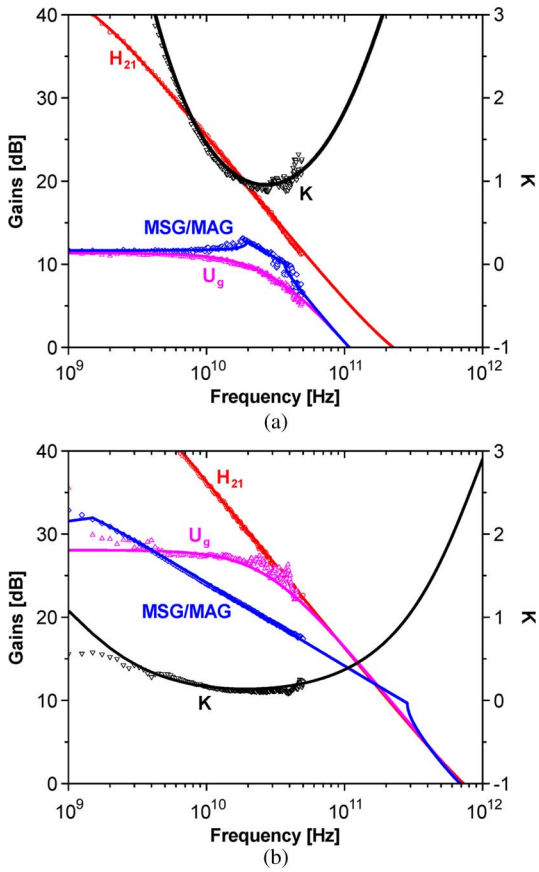

Fig. 3. $|H_{21}|$, Mason's unilateral gain (U_g), MSG, and stability factor (k) against frequency for $L_g = 30$ nm InAs PHEMTs with $W_g = 2 \times 50$ μm at $V_{\rm GS} = 0.2$ V and (a) $V_{\rm DS} = 0.1$ and (b) 0.5 V, together with those (solid lines) from S-parameter simulations from a small-signal model.

Microwave performance was characterized using three different network analyzers with a standard LRM calibration: 1) 1–40 GHz using an HP 8510C; 2) 1–50 GHz using a separate HP 8510C; and 3) 1–60 GHz using an Agilent PNA. We used on-wafer open and short structures to subtract pad capacitances and inductances from the measured device S-parameters. Using the de-embedded S-parameters, we constructed a small-signal model. In this model, R_S and R_D were determined using the gate current injection technique and R_G using the S-parameter measurements.

Fig. 3 shows H_{21}, maximum stable gain (MSG), Mason's unilateral gain (U_g), and stability factor (k) against frequency from 1 to 50 GHz for a 30-nm-gate-length device at $V_{\rm GS} = 0.2$ V and (a) $V_{\rm DS} = 0.1$ and (b) 0.5 V, together with predictions from the small-signal model (solid lines). At both values of $V_{\rm DS}$, an excellent fit is obtained over the entire frequency range. In this particular measurement, a value of $f_T = 645$ GHz was obtained at $V_{\rm DS} = 0.5$ V, by extrapolating $|H_{21}|$ with a slope of -20 dB/dec using a least squares fit. Measurements on the other two systems in this same device yielded 645 and 643 GHz, as summarized in Table I.

We have also selected three different 30-nm devices which showed nearly identical dc behavior. The f_T of these devices in measurements from 1 to 50 GHz was 645 [shown in Fig. 3(b)],

TABLE I
VALUES OF THE EXTRACTED f_T AND $f_{\max}$ FOR 30-nm InAs PHEMTs USING THREE DIFFERENT MEASUREMENT SYSTEMS ON THE SAME DEVICE, AT $V_{\rm GS} = 0.2$ V AND $V_{\rm DS} = 0.5$ V

		8510C @MIT	8510C @TSC	PNA @UCSB	Avg.	STD
f_T [GHz]	From H_{21}	645	645	643	644.3	0.9
	From Gummel's approach	644	644	645	644.3	0.5
f_{max} [GHz]		681	686	677	681.3	3.7

644, and 644 GHz. The value of f_T in these devices was verified through Gummel's approach [2], [14], yielding $f_T = 644$ GHz with a standard deviation of 1.4 GHz. We also verified f_T through the small-signal model. An extrapolated cutoff frequency from the measured frequency range with a slope of -20 dB/dec leads to a value of $f_T = 648$ GHz. On average, then, we are confident in reporting an f_T for this technology at this bias point of 644 GHz. To the knowledge of the authors, this is the highest f_T ever reported in any FET on any material system.

Regarding $f_{\max}$, it is hard to directly extract it from the experimental measurement of U_g, particularly at high values of $V_{\rm DS}$. This is because U_g is apt to show sharp peaky behavior at intermediate frequencies when $V_{\rm DS} > 0.6$ V. For a given device, we have verified that this behavior is reproducible across three different measurement systems. Such features have also been reported by other authors in very high frequency devices [1]. To avoid this problem, in this work, we have focused on $V_{\rm DS} \leq 0.5$ V because, in this region, U_g is relatively well behaved and our small-signal model predicts the experimental gain characteristics relatively well, as shown in Fig. 3(a) and (b). Using this model, we extrapolated a value of $f_{\max}$ of 686 GHz at $V_{\rm DS} = 0.5$ V [Fig. 3(b)]. The average $f_{\max}$ obtained among the three systems at this bias point is 681 $\pm$ 4 GHz. We are therefore confident in reporting an $f_{\max}$ of 681 GHz for this technology at the selected bias point. Our small-signal model extraction reveals that this excellent value of $f_{\max}$ arises from a combination of $g_m/g_o = 14.4$ and $C_{\rm gs}/C_{\rm gd} = 6.3$. The relatively low values of g_o and $C_{\rm gd}$ arise partly from the widening $L_{\rm side}$. To the knowledge of the authors, this is the first simultaneous demonstration of both f_T and $f_{\max}$ in excess of 640 GHz in any transistor technology on any material system.

IV. CONCLUSION

We have fabricated $L_g = 30$ nm InAs PHEMTs having a simultaneous record f_T of 644 GHz and an $f_{\max}$ of 681 GHz at $V_{\rm DS} = 0.5$ V. This outstanding performance stems from improved short-channel effects and reduced parasitic capacitance obtained by widening $L_{\rm side}$ to 150 nm and reducing the parasitic source and drain resistances through an optimized ohmic contact process.

ACKNOWLEDGMENT

Epitaxial heterostructures were supplied by MBE Technology. Device fabrication took place at the Microsystems Technology Laboratories, the Scanning-Electron-Beam Lithography Facility, and the Nanostructures Laboratory at the Massachusetts Institute of Technology. The authors would like to thank P. Chen, at TSC, and Nidhi and U. Mishra, at UCSB, for the help with high-frequency S-parameter measurements.

REFERENCES

[1] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT device with $f_{\max}$ greater than 1 THz," in *IEDM Tech. Dig.*, 2007, pp. 609–612.

[2] D.-H. Kim and J. A. del Alamo, "30-nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 830–833, Aug. 2008.

[3] D.-H. Kim and J. A. del Alamo, "30-nm E-mode InAs PHEMTs for THz and future logic applications," in *IEDM Tech. Dig.*, 2008, pp. 719–722.

[4] W. Snodgrass, W. Hafez, N. Harff, and M. Feng, "Pseudomorphic InP/InGaAs heterojunction bipolar transistors (PHBTs) experimentally demonstrating $f_T = 765$ GHz at 25 °C increasing to $f_T = 845$ GHz at -55 °C," in *IEDM Tech. Dig.*, 2006, pp. 595–598.

[5] Z. Griffith, E. Lind, and M. J. W. Rodwell, "Sub-300 nm InGaAs/InP type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz $f_{\max}$ and 416 GHz f_T," in *Proc. IEEE Int. Conf. IPRM*, 2007, pp. 403–406.

[6] A. Endoh, Y. Yamashita, K. Shinohara, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, "InP-based high electron mobility transistors with a very short gate-channel distance," *Jpn. J. Appl. Phys.*, vol. 42, no. 4B, pp. 2214–2218, Apr. 2003.

[7] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "547 GHz f_t $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ HEMTs with reduced source and drain resistance," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 241–243, May 2004.

[8] S. Wada, J. Yamazaki, M. Ishikawa, and T. Maeda, "An 0.1-μm voidless double-deck-shaped (DDS) gate HJFET with reduced gate-fringing-capacitance," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 859–864, May 1999.

[9] T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso, and E. Zanoni, "30-nm two-step recess gate InP-based InAlAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 49, no. 10, pp. 1694–1700, Oct. 2002.

[10] D.-H. Kim, J. A. del Alamo, J.-H. Lee, and K.-S. Seo, "The impact of side-recess spacing on the logic performance of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs," in *Proc. 18th IEEE IPRM Conf.*, May 2006, pp. 177–180.

[11] D.-H. Kim and J. A. del Alamo, "Impact of lateral engineering on the logic performance of sub-50 nm InGaAs HEMTs," in *Proc. ISDRS*, 2007, pp. 1–2.

[12] K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Mimura, S. Hiyamizu, and T. Matsui, "Nanogate InP-HEMT technology for ultrahigh-speed performance," in *Proc. 16th IEEE IPRM Conf.*, 2004, pp. 721–726.

[13] D. R. Greenberg and J. A. del Alamo, "Nonlinear source and drain resistance in recessed-gate heterostructure field-effect transistors," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1304–1306, Aug. 1996.

[14] H. K. Gummel, "On the definition of the cutoff frequency f_T," *Proc. IEEE*, vol. 57, no. 12, p. 2159, Dec. 1969.