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# 350 mV, 5 GHz Class-D Enhanced Swing Differential and Quadrature VCOs in 65 nm CMOS

Ankur Guha Roy, *Student Member, IEEE,* Siladitya Dey, *Student Member, IEEE,* Justin B. Goins, *Student Member, IEEE,* Terri S. Fiez, *Fellow, IEEE,* Kartikeya Mayaram, *Fellow, IEEE*

**Abstract**

A new enhanced swing class-D VCO which operates from a supply voltage as low as 300 mV is presented. The architectural advantages are described along with an analysis for the oscillation frequency. Prototype differential and quadrature variants of the proposed VCO have been implemented in a 65 nm RF CMOS process with a 5 GHz VCO oscillation frequency. At a 350 mV supply, the measured phase noise performance for the quadrature VCO with a 5% tuning range is -137.1 dBc/Hz at 3 MHz offset with a power dissipation of 2.1 mW from a 0.35 V supply. The highest resulting figure-of-merit (FoM) is 198.3 dBc/Hz.

**Index Terms**

Oscillators, Voltage controlled oscillators, Low Voltage VCO, Enhanced Swing, class-D, Differential VCO, Quadrature VCO, Transformer Coupling.

The authors are with the Department of EECS, Oregon State University, OR 97331 USA. e-mail: guharoya@eecs.oregonstate.edu

# I. Introduction

Wireless sensor networks (WSN) have been an important area of interest during recent years. WSNs usually contain numerous independent sensor nodes that power themselves from energy harvesters such as thermoelectric or piezoelectric generators. Typically these energy harvesters produce low power and low voltage outputs. The power consumption of a sensor node can be reduced by duty cycling for low data rate applications [1]. The low voltage output of an energy harvester necessitates the use of circuits that can operate below 0.5 V. The design of RF circuits that can operate in this voltage range is challenging. Most transceivers require a voltage controlled oscillator (VCO) with low phase noise performance, which is difficult to obtain when the output swing is constrained by a low supply voltage. Swing enhancement techniques are needed to increase the oscillation amplitude [2]–[4]. The increased oscillation amplitude results in better phase noise performance.

The WSN transceiver architectures that employ complex signal processing with an in-phase and a quadrature component (e.g., the direct conversion architecture in [5]) require a local oscillator (LO) with two output phases which are $90^o$ apart. Several techniques have been reported in the literature [6]–[12] to implement a quadrature signal. These include: a frequency doubled VCO followed by a divide-by-2 circuit [6], a differential VCO followed by a poly-phase filter [7], an LC-ring based structure [8], an energy circulating structure [9], and two VCOs coupled to each other to generate quadrature outputs [10]–[12]. Most of these methods are only usable for high supply voltage applications. The first two methods [6], [7] consume additional power due to the presence of an extra divider and poly phase filter. The methods used in [8], [9] can generate multiple phases in a power efficient manner, but they are not area-efficient due to the presence of additional inductors. The method used in [10] is preferred due to reduced power consumption, smaller area, and ease of implementation. However, the architecture in [10] requires a higher supply voltage and it is also not usable for sub 0.5V WSN applications.

A VCO consumes a large fraction of the total power of an entire WSN transceiver [13]. There have been numerous efforts to reduce the power consumption of a VCO for a given phase noise specification. Additional noise filters can be used with the tail current source as in [14], [15]. A power efficient, high voltage class-C VCO architecture has been proposed in [16] with reduced power consumption compared to a standard cross-coupled VCO that operates in the class-B mode [17]. Multiple class-C VCO architectures have been reported recently that achieve enhanced performance at a reduced supply voltage by employing an amplitude control loop [18]–[21].

Since an oscillator is an amplifier connected in feedback, a class of switching amplifiers based on the operation of the MOSFET in class D, E or F mode can be used to implement an oscillator with a good power conversion efficiency. Differential class-D and class-F VCOs have been previously reported [22]–[27].

The VCO in [22] is shown in Fig. 1(a). It is a discrete BJT implementation with a transformer turns ratio of at least 10:1. This makes it not suitable for an RF CMOS integrated VCO. The high transformer turns ratio reduces the loop gain causing potential start-up issues. The architecture of [23], [24] is shown in Fig. 1(b). In this architecture, class-D operation is achieved with an inductor. This simplifies the design and makes it viable for on-chip implementation. However, this method is not directly applicable for quadrature output generation without using additional coupling elements.

This paper presents differential and quadrature VCOs designed for low-voltage sensor network applications. The proposed designs are enhanced-swing class-D VCO architectures, suitable for GHz range frequencies with a sub 0.5 V supply. The proposed class-D VCO exploits the architectural benefits of [22], as well as the benefits of a MOSFET based implementation [23], [24], [28]. Our work shows the first on-chip implementation of a quadrature class-D VCO with the best FoM reported to date [29]. A similar class-D quadrature VCO architecture was also

recently proposed in parallel to our work and presented simulation results [30].

The rest of the paper is organized as follows: Section II presents the evolution of the proposed class-D quadrature VCO architecture followed by some architectural analyses. Section III focuses on the design considerations and Section IV provides measurement results from a prototype test-chip. Finally, conclusions are drawn in Section V.

## II. Proposed Differential and Quadrature Class-D VCOs

A current-mode class-D power amplifier (PA) [31], [32] is shown in Fig. 2(a). A differential class-D VCO cell can be derived by introducing a feedback between the input and the output of this power amplifier, as shown in Fig. 2(b). This differential VCO architecture uses a top inductor, $L_{top}$ and a transformer similar to [22] to reduce the power consumption.

Two of these VCOs can be combined to implement a quadrature class-D VCO, shown in Fig. 2(c) [29]. The top inductors are combined into a single inductor $(L_{top})$, which is leveraged for a super-harmonic coupling [33] between the two VCOs. The super-harmonic coupling ensures that the two differential VCO cells oscillate in quadrature. Since the inductor is a passive, reactive element, it adds less noise compared to an active device coupled quadrature VCO as in [12]. In our work, swing enhancement is achieved through the VCO architecture instead of using two additional inductors as in [10]. This saves valuable chip area. The output peak-to-peak swing of this oscillator is well above the supply voltage ($\approx 3V_{DD}$). The enhanced output swing results in an improved phase noise performance.

The differential VCO shown in Fig. 2(b) can be redrawn as in Fig. 3(a) with an ideal transformer. The inductance of the primary coil is modeled as two separate inductors ($L/2$ each) and the MOSFETs are shown as switches. Each MOSFET switch is 'on' for approximately half of the oscillation period. A sufficiently large value of the top inductor, $L_{top}$ works like a current source (or choke) of value equal to the average current consumption, $I_{avg}$ through the VCO.

This current is steered through $M_1$ (or $M_2$) for approximately half of the period as shown in Fig. 3(b). The MOSFETs dissipate power when both $V_{DS}$ and $I_D$ are non-zero as shown in Fig. 3(c). In the VCO of [23], the gate and drain bias voltages of the MOSFETs are identical. In the proposed differential VCO cell shown in Fig. 3(a), a transformer coupling between the gate and the drain of a MOSFET switch allows for a separate gate bias $(V_G)$. The gate bias, $V_G$, is shown in Fig. 3(b) as a dashed-line.

### *A. Effect of Decoupling the Supply and Gate Bias*

The isolation of the average gate and drain bias can be used for reduction of the VCO power consumption in the following ways.

*1) Reduced Supply Voltage Operation:* Since the gate and drain bias voltages are decoupled, the proposed VCO can oscillate at a lower supply voltage than the VCO in [23], [30]. The power consumption in the VCO can be reduced by keeping $V_G$ constant and reducing the supply voltage. A high value of $V_G$ ensures a high start-up gain. The simulated average current consumption for the proposed quadrature VCO, shown in Fig. 4 illustrates this effect.

*2) Improved Power Conversion Efficiency (PCE):* The gate bias, $V_G$, determines the 'on' time of the MOSFET switches and can be utilized to minimize the time overlap between $V_{DS}$ and $I_D$. Thereby, the power dissipated in the MOSFET switches can be reduced, which in turn reduces the power consumption in the class-D VCO.

The power conversion efficiency (PCE) of a current mode class-D power amplifier (PA) was calculated in [31]. Under the assumption of a high gate-to-source swing, the PCE of the PA in Fig. 2(a) is given by,

$$PCE = \frac{32V_{DD}}{9I_{avg}R_L} \tag{1}$$

The VCO in Fig. 2(b) approximately follows this equation for a high gate-to-source swing. For such a VCO, $R_L$ is the load resistance of the primary winding. $V_G$ can be used to decrease

$I_{avg}$. Thus, for a sufficiently high gate-to-source swing the PCE of the VCO can be improved by reducing the gate bias.

### *B. Effect of the Top Inductor*

The top inductor is used for super-harmonic coupling two differential VCO cells to ensure that they oscillate in quadrature. The super-harmonic coupling reduces the output phase noise of the quadrature VCO by 3 dB compared to the individual differential VCO cells. However, two differential VCO cells consume twice as much power compared to a single differential VCO cell. Therefore, the proposed quadrature VCO retains the same efficiency as the proposed differential VCO cell with a top inductor and a bias shift.

The top inductor also reduces the supply noise sensitivity of the VCO, as it acts as a low pass filter and reduces the supply noise sensitivity of the VCO at high frequencies (in GHz range). It should be noted that the transfer function of the low frequency supply noise to the output is almost unchanged by the addition of a top inductor as an inductor has negligible impedance near DC.

The simulated oscillation frequency, for different top inductor values is shown in Fig. 5. For a primary tank inductance $L$, it was observed that for $L_{top} \geq 1.2L$, the sensitivity of the oscillation frequency with $L_{top}$ is negligible.

### *C. Oscillation Frequency*

The previously reported class-D VCO with a floating tank capacitor in [24] has an oscillation frequency of $\approx \frac{1.09}{\sqrt{LC}}$ due to the time variant nature of the tank. A tail filter reduces this time variance and brings the oscillation frequency closer to the resonance frequency [24]. A similar behavior was observed with a top inductor. If $L_{top}$ is sufficiently high, it has a negligible effect on the oscillation frequency of the VCO. The oscillation frequency is approximately given by,

$$\omega_{osc} \approx \frac{1}{\sqrt{LC}} \tag{2}$$

A detailed derivation of the oscillation frequency is shown in Appendix A.

The approximate oscillation frequency in Eq. (2) is derived based on the assumption that the gate of the MOSFET does not load the secondary winding of the transformer. However, the gate-to-source capacitance $(C_{gs})$ of a large MOSFET can contribute significant loading to the transformer. In a transformer coupled VCO, the secondary winding inductance and this capacitance can potentially introduce a second resonance frequency [25]. The two possible oscillation modes of the capacitively loaded transformer architecture are shown in [25] as,

$$\omega_{1,2} = \sqrt{\frac{1 + \left(\frac{L_2 C_{gs}}{LC}\right) \pm \sqrt{1 + \left(\frac{L_2 C_{gs}}{LC}\right)^2 + \left(\frac{L_2 C_{gs}}{LC}\right)(4k_m^2 - 2)}}{2L_2 C_{gs}(1 - k_m^2)}} \tag{3}$$

where $L$ and $L_2$ are the primary and secondary tank inductances, respectively, $C$ is the tank capacitance, $k_m$ is the coupling factor between the primary and secondary winding of the transformer.

As a design choice, a transformer with 1:1 turns ratio was used, i.e., $L \approx L_2$. The coupling factor, $k_m$ for a stacked transformer can be fairly high $(\approx 0.9)$. As a result, the main resonance frequency $(\omega_2)$ of the tank can be expressed as,

$$\omega_1 \approx \sqrt{\frac{1}{L(C + C_{gs})}} \tag{4}$$

Therefore, the oscillation frequency reduces by a factor of $\sqrt{\frac{C}{C+C_{gs}}}$ compared to Eq. (2). In order to keep this error to less than $10\,\%$, $C_{gs}$ should be less than $20\,\%$ of $C_1$.

The second resonance frequency is approximately given by,

$$\omega_2 \approx \sqrt{\frac{(C + C_{gs})}{L_1 C C_{gs}(1 - k_m^2)}} \tag{5}$$

Assuming $C_{gs}$ is smaller than $20\,\%$ of $C_1$, and $k_m \approx 0.9$, $\omega_2$ is approximately 30 times higher than $\omega_1$. This frequency is typically much larger than the self resonance frequency of the stacked

transformer. Therefore, the only possible oscillation mode is at the frequency $\omega_1$.

Since the quadrature VCO is derived from the differential VCO cell, it has an identical oscillation frequency.

### *D. The Output Waveform*

The simulated output voltage waveform of the four single-ended outputs of the proposed quadrature VCO is shown in Fig. 6(a). The differential waveforms are shown in Fig. 6(b). Differentially the two outputs generate a full sinusoidal signal but the single-ended outputs are approximately half sinusoids. The class-D VCO has an RLC tank which is periodically switched by an injection current. The band-pass characteristics of the tank ensures that the differential output voltage is sinusoidal. If the 'on' resistance of the switch is assumed to be small, for approximately half of the time period the single ended outputs are clamped to the ground potential. The output voltage waveform is similar to the voltage waveform observed in a current mode class-D PA [31].

### *E. Oscillation Amplitude of the Class-D VCO*

The differential output voltage of the class-D VCO is sinusoidal with an amplitude $A$. The single-ended output voltage, $V_{DS}(t)$ at the drain of the two MOSFETs and at the center tap of the primary side of the transformer $(V_N)$, under the assumption $L_{top} \gg L/2$, is shown in Fig. 7. The two inductors of value $L/2$ each, work as a voltage divider.

$A$ can be calculated by finding the average value of $V_N$ over the oscillation time period $(T)$, which has to equal $V_{DD}$. This implies that,

$$\frac{1}{T}\int_0^T \left|\frac{A}{2}\sin(\omega t)\right| dt = V_{DD} \quad \Longrightarrow A = \pi V_{DD} \tag{6}$$

A similar method was used in [22] to compute the output oscillation amplitude. An accurate way of calculating the oscillation amplitude was reported in [24]. However, the final results

from both methods are very close indicating that the approximation of the single-ended output waveform by a half sinusoid is valid.

### *F. Phase Noise of the Class-D VCO*

The noise contributors in the differential VCO are the input impedance, $R_p$ of the primary winding at the oscillation frequency, the equivalent series resistance of the top inductor, and the MOSFETs ($M_{1-2}$). The noise sources are shown in Fig. 8.

The noise contribution of the parasitic series resistance $(R_{top})$ of the top inductance was ignored. A perturbation projection vector (PPV) simulation using Cadence Spectre [34] justifies this assumption. The PPV analysis provides the output phase sensitivity of an oscillator to the noise perturbations [35], [36] injected at different times of the oscillation period. Fig. 9(a) and (b) show the PPV from $R_{top}$ and $R_p$, respectively. It is evident that the PPV from $R_{top}$ is approximately 3 orders of magnitude less than the PPV from $R_p$. If the top inductor has a large quality factor, $R_{top}$ is low. The noise contribution from $R_{top}$ can be ignored due to the low noise generation and a low noise transfer function to the output phase.

The output thermal noise generated by a MOSFET depends directly on the small-signal parameters, $g_m(t)$ and $g_{ds}(t)$ [37]. The PPV from different noise sources along with the small-signal time varying transconductance, $g_{m1}(t)$, and $g_{m2}(t)$, and output conductances, $g_{ds1}(t)$, and $g_{ds2}(t)$, are shown in Figs. 9 (c)-(f), respectively. The PPV simulation shows that when the noise generated by a MOSFET is at its maximum value, the transfer function to the output is minimum. This observation can be explained as follows. The two MOSFETs in a class-D VCO act as switches and ideally there is no overlap between their 'on' times. A simplified equivalent circuit diagram for the impedance seen by a MOSFET noise source is shown in Fig. 10. In this picture, M1 is 'on' and M2 is 'off'. As the 'on' resistance of the MOSFET switch $(R_{on})$ is small and the 'off' resistance of the MOSFET switch $(R_{off})$ is high, most of the generated current

noise has a shunt path to ground without significantly affecting the node voltages. Therefore, the output voltage of a class-D VCO should have negligible noise contribution from the MOSFETs. However, in a circuit implementation of a class-D VCO there is some overlap between the 'on' times of the two MOSFETs and they contribute to the phase noise when both are simultaneously 'on'.

The low noise contribution from the MOSFETs and a high oscillation amplitude enable the class-D VCO to exhibit a phase noise performance comparable to the other enhanced swing VCOs [4], [10], which operate in class-AB/B/C modes.

### *G. Effect of Tank-Mismatch on the Phase Error*

In a super-harmonic coupled quadrature VCO, the tank mismatch causes a shift in the resonance frequency of one tank with respect to the other. The oscillation frequency of the quadrature VCO is the average of the resonance frequencies of the two tanks [33]. Since both of the tanks operate slightly off-resonance, there can be a phase error between the in-phase and the quadrature components.

In [33], the output phase error for a given tank mismatch was shown to decrease with a reduction in the average 'on' resistances of the MOSFETs. Similar characteristics were observed from simulations of a quadrature class-D VCO core with a 0.5 % mismatch between the tank capacitors (which can be ensured with a careful design). Since the MOSFETs in the VCO operate in the triode region during most of their on times, the W/L ratio is linearly related to the average on conductance of a MOSFET.

The effect of the tank mismatch on the output phase error of a quadrature VCO was extensively analyzed in [33], [38], [39]. The output phase error $(\phi_e)$ for a super-harmonic coupled quadrature VCO can be expressed as [39],

$$\phi_e = \frac{3Q}{4}\left(\frac{1}{m}+\frac{1}{3}\right)\frac{\Delta\omega}{\omega_o} \tag{7}$$

where $Q$ is the quality factor at resonance, $m$ is the ratio of the second harmonic current to the average bias current through the top inductor (known as the coupling factor), $\Delta\omega$ is the difference between the resonance frequencies of the two tanks in presence of mismatch, and $\omega_o$ is the resonance frequency in absence of mismatch. As predicted by this equation, the output phase error reduces if the coupling factor is increased. The simulated phase errors for different tank mismatches and top inductor values are shown in Fig. 11(a). An increase in the top inductor increases the coupling factor and thus reduces the phase error.

### *H. Effect of Tank-Mismatch on the Phase Noise*

In the active device coupled quadrature VCOs, there is a trade-off between the phase noise and the phase error [38], [40]. If the coupling factor is increased, the phase error reduces but the phase noise increases. The oscillation frequency of an active device coupled quadrature VCO deviates from the tank resonance frequency in presence of coupling. An increase in the coupling factor increases the amount of this frequency deviation. The deviated oscillation frequency causes a degradation in the quality factor and thus increases the phase noise. However, this phase noise degradation can be reduced by using $90^o$ phase shifters inside the coupling loop [38]. These additional phase shifters restore the oscillation frequency close to the tank resonance frequency and thus reduce the phase noise degradation with coupling.

A super-harmonic coupled quadrature VCO is similar to the VCO with a $90^o$ phase shifter since the oscillations are very close to the tank's resonance frequency without causing any Q degradation [39], [41]. A super-harmonic coupled class-D quadrature VCO shows the same behavior. The simulated phase noise for different top inductor and mismatch values is shown in Fig. 11(b). For small mismatches, the phase noise was found to be approximately constant. A

very high mismatch can considerably change the oscillation frequency from the tank resonance frequency and thus increase the phase noise. The simulation results in Fig. 11(b) also show that an increase in the top inductor value reduces the degradation in the phase noise in presence of the mismatch.

### *I. Effect of the Gate Bias and Top Inductor on the Performance of the Proposed VCO*

Three differential VCO architectures were simulated and their performances were compared for different supply voltages. The three VCO architectures are: (i) a previously reported class D VCO architecture [23] (VCO A), (ii) a modified class-D VCO architecture with a top-inductor (VCO B), and (iii) the proposed differential class-D VCO cell with a top inductor and a bias shift (VCO C). To facilitate a fair comparison, identical MOSFET device sizes were used for all VCOs. The primary side of the transformer in (iii) was used as the tank inductor in the first two VCOs and the oscillation frequency of the three VCOs was scaled to 5 GHz by adjusting the floating tank capacitor.

A VCO is often characterized by its Figure-of-Merit ($FoM$). The $FoM$ is a metric that normalizes the VCO performance with respect to phase noise, the average power consumption, the oscillation frequency, and the offset frequency of the phase noise measurement. The simulated power consumption, phase noise, and $FoM$ characteristics of the VCOs are shown in Figs. 12 (a), (b), and (c), respectively. As shown in Fig. 12 (c), VCO B has a higher $FoM$ compared to VCO A.

However, both VCO A and VCO B are limited by the supply voltage and are unable to operate with a supply voltage less than 0.4 V. As shown in Fig. 12 (a), VCO C enables oscillation at a lower supply voltage by decoupling the gate and drain bias voltages, while retaining a good $FoM$. For a very low supply voltage the $FoM$ of VCO C falls rapidly due to an increase in the phase noise. The phase noise increases since both of the MOSFETs are simultaneously ‘on’

for a considerable time, thus injecting noise in the VCO loop. The oscillation amplitude also decreases with the supply voltage causing a further degradation of the phase noise.

With a high supply voltage (close to 0.6 V), Fig. 12 (a) shows that a reduction in the gate bias reduces the average current consumption of VCO C, thus increasing the PCE. Fig. 12 (b) shows that the phase noise of VCO C degrades slightly with a reduction in the gate bias. However, the $FoM$ degradation due to the bias shift is less than a dB in this region of operation. Thus, VCO C can retain a good $FoM$ with a lower power dissipation compared to VCO A and VCO B.

The design of VCO A in [24] utilizes wide MOSFET switches with large $C_{gs}$ values. This single-ended parasitic capacitor reduces the oscillation frequency of VCO A. Therefore, for a high frequency operation of VCO A, a small tank inductance will be needed. However, a small tank inductance increases the power consumption of VCO A. For low power and high frequency applications, large tank inductors and small parasitic capacitors are required. Therefore, VCO B is a better design choice as it achieves a high FoM with a large tank inductor and narrow switches. The proposed VCO C further reduces the power consumption by using a bias shift.

The oscillation frequency and phase noise of the proposed class-D VCO depend on the implementation of the tank capacitor. The best performance is achieved with a floating capacitor. If the tank capacitor is single-ended instead of a floating structure, the oscillation frequency decreases and the phase noise degrades.

### *J. Start-up Requirement of the Proposed Quadrature VCO*

During the start-up phase, each differential VCO cell in a class-D quadrature VCO behaves as a cross-coupled differential VCO cell with a bias shift. Therefore, the start-up characteristics of the differential VCO cell is comparable to a cross-coupled VCO. MOSFETs with large $W/L$ ratios are used as switches to function as large negative transconductors and ensure a reliable start-up. The start-up loop gain of this architecture is identical to a cross-coupled VCO architecture and

much higher compared to a Colpitts based architecture as in [4].

## III. Design Considerations for Differential and Quadrature VCOs

The quadrature VCO was implemented in a 9 metal 65nm RF CMOS process. The MOSFET $W/L$ ratios were selected as $128\mu\mathrm{m}/0.06\,\mu\mathrm{m}$ to operate as low resistance switches.

### *A. The Transformer*

In our implementation, the secondary coil of the transformer is connected to the gates of the MOSFETs ($M_{1-2}$) to provide voltage feedback as shown in Fig. 3(a). Since the gate introduces only a capacitive loading to the secondary coil, there is no static power flow, relaxing the loading and quality factor (Q) requirements for the secondary coil. The reduced loading of the secondary coil allows the use of a transformer with approximately 1:1 turns ratio which enables an on-chip implementation. The reduced Q requirement of the secondary coil also allows the use of a stacked transformer structure and thus saves silicon area.

The transformer was designed as a stacked structure with approximately 1:1 turns ratio, as shown in Fig. 13. A stacked transformer requires the same area as an inductor and does not increase the overall chip area.

The primary coil of the transformer was implemented using an ultra-thick copper layer M9 to achieve a high quality factor $(Q \approx 20)$ at 5 GHz. A high quality factor of the primary coil improves the phase noise performance. The secondary coil is a stacked inductor consisting of two coils in parallel. The stacking is done to achieve a Q of approximately 3 at 5 GHz. In the secondary coil, the first (second) coil was implemented using layers M6 and M5 (M4 and M3). The lower Q secondary coil does not affect the phase noise performance as it is only loaded by a lossless capacitor.

Simulations of the inductance and quality factors of the transformer windings, using ADS Momentum [42], are shown in Fig. 14. The self-resonance frequency is 18 GHz, which is much higher than the oscillation frequency.

### B. The Top Inductor

The top inductor value was chosen close to 2 nH with an ultra thick metal layer to ensure a high self-resonance frequency (23 GHz) and a high quality factor of 15 at the operating frequency. Since the self-resonance frequency is higher than the second harmonic frequency of the VCO, such a design choice ensures reliable coupling without introducing any phase shift.

### C. Tank Characteristics

In the proposed design $C \approx 1\,\mathrm{pF}$ and $C_{gs}$ of the MOSFETs was $\approx 100\,\mathrm{fF}$. These values ensure $C_{gs}$ is less than 10% of $C$. Therefore, as described in Section II-C, the simulated tank impedance, has only one resonance mode.

### D. The Varactor and Capacitor Bank

Both differential and quadrature versions of the VCOs were implemented and two variants of each VCO were designed. The first variant (VCO1/VCO3) has a 5% tuning range achieved by a MOS accumulation varactor tuning. The second variant (VCO2/VCO4) has a 20% tuning range with a 9 level, thermometer coded MIM capacitor bank for coarse tuning and a varactor for fine tuning. The switched capacitor bank was implemented using an architecture similar to [43], shown in Fig. 15(a).

### E. Output Buffer Design

The single-ended, half-sinusoidal VCO outputs were converted to a differential square wave by a sine-to-square converter with duty cycle correction as in [44], shown in Fig. 15(b). This is followed by a CML buffer with 50$\Omega$ output termination for measurement. The extracted simulation of the quadrature VCOs, including the buffers, shows a maximum phase error of $0.04^o$ across process and temperature corners in absence of random mismatches.

### *F. Limits on the Maximum Oscillation Amplitude*

Although an enhanced swing VCO can theoretically increase the output swing to a much larger value compared to the supply voltage, breakdown voltage considerations limit the output swing [4]. To alleviate this issue, special MOSFETs with a thick gate-oxide were used in the high supply voltage implementation of a class-F VCO in [25]. In the on-chip implementation of the proposed class-D VCO, standard MOSFETs were used and it was ensured that all the nodes swing within the technology specified breakdown voltage limits for a reliable operation.

As an added advantage, in a class-D VCO the source and the bulk terminals of the MOSFETs are kept at the same potential. This mitigates the possibility of accidentally forward biasing the source-bulk junction which is a potential problem in a Colpitts based enhanced swing architecture as in [4].

The MOSFET switch in the capacitor bank shown in Fig. 15 is also susceptible to breakdown. When the MOSFET is turned off, the gate is pulled down to ground. The source and drain of the MOSFET are pulled up to a voltage, $V_{DD,L}$, as shown in Fig. 16(a). The capacitors block the dc component. Therefore, the waveform at the MOSFET source or drain is a dc shifted version of the output signal. Since the output signal is enhanced swing in nature, the gate-to source or the gate-to-drain swing of the MOSFET can go beyond the breakdown specification. In order to avoid this issue, $V_{DD,L}$ was kept sufficiently low ($\leq 700\,\mathrm{mV}$).

When the MOSFET switch is 'on', the gate is pulled to a high voltage, $V_{DD,H}$ and the source and drain quiescent voltages are pulled down to the ground, as shown in Fig. 16(b). In this configuration, there is no breakdown issue. $V_{DD,H}$ was kept sufficiently high to reduce the MOSFET 'on' resistance.

## IV. Measurement Results

The core areas (excluding the output buffers) of the two quadrature (differential) VCOs are $0.35\,mm^2$ $(0.17\,mm^2)$ and $0.40\,mm^2$ $(0.19\,mm^2)$, respectively. A die micro-graph with the four

VCOs is shown in Fig. 17.

The phase noise and tuning range measurements of the prototype differential and quadrature class-D VCOs were performed using an Agilent E5052A signal source analyzer. All measurements were taken using the single-ended outputs. The output carrier power level, at the CML buffer output was amplified using a Mini Circuits TB-409-39+ low noise amplifier module. All the measurement results use the following bias voltages, $V_D = 350\,\mathrm{mV}$, $V_G = 400\,\mathrm{mV}$, $V_{DD,L} = 700\,\mathrm{mV}$, and $V_{DD,H} = 1\,\mathrm{V}$. These bias voltages were generated by an off chip low noise regulator.

### *A. Tuning Characteristics*

The measured tuning characteristics of the quadrature VCOs are shown in Fig. 18. The measured VCO gains for the two quadrature VCOs (VCO1 and VCO2) over the entire frequency range were found to be, $132 - 160\,\mathrm{MHz/V}$ and $51 - 255\,\mathrm{MHz/V}$, respectively, with a 350 mV supply. The tuning characteristics of the two differential VCOs (VCO3 and VCO4) were found to be very similar to VCO1 and VCO2, respectively, and are not shown.

*1) Supply Pushing:* The supply pushing characteristics for the quadrature VCO are shown in Fig. 19. This is superior compared to the performance reported in [24].

### *B. Phase Noise Performance*

The measured noise characteristics of the quadrature and differential VCOs are shown in Figs. 20 (a) and (b), respectively. For VCOs 1 and 3 at a 5 GHz oscillation frequency, the phase noise at 3 MHz offset is -137.1 dBc/Hz, and -133.9 dBc/Hz, respectively. For VCOs 2 and 4 at a 4.5 GHz oscillation frequency, the phase noise at 3 MHz offset is -135.2 dBc/Hz and -132.3 dBc/Hz, respectively. The $1/f^3$ noise corner for all the measured VCOs was found to be between $1 - 2$ MHz.

The measured phase noise was approximately 1.5 dB lower than the simulated values shown in Fig. 12 (c). The performance improvement is attributed to the quality factor of the transformer. In the electromagnetic simulations in ADS [42] the substrate was modeled as a standard lightly doped p-type substrate. However, a substrate passivation layer was used to reduce the eddy current losses. The increased substrate resistivity was shown to improve the Q. An increased Q reduces the phase noise.

### *C. Performance Summary*

The $FoM_T$ is a performance metric of a VCO that takes into account its tuning range [45]. The power consumption, phase error, $FoM$, $FoM_T$, and a comparison with the state-of-the art VCOs are reported in Tables I and II.

The phase error can be accurately measured using an on-chip mixer [11], [12]. Instead of using such a mixer, a symmetric layout was used in the buffer layout and the PCB traces. However, this approach does not compensate for any extra delay from the output buffer or the CML buffer mismatch. The probable cause for the large measured phase error in Table I is the combined effects of the tank mismatch and the output buffer mismatch.

The FoM of VCO1 is approximately 2.3 dB better than the prior work in [9]. The proposed class-D quadrature VCO achieves the best performance at the lowest supply voltage. The $FoM_T$ is also one of the highest among the LC oscillators with a single oscillation mode that uses only capacitor bank switching.

## V. Conclusion

Differential and quadrature low voltage class-D VCOs with a 5 GHz center frequency, implemented in a 65 nm CMOS process were reported in this work. These VCOs improve the carrier power by swing enhancement and thus reduce the output phase noise. The measured phase noise from a prototype test-chip was comparable to prior state-of-the art high voltage, current biased,

CMOS LC VCOs. The class-D mode of operation enable the quadrature VCO to achieve the best FoM to date at the lowest supply voltage.

## ACKNOWLEDGMENTS

The authors would like to thank, Berkeley Design Automation for the Analog Fast Spice (AFS) simulator, Thomas Brown and Satwik Patnaik of Intel for their help with testing, Saurabh Saxena and Amr Elshazly for the output and CML buffer design, Romesh Nandwana for useful discussions, and the anonymous reviewers for their valuable comments for improving the quality of the paper.

## APPENDIX A

*Oscillation Frequency Calculation*

The oscillation frequency of a class-D VCO was calculated in [24], based on the oscillator's transient characteristics. This method can be extended to the proposed class-D VCO architecture.

The LC tank of the class-D VCO in Fig. 21 (a) can be redrawn using a $T-\pi$ (or $Y-\Delta$) transformation [32] as shown in Fig. 21 (b). If the inductors have a high quality factor, the equivalent component values in the $\pi$ network are given by,

$$\begin{aligned} L_p &= L\left(1+\frac{L}{4L_{top}}\right) \\ L_1 &= \frac{L}{2}+2L_{top} \end{aligned} \tag{8}$$

Figs. 21 (c) and (d) show the equivalent circuits of the VCO in Fig. 21 (b), when MOSFETs $M_1$ and $M_2$ are 'on', respectively. Both $M_1$ and $M_2$ are 'on' for approximately half of the oscillation time-period, $T_{osc}$. $M_1$ is 'on' during the time interval $T_1$ and 'off' during $T_2$. The simulated periodic waveforms of $i_{L_1}(t)$, $v_C(t)$, and $i_{L_p}(t)$ for the $\pi$-equivalent VCO in Fig. 21 (b) are shown in Fig. 21 (e).

From [24] and also as seen from the simulated waveforms,

$$T_1 = T_2 = \frac{T_{osc}}{2} \tag{9}$$

The loss components of $L_1$ and $L_p$ have been modeled by the resistors, $R_1$ and $R_p$, respectively. During $T_1$, $\left(0 \leq t \leq \frac{T_{osc}}{2}\right)$, inductor $L_1$ is shorted to ground through the resistor $R_1$, as shown in Fig. 21 (c). Therefore, $i_{L_1}(t)$ can be expressed as,

$$i_{L_1}(t) = i_{L_1}(0) + \frac{V_{DD}}{R_1}\left(1 - e^{-R_1 t/L_1}\right) \tag{10}$$

At $t = \frac{T_{osc}}{2}$, $M_1$ turns off, $M_2$ turns 'on', and the time interval $T_2$, $\left(\frac{T_{osc}}{2} \leq t \leq T_{osc}\right)$ starts. During $T_2$, inductor $L_1$ is connected to ground via an RLC network as shown in Fig. 21 (d). In Fig. 21 (e), $v_C\left(\frac{T_{osc}}{2}\right) = 0\,\mathrm{V}$ and the current across the inductor $L_p$ is at its minimum value, $i_{L_p,min}$. $i_{L_1}\left(\frac{T_{osc}}{2}\right)$ can be calculated using Eq. (10) and remains unchanged when the oscillator transitions from time interval $T_1$ to $T_2$. The equivalent Laplace domain network representation during $T_2$, including all the initial conditions is shown in Fig. 21 (f).

The oscillation frequency, $\omega_{osc}$ is calculated assuming that the network has a negligible loss [24]. A low loss assumption means that during $T_2$, $R_1 \approx 0$ and $R_p \approx \infty$ in the network in Fig. 21 (f). Therefore, the current in the Laplace domain, $I_{L_1}(s)$ can be expressed as,

$$\begin{aligned} I_{L_1}(s) = {} & \frac{V_{DD}}{s^2(L_1+L_p)}\left[\frac{1+s^2L_pC}{1+s^2\left(\frac{L_1L_p}{L_1+L_p}\right)C}\right] + \frac{L_1 i_{L_1}\left(\frac{T_{osc}}{2}\right)}{s(L_1+L_p)}\left[\frac{1+s^2L_pC}{1+s^2\left(\frac{L_1L_p}{L_1+L_p}\right)C}\right] \\ & + \frac{L_p i_{L_p,min}}{s(L_1+L_p)}\left[\frac{1}{1+s^2\left(\frac{L_1L_p}{L_1+L_p}\right)C}\right] \end{aligned} \tag{11}$$

Since $L_1 \gg L_p$ (a design choice), Eq. (11) can be simplified to,

$$I_{L_1}(s) = \frac{V_{DD}}{s^2 L_1} + \frac{i_{L_1}\left(\frac{T_{osc}}{2}\right)}{s} + \frac{L_p i_{L_{p,min}}}{sL_1}\left[\frac{1}{1+s^2 L_p C}\right] \tag{12}$$

Therefore, during $T_2$,

$$i_{L_1}(t) = \frac{V_{DD}}{L_1}\left(t - \frac{T_{osc}}{2}\right) + i_{L_1}\left(\frac{T_{osc}}{2}\right) + \frac{L_p i_{L_{p,min}}}{L_1} - \frac{L_p i_{L_{p,min}}}{L_1}\cos\left[\omega_{tank}\left(t - \frac{T_{osc}}{2}\right)\right] \tag{13}$$

where $\omega_{tank} = \frac{1}{\sqrt{\left(\frac{L_1 L_p}{L_1+L_p}\right)C}} \approx \frac{1}{\sqrt{L_p C}}$.

At $t = T_{osc}$,

$$i_{L_1}(T_{osc}) = \frac{V_{DD}}{L_1}\left(\frac{T_{osc}}{2}\right) + i_{L_1}\left(\frac{T_{osc}}{2}\right) + \frac{L_p i_{L_{p,min}}}{L_1} - \frac{L_p i_{L_{p,min}}}{L_1}\cos\left[\frac{\omega_{tank} T_{osc}}{2}\right] \tag{14}$$

Since $T_{osc}$ is the oscillation period,

$$i_{L_1}(0) = i_{L_1}(T_{osc}) \tag{15}$$

As the RLC network has a negligible loss, the following two equations hold [24],

$$i_{L_1}\left(\frac{T_{osc}}{2}\right) = i_{L_1}(0) + \frac{V_{DD}}{L_1}\frac{T_{osc}}{2} \tag{16}$$

$$i_{L_1}(0) = -i_{L_1}\left(\frac{T_{osc}}{2}\right) \tag{17}$$

Substituting Eqs. (15), (16), and (17), in Eq. (14) and upon simplification,

$$1 - \cos\left[\frac{\omega_{tank} T_{osc}}{2}\right] = -\frac{V_{DD} T_{osc}}{L_p i_{L_{p,min}}} \tag{18}$$

As described in Sections II-D and II-E, the differential voltage waveform across the RLC tank is sinusoidal with an oscillation amplitude, $A \approx \pi V_{DD}$. Since the peak voltage across $L_p$ is $\pi V_{DD}$, the minimum current through it is given by,

$$i_{L_p,min} = - \frac{\pi V_{DD}}{\omega_{osc} L_p} \tag{19}$$

where, $\omega_{osc} = \frac{2\pi}{T_{osc}}$ is the oscillation frequency.

By using Eq. (19) in Eq. (18),

$$\cos\left[\frac{\omega_{tank} T_{osc}}{2}\right] = -1 \tag{20}$$

Therefore, $\omega_{osc}$ is given by,

$$\omega_{osc} = \omega_{tank} \approx \frac{1}{\sqrt{L_p C}} \tag{21}$$

This expression for the oscillation frequency is valid when $L_1 \gg L_p$. Using Eq. (8) this design requirement can be simplified to, $L_{top} \gg \frac{L}{2}$ and $\omega_{osc} = \frac{1}{\sqrt{LC}}$. Therefore, with an $L_{top} \gg 0.5L$, the oscillation frequency approaches the resonance frequency of the tank.

The oscillation frequency analysis described above is simplified by using a $T-\pi$ transformation and Eq. (6). However, using a method similar to [24] the oscillation frequency can be calculated directly from the $T$ network in Fig. 21(a) without resorting to Eq. (6) (a topic of future work).

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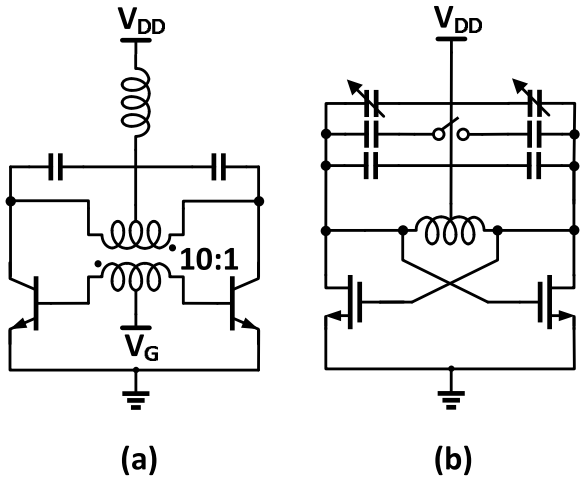


Fig. 1. Differential class-D VCOs: (a) Discrete implementation by Baxandall, (b) Fanori and Andreani's implementation.

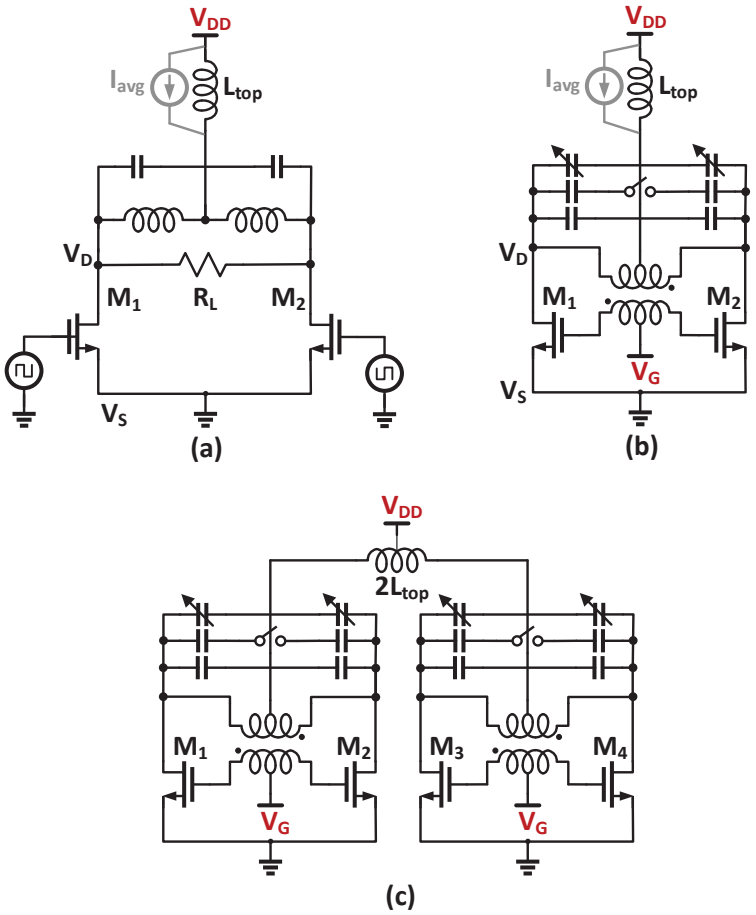


Fig. 2. (a) A current-mode class-D PA. (b) Proposed differential VCO cell with a bias shift. (c) Proposed quadrature class-D VCO with a super-harmonic coupling. For the VCOs, $R_L$ is the equivalent parallel resistance of the tank inductance. Therefore, it is not explicitly shown.

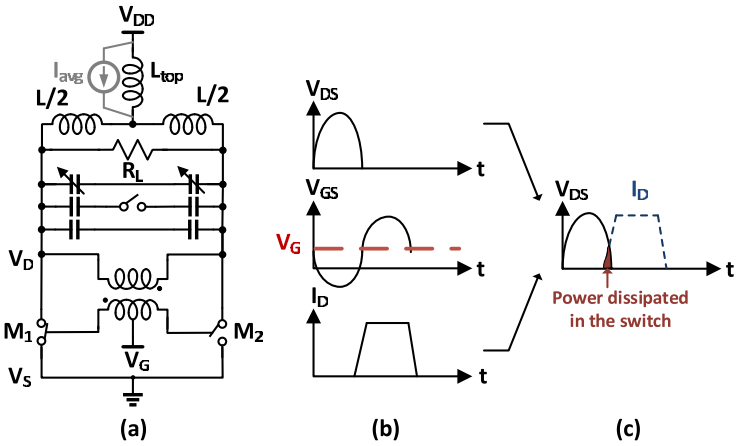


Fig. 3. (a) The equivalent circuit of the differential VCO cell with an ideal transformer, switches and inductance of the primary coil, drawn separately. (b) The waveform at the MOSFET nodes. (c) Conceptual plot of the power consumption in the MOSFET.

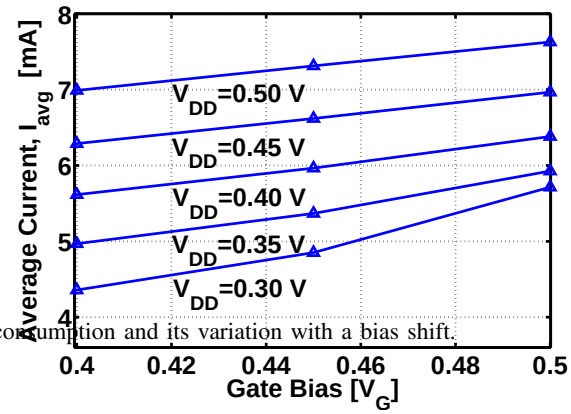


Fig. 4. Simulated average current consumption and its variation with a bias shift.

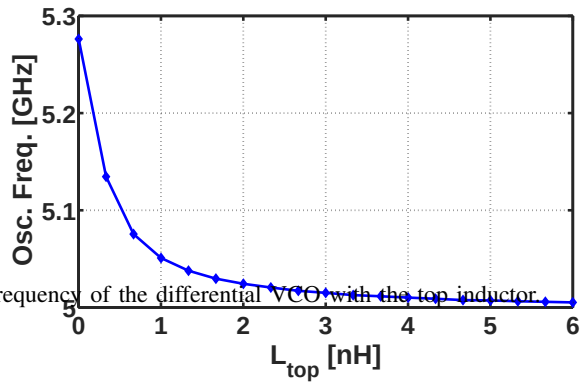


Fig. 5. Variation of the oscillation frequency of the differential VCO with the top inductor.

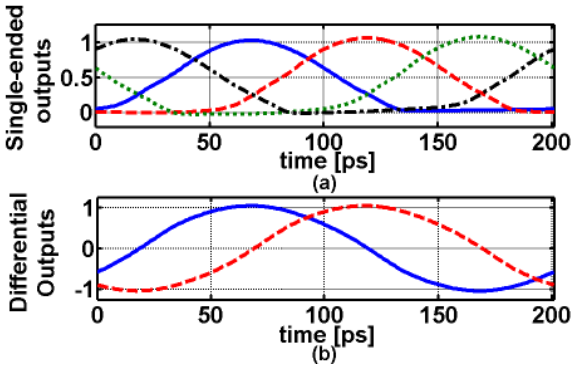


Fig. 6. (a) Simulated output voltages of (a) the four single-ended outputs of the quadrature VCO, (b) the differential outputs of the two cells of the VCO.

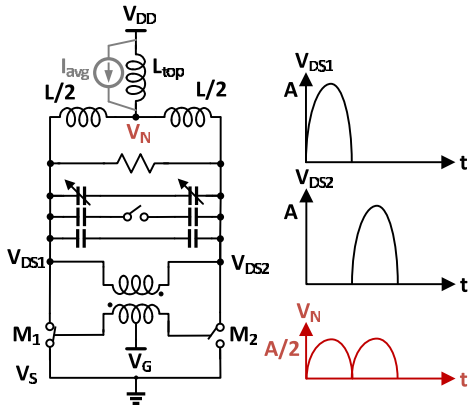


Fig. 7. The approximate waveform at the MOSFET drains and at the center tap of the primary side of the transformer ($V_N$).

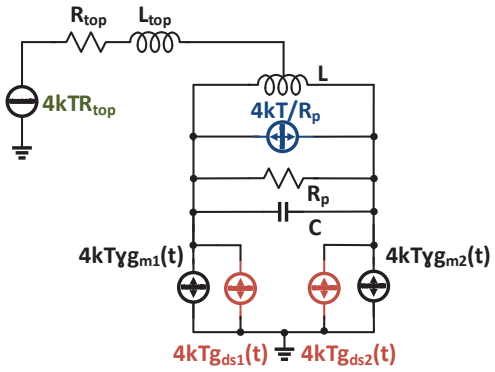


Fig. 8. Noise sources in a class-D VCO.

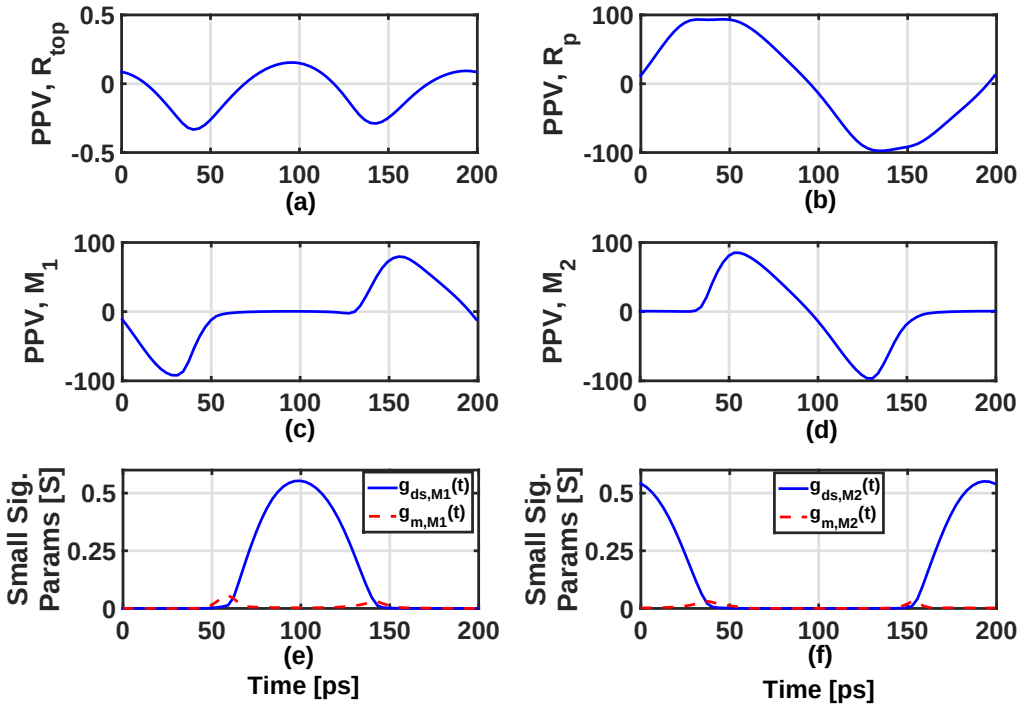


Fig. 9. Simulated values of PPV from different components, with a supply voltage, $V_{DD} = 350\,\mathrm{mV}$ and gate bias, $V_G = 400\,\mathrm{mV}$. 200 ps corresponds to one cycle of the oscillation. (a) PPV from $L_{top}$. (b) PPV from $R_p$. (c) PPV from $M_1$. (d) PPV from $M_2$. (e) Simulated $g_{ds}(t)$ and $g_m(t)$ waveforms for $M_1$. (f) Simulated $g_{ds}(t)$ and $g_m(t)$ waveforms for $M_2$.

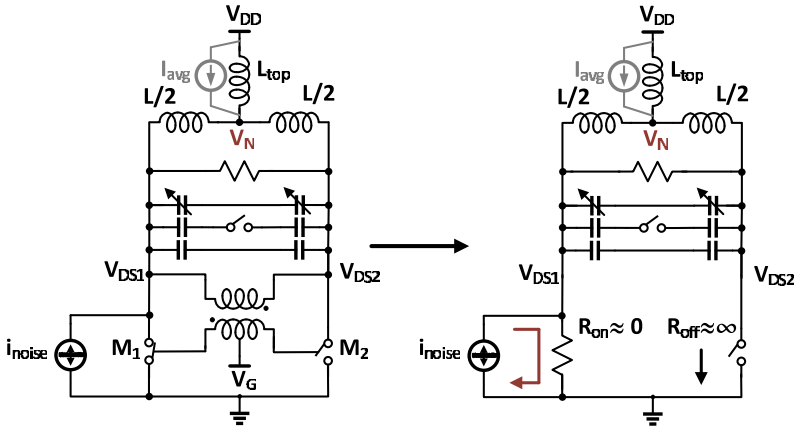


Fig. 10. Simplified schematic of the impedance seen by the noise source of an 'on' transistor in the class-D VCO.

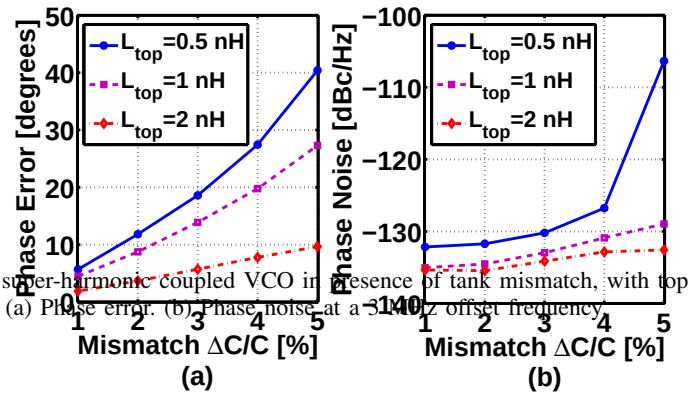


Fig. 11. Simulated response of a super-harmonic coupled VCO in presence of tank mismatch, with top inductor values of 0.5 nH, 1 nH, and 2 nH, respectively. (a) Phase error. (b) Phase noise at a 3 MHz offset frequency.

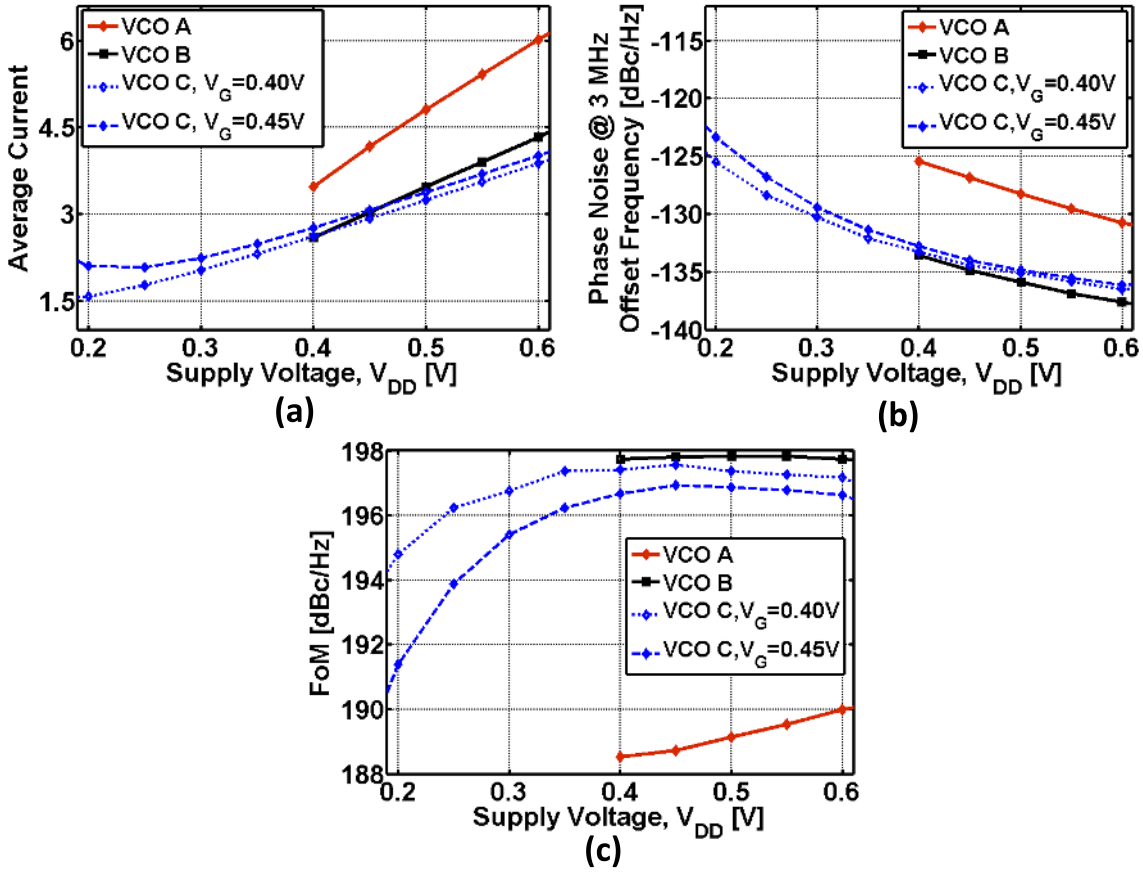


Fig. 12. Simulated performance comparison of Fanori and Andreani's architecture (VCO A), a modified Fanori and Andreani's architecture with a top-inductor (VCO B), and the proposed differential VCO cell with the top inductor and a bias shift (VCO C). VCO C starts oscillating with a sub 0.4 V supply. (a) Average current consumption. (b) Phase noise at a 3 MHz offset frequency. (c) Figure-of-Merit.

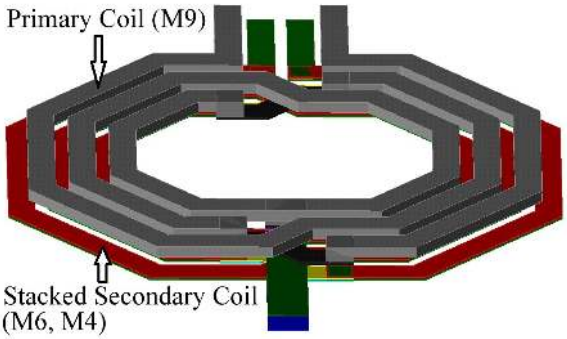


Fig. 13. The stacked transformer structure.

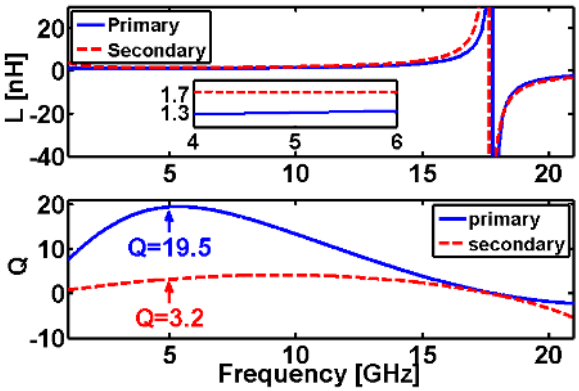


Fig. 14. Simulated transformer primary and secondary characteristics. The inset shows the inductances in 4-6 GHz frequency range.

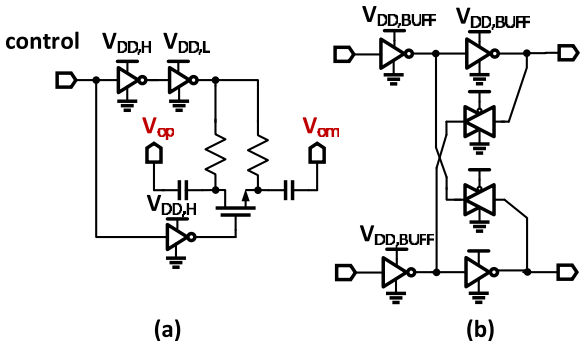


Fig. 15. Schematics of (a) capacitor bank, (b) level shifting VCO buffer.

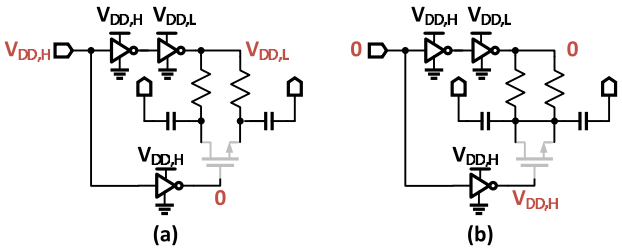


Fig. 16. (a) The MOSFET switch in 'off' mode. (a) The MOSFET switch in 'on' mode.

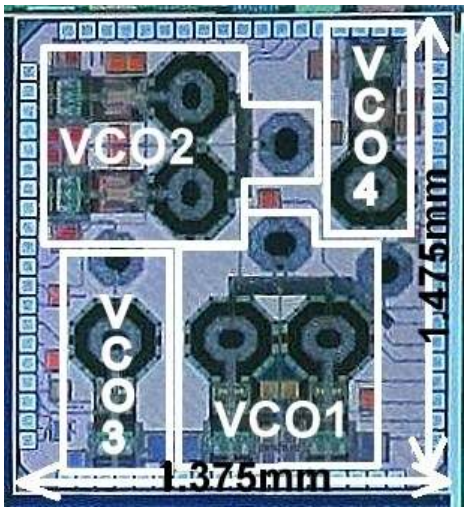


Fig. 17. Die micro-graph of quadrature VCO with varactor tuning (VCO1), quadrature VCO with cap-bank and varactor tuning (VCO2), differential VCO with varactor tuning (VCO3), and differential VCO with cap-bank and varactor tuning (VCO4).

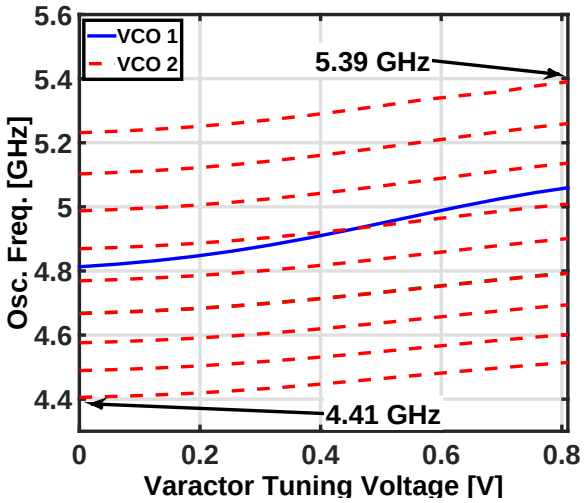


Fig. 18. Measured tuning characteristics of the two quadrature VCOs.

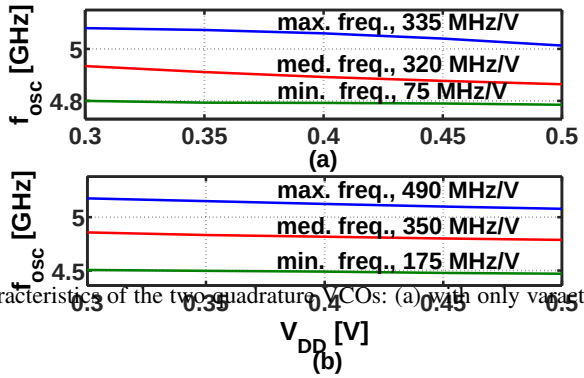


Fig. 19. Measured supply pushing characteristics of the two quadrature VCOs: (a) with only varactor based tuning, (b) capacitor bank and varactor based tuning.

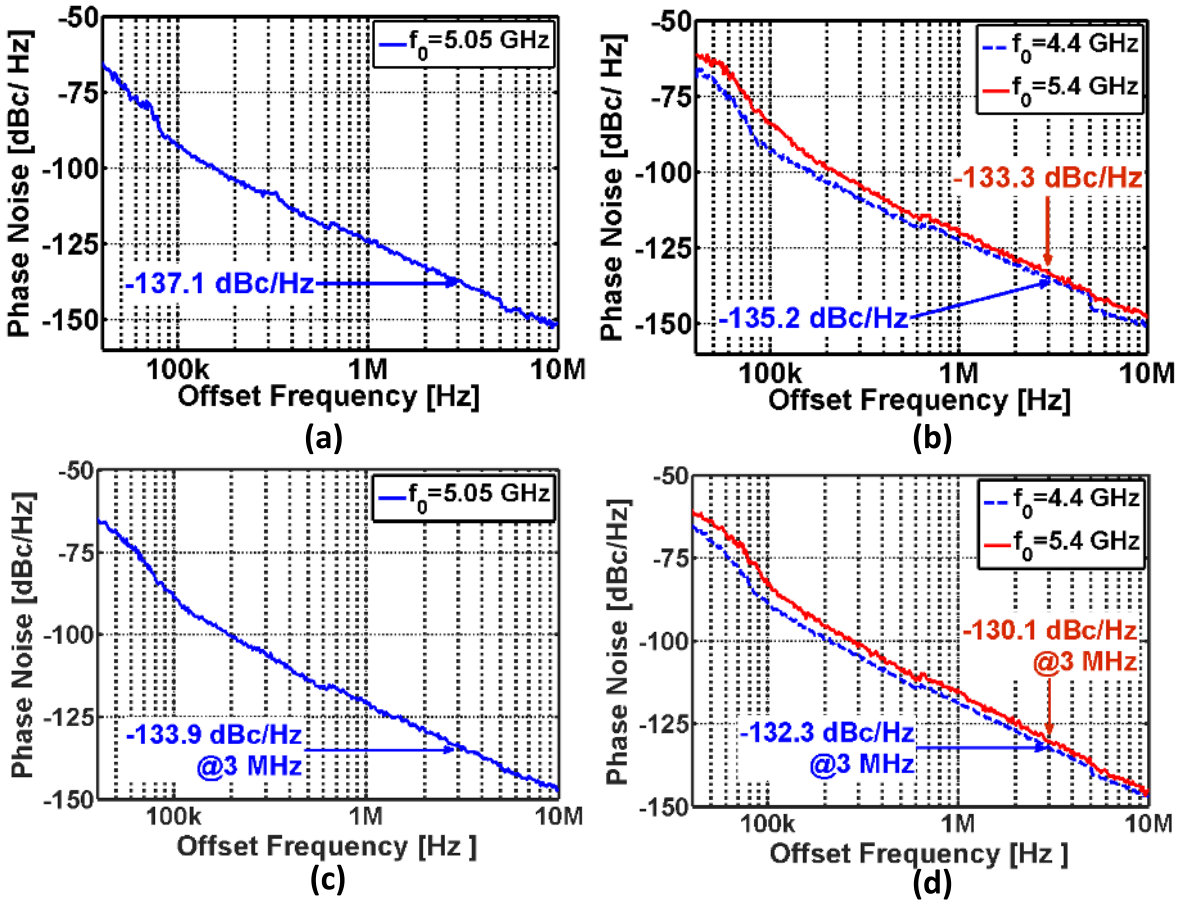


Fig. 20. Measured phase noise of the prototype VCOs at a supply voltage of 350 mV and gate bias of 400 mV (a) The quadrature VCO with only varactor based tuning (VCO1), (b) The quadrature VCO with capacitor bank and varactor based tuning (VCO2). (c) The differential VCO with only varactor based tuning (VCO3). (d) The differential VCO with capacitor bank and varactor based tuning (VCO4).

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED QUADRATURE VCO DESIGN AND A COMPARISON WITH THE STATE-OF-THE ART QUADRATURE VCOS.

| | [8] | [9] | [10] | [33] | This work | |
|---|---|---|---|---|---|---|
| | | | | | [w/ varactor] | [w/ cap-bank] |
| **Architecture Type/ Coupling Type** | X-Coupled/ LC Ring | X-Coupled/ Energy-Circulating | Enhanced Swing/ Capacitive | X-Coupled/ Super-harmonic | Class-D/ Super-harmonic | Class-D/ Super-harmonic |
| **Technology [nm]** | 130 | 180 | 130 | 250 | 65 | 65 |
| **Power Supply [V]** | 0.506 | 1.8 | 0.6 | 2.5 | 0.35 | 0.35 |
| **Freq./Offset Freq. [GHz/MHz]** | 5.121/1 | 5.3/1 | 5.6/3 | 4.88/1 | 5/3 | 4.4-5.4/3 |
| **Tuning Range [%]** | - | 1 | 4 | 12 | 5 | 20 |
| **Phase Error [°]** | 0.1 | - | 3 | 2.6 | 7** | 8** |
| **Phase Noise [dBc/Hz]** | -126.1 | -134.4 | -132.3 | -125 | -137.1 | -135.2--133.3 |
| **Osc. Core Area [mm²]** | 0.73 | 3.04 | 0.48 | - | 0.35 | 0.40 |
| **DC Power [mW]** | 4.1 | 20.7 | 4.2 | 22 | 2.1 | 2.6-2.3 |
| **FoM [dBc/Hz]** | 194.2 | 196 | 191.4 | 185 | 198.3 | 194.4-194.8 |
| **$FoM_T$ [dBc/Hz]** | - | 176 | 183.4 | 186.6 | 192.3 | 200.8 |

$$FoM = 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1\,mW}\right) - L\{\Delta f\} \qquad FoM_T = FoM + 20\log\left(\frac{TR[\%]}{10}\right)$$

**No on-chip mixer was used for measurement.

TABLE II
PERFORMANCE SUMMARY OF THE PROPOSED DIFFERENTIAL VCO DESIGN AND A COMPARISON WITH THE STATE-OF-THE ART DIFFERENTIAL VCOS.

| | [4] | [16] | [24] | [28] | This work | |
|---|---|---|---|---|---|---|
| | | | | | [w/ varactor] | [w/ cap bank] |
| **Architecture Type** | Enhanced Swing | Class-C | Class-D | Class-D | Class-D | Class-D |
| **Technology [nm]** | 130 | 130 | 65 | 65 | 65 | 65 |
| **Power Supply [V]** | 0.475 | 1 | 0.4-0.6 | 0.4 | 0.35 | 0.35 |
| **Freq./Offset Freq. [GHz/MHz]** | 4.9/3 | 4.9/3 | 2.5-3.3/5 | 2.4-5.3/10 | 5/3 | 4.4-5.4/3 |
| **Tuning Range [%]** | 3 | 14 | 28 | 75 | 5 | 20 |
| **Phase Noise [dBc/Hz]** | -136.2 | -133 | -144 | -149/-139 | -133.9 | -132.3--130.1 |
| **Osc. Core Area [mm²]** | 0.28 | - | 0.19 | - | 0.17 | 0.19 |
| **DC Power [mW]** | 2.7 | 1.4 | 6 | 4.4-6 | 1.3 | 1.65-1.5 |
| **FoM [dBc/Hz]** | 196.2 | 196 | 189/190 | 187-189 | 197.4 | 193.4-193.5 |
| **$FoM_T$ [dBc/Hz]** | 184.2 | 198.9 | 198.9 | 206 | 191.4 | 199.7 |

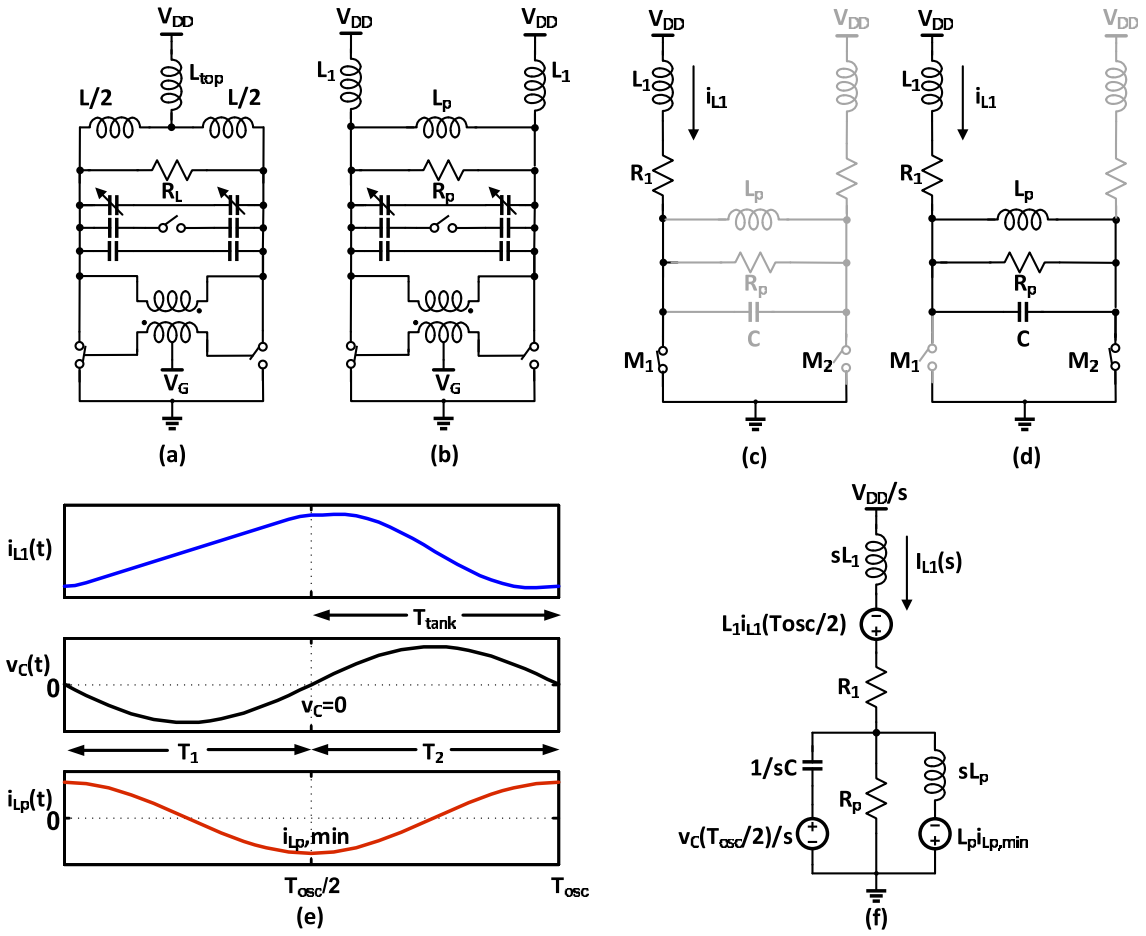


Fig. 21. (a) The proposed class-D differential VCO cell. (b) $\pi$ equivalent of the VCO cell in (a). (c) Equivalent circuit of the VCO when $M_1$ is 'on'. (d) Equivalent circuit of the VCO when $M_2$ is 'on'. (e) Simulated periodic waveforms of the VCO circuit in (b). (f) Laplace domain equivalent circuit of the VCO when $M_2$ is 'on' (circuit in (d)).