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360 nW Gate-Driven Ultra-Low Voltage CMOS Linear Transconductor with 1 MHz Bandwidth and Wide Input Range

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***Abstract*— A low voltage linear transconductor is introduced. The circuit is a pseudo differential architecture that operates with ±0.2V supplies and uses 900nA total biasing current. It employs a floating battery technique to achieve low voltage operation. The transconductor has a 1MHz bandwidth. It exhibits a SNR = 72dB, SFDR = 42dB and THD = 0.83% for a 100mVpp 10kHz sinusoidal input signal. Moreover, stability is not affected by the capacitance of the signal source. The circuit has been validated with a prototype chip fabricated in a 130nm CMOS technology.**

***Index Terms*—Analog integrated circuits, low-power, low voltage, linear operational transconductance amplifier.**

I. Introduction

Linear voltage-to-current converters (transconductors or OTAs) and operational amplifiers (OP-AMPs) are core circuits of analog IC design. A transconductor that is linear over a wide differential input signal range V_d is a key element to implement current-mode and OTA-C systems. Some examples of the utilization of OTAs are: wide-band amplifiers, high frequency gm-C filters [1][2], multipliers [3] and precision rectifiers [4], among many others.

Transconductors are used in current mode feedforward systems with only low impedance (high frequency) and low swing nodes in the signal path. These systems mainly rely on current mirrors [5] and they can have very wide bandwidth.

Conventional transconductor and OP-AMP architectures use a differential input stage. The headroom of the differential pair HR_{DP} constrains the differential and common mode input swing to a relatively small value $V_{ppswing}=V_{supply}-HR_{DP}$, where $HR_{DP}\sim V_{GS}+V_{DSsat}$. The headroom is directly affected by V_{supply}. With the scaling down of CMOS fabrication technologies, the nominal supply voltage has continuously decreased. On the other hand, the threshold voltage of PMOS and NMOS transistors has not been reduced at the same rate. As a comparison example a 130nm CMOS process has a nominal supply voltage V_{supply}=1.2V and PMOS and NMOS threshold voltages $V_{THN} \approx | V_{THP} | \approx 0.4$V. While for a 16nm CMOS process supply voltage has been reduced to V_{supply}=0.7V while the threshold voltage is approximately the same $V_{TH}\approx$0.4V. This limits the portability of a circuit design with scaling down of CMOS technologies.

Even in older technologies that can use higher supply voltages it is convenient to operate with very low supply voltages in order to achieve very low power dissipation which is of paramount importance in some applications such as biomedical [6][7] and wireless applications.

Subthreshold operation of MOS transistors is a natural option for low voltage systems because it allows gate-source voltages lower than V_{TH} which lessen supply requirements [8].

Another technique that allows operation of linear transconductors with very low supply voltages and with close to rail to rail differential input swing is based on floating gate transistors [9]. They use capacitive voltage dividers to reduce swing at the input terminals of the transconductor and to shift the DC common mode input voltage at the gates of the differential pair close to one of the rails in order to provide additional headroom for the input differential pair. Since they are based on charge conservation, they cannot be used in CMOS technologies with gate leakage. Quasi floating gate techniques [10][11] allow implementation of dynamic low voltage transconductors with wider differential input range. Due to their dynamic nature and the utilization of pseudo resistors implementing very large resistive elements they may have large turn on times.

Another technique that allows implementation of low voltage linear OTA's is the bulk driven (BD) technique [12]-[15]. In this technique input signals are injected at the bulk terminals rather than at the gate terminals of the MOS transistor. In order to avoid forward biasing of the bulk PN junctions at the input terminals of the MOS transistor the differential (and common mode) input swing is limited to approximately ±0.3V. Larger swings result in very large input currents that load the input signal source.

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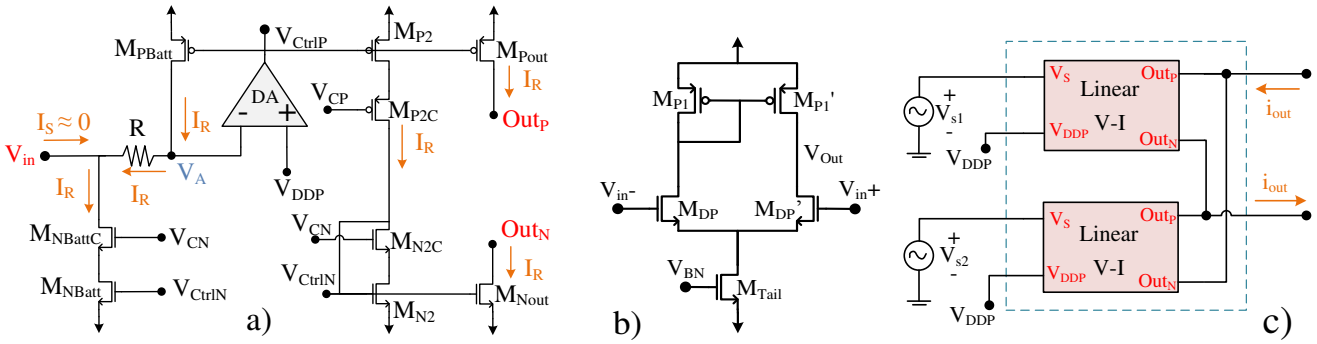

Fig. 1 a) Low voltage linear V-I conversion unit. b) Transistor level implementation of the differential amplifier (DA). c) Low voltage OTA with differential input $V_d=V_{s1}-V_{s2}$ and complementary output currents using two linear V to I conversion units.

Both the floating gate technique and the bulk driven technique suffer from significant degradation (typically a factor 5 or higher) of input noise, input offset voltage and of the gain-bandwidth (GB) product. In floating gate circuits this is caused by the input capacitive divider, while, in bulk-driven circuits it is due to the fact that the bulk transconductance gain g_{mb} is approximately a factor 5 smaller than the main transconductance gain g_m.

A gate-driven technique to implement low voltage OTAs is based on CMOS inverters [16]. In this technique in order to keep linear transconductance both inverter transistors must be on at all times. For this reason (similar to BD circuits) the technique of [16] has very small signal swing $V_{swingpp}=V_{supply}-V_{GS}-V_{SG}$, with low supply voltage. Other limitations that affect this technique are that the transconductance is strongly supply and temperature dependent, it has poor CMRR and the quiescent current (static power dissipation) is also strongly dependent on the common mode input voltage.

In this paper we report and show experimental verification of a gate-driven differential linear voltage-to-current converter that operates with ±0.2V supply voltages, with large differential and common mode input signal range and without the GB, offset and noise degradation associated with floating gate and bulk driven circuits. In addition, the transconductor has high input impedance and high CMRR.

This paper is organized as follows: Section II describes the proposed circuit. The AC and noise analysis are presented in Sections III and 0, respectively. In Section V the simulated and experimental results of a test chip are discussed. Conclusions are presented in Section VI.

II. Circuit Description

Fig. 1a shows an auxiliary circuit used to implement a wide input range low-voltage linear V to I conversion unit. The differential amplifier (DA) with NMOS input transistors used in this circuit is shown in Fig. 1b. The circuit of Fig. 1a operates as follows:

The positive input terminal of the DA is connected to a voltage V_{DDP} which is very close to V_{DD}, ($V_{DDP}\approx V_{DD}$-0.07V). This provides a headroom for the DA with value $HR_{DP}= V_{supply}$ - 0.07V which allows the circuit to operate with a minimum supply voltage $V_{supplyMin}=HR_{DP}=V_{GS}+V_{DSsat}$. A current I_R is generated by connecting the voltages V_{CtrlP} and voltage V_{CtrlN} at the gates of transistors M_{PBatt} and M_{NBatt}. They generate equal sourcing and sinking currents I_R that flow through R and have a value that satisfies the conditions of eq. (1) and (2), where $I_Q=V_{DDP}/R$ and $i_s=V_s/R$. This causes the voltage V_A at the negative input terminal of the DA to have a value V_{DDP} equal to the voltage at the positive input terminal. Note that the current I_s supplied by the signal source V_S is ideally zero. This avoids loading the signal source V_s by the V to I conversion unit. Additional sinking and sourcing (eventually scaled) replicas of the current I_R can be generated using the voltages V_{CtrlP} and V_{CtrlN} to drive PMOS and NMOS transistors.

$$I_R = \frac{V_{DDP}-V_s}{R} = \frac{V_{DDP}}{R} - \frac{V_s}{R} \quad (1)$$

$$I_R = I_Q - i_s \quad (2)$$

The generation of complementary output current signals $\pm i_{out}$ free from the offset term I_Q and common mode components requires two auxiliary V-I conversion circuits with their input terminals connected to differential input signals V_{s1} and V_{s2} as shown in Fig. 1c. The two V-I converters generate sinking and sourcing currents with values $I_{R1}=I_Q-V_{s1}/R$ and $I_{R2}=I_Q-V_{s2}/R$ that are used to generate complementary offset free output currents $\pm i_{out}=\pm(V_{s1}-V_{s2})/R$. The transconductor has a transconductance gain $g_{mOTA}= i_{out}/(V_{s1}-V_{s2})=1/R$.

Note that V_{DDP} has a value $V_{DDP}=V_{DD}$ - 0.07V to leave headroom for the PMOS transistor M_{PBatt} in Fig. 1a to operate as a current source. The output voltage range is limited by the drain-source saturation voltage of transistors M_{PBatt}, M_{NBattC} and M_{NBatt}, to a value $V_s=(V_{DD}-V_{SS})-2|V_{DSsat}|\approx$ 0.26V. (assuming V_{supply}=0.4V and V_{DSsat}=0.07V). On the input side the range is also limited in the positive direction by the voltage V_{DDP} since the input signal cannot be higher than V_{DDP}. Although linear V to I conversion is achieved using the DA with negative feedback the bandwidth of the V-I conversion can be high since it is a local feedback loop with only parasitic capacitances at all nodes in the circuit of Fig. 1a. If necessary, a small compensation capacitance Cc can be used at node V_{CtrlP} of the DA to generate a dominant pole that achieves a phase margin greater than 60°. A detailed analysis is presented in the following section.

The proposed approach is based on two single ended circuits in parallel and can be classified as a pseudo differential scheme. In most pseudo differential systems (like an MOS differential amplifier with its sources connected to a rail)

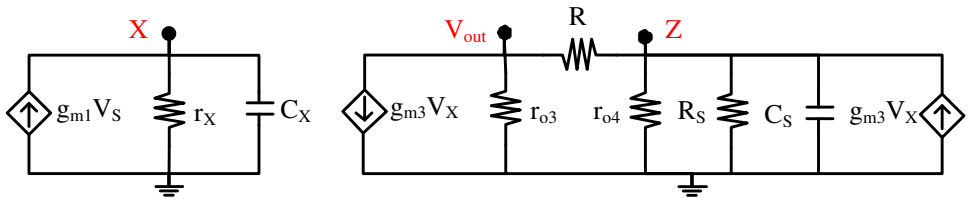

Fig. 2 Small signal representation of battery and output branch.

common mode and static current components are strongly dependent on the common mode input voltage which can lead to large and unpredictable common mode drain current values. In pseudo differential pairs drain currents have a strong nonlinear dependency on the input static and common mode voltages, on transistor parameters and on temperature. In the presence of a common mode voltage V_{CM}, the common mode current i_{CM} varies following the transistor square law in strong inversion or has an exponential dependence when the transistors operates in subthreshold. This can cause the power dissipation of a circuit with a pseudo differential MOS amplifier to increase significantly with the common mode input voltage $V_{CM.}$ This is not the case for the scheme presented here. If V_{s1},V_{S2} are non-complementary voltages and have a common mode input component $V_{CM}=(V_{s1}+V_{s2})/2$, then I_{R1} and I_{R2} will be given by (3) and (4). Where $V_d=V_{s1}-V_{s2}$, $i_{out}=V_d/2R$ and $I_{CM}=(V_{s1}+V_{s2})/2R$. Although the proposed architecture can be considered as a pseudo differential scheme, it offers the advantage of having a well-defined common mode current I_{CM}. This current is linearly dependent on V_{CM} and on $G=1/R$. Moreover, its maximum value I_{CMMAX} is reached when $V_{CM}= V_{SS}+V_{DSsat}$ and is less than twice the quiescent current.

The common mode current I_{CM} along with the quiescent current I_Q that appears in I_{R1} and I_{R2} are cancelled when the current i_{out} is derived.

$$I_{R1}=\frac{V_{DDP}-(V_{CM}+(V_d/2))}{R}=I_Q-I_{CM}-\frac{i_{out}}{2} \quad (3)$$

$$I_{R2}=\frac{V_{DDP}-(V_{CM}-(V_d/2))}{R}=I_Q-I_{CM}+\frac{i_{out}}{2} \quad (4)$$

If required, the transconductance can be made tunable by: a) replacing R by an MOS transistor in triode region such that the resistance can be controlled by the gate voltage of the transistor, b) utilization of gain programmable current mirrors in the V to I conversion unit.

III. AC Analysis

A simplified AC equivalent circuit to derive the open loop gain of the circuit of Fig. 1a is shown in Fig. 3 whose small signal representation is shown in Fig. 2. The feedback loop is opened, and a test voltage V_S is applied at the gate of M_1. The signal source V_s applied at node Z is represented only by its internal impedance R_s in parallel with C_s. The resistance R_s is assumed to satisfy the condition $R_s<<r_o$. The case of a high impedance signal source R_s~r_o (or higher) is not of interest since a high impedance source performs already as a current source and for this reason a voltage to current conversion is not required.

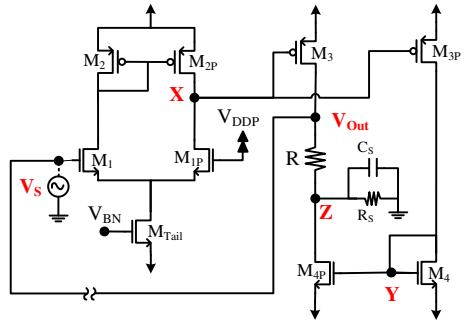

Fig. 3 Simplified equivalent circuit of Fig. 1a with non-ideal signal source V_s.

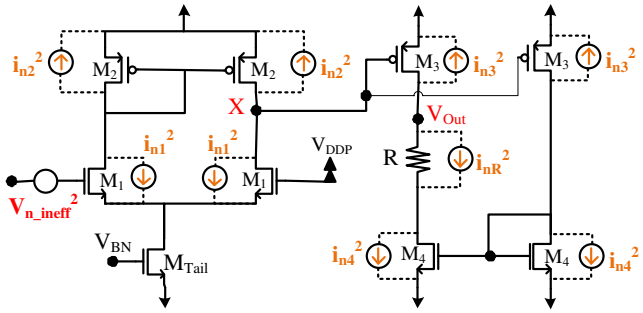

Fig. 4 Circuit representation for noise analysis.

Assuming $r_o>>R$, R_s, $1/g_m$ it can be shown that the open loop gain A_{OL} is approximately given by (5), having a single pole ω_{PX} defined by (9), where C_X and r_X are the capacitance and resistance at node X, being $r_X=r_{o1}||r_{o2}$.

The open loop DC gain (A_{OLDC}) is expressed in (6), where A_I (7) is the gain of the first stage and A_{II} (8) is the gain of the second stage, (V_{out}/V_S corresponds to the negative of the open loop gain). For the second stage there is a pole-zero cancellation.

The gain bandwidth product (GB) of the circuit is given by (10). From this equation it can be seen that the circuit performs approximately as a one pole system with high GB. Therefore, the impact of the source capacitance on the stability of the circuit can be neglected.

$$A_{OL}=\frac{A_{OLDC}}{1+(s/\omega_{PX})} \quad (5)$$

$$A_{OLDC}=\mid A_I A_{II} \mid = g_{m1}r_X \cdot g_{m3}R \quad (6)$$

$$A_I = g_{m1}r_X \quad (7)$$

$$A_{II}=-g_{m3}R \quad (8)$$

$$\omega_{PX}=\frac{1}{r_X C_X} \quad (9)$$

$$GB=A_{OLDC}\cdot\omega_{PX}=\frac{g_{m1}A_{II}}{C_X} \quad (10)$$

TABLE I PERFORMANCE AND DESIGN PARAMETERS OF LOW-VOLTAGE LINEAR TRANSCONDUCTOR

Parameter	Value	Parameter	Value
g_{mOTA}(µA/V)	0.769	I_{BIAS} (µA)	0.1
W_{PMOS} (µm)	18	Supply Voltage (V)	±0.2
W_{NMOS} (µm)	2.88	A_{OL} (dB)	37.4
$L_{PMOS\,/\,NMOS}$ (nm)	360	f_{-3dB} OTA(MHz)	1.099
R (MΩ)	1.3	GB (kHz)	600
R_L (MΩ)	1.3	Phase Margin (°)	52
V_{DDP} (V)	0.12	Rout (MΩ)	100

* with short circuit at output
** with open circuit at output

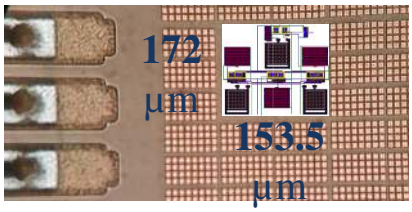

Fig. 5 Microphotograph of the fabricated chip with the layout.

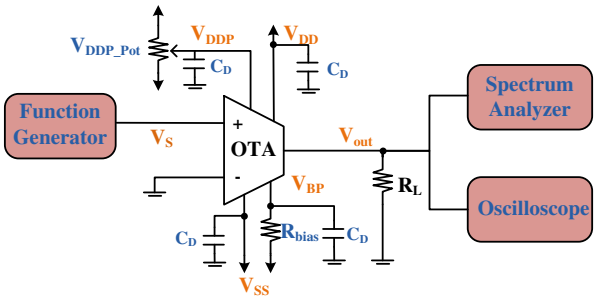

Fig. 6 Testbench diagram of the low voltage OTA with external components and equipment.

IV. NOISE ANALYSIS

The noise representation of the circuit of Fig. 1a is shown in Fig. *4* that includes noise current sources. The noise analysis of this circuit, assuming $A_1>>1$, leads to an equivalent input noise voltage approximately given by (11). This expression includes the thermal and 1/*f* noises. The noise bandwidth is given by (12). In the specific case of thermal noise, it is given by (13). If $g_{m1}\approx g_{m2}$ the squared RMS noise V_{RMS}^2 is given by (14).

$$V_{n\_ineff}^{\ 2} = 2i_{n1}^{\ 2}\left(1+\frac{i_{n2}^{\ 2}}{i_{n1}^{\ 2}}\right)\frac{1}{g_{m1}^{\ 2}} \tag{11}$$

$$BW_{noise} = \frac{\pi}{2}GB = \frac{g_{m1}}{4C_X} \tag{12}$$

$$V_{RMS}^{\ 2} = V_{n\_ineff}^{\ 2}\cdot BW_{noise} = \frac{2\left(1+(g_{m2}/g_{m1})\right)}{3}\frac{kT}{C_X} \tag{13}$$

$$V_{RMS}^{\ 2} = \frac{4}{3}\frac{kT}{C_X} \tag{14}$$

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed circuit of Fig. 1 with a single-ended output was fabricated in a 130nm CMOS nwell process. This technology has nominal NMOS and PMOS threshold voltages

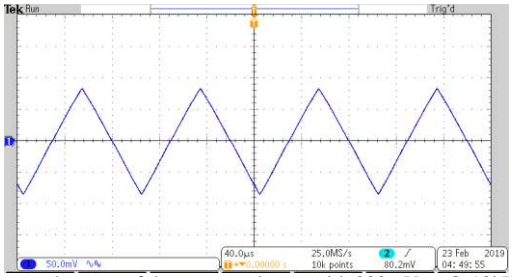

Fig. 7 Measured output of the transconductor with 200mVpp @ 10kHz single-ended triangular input.

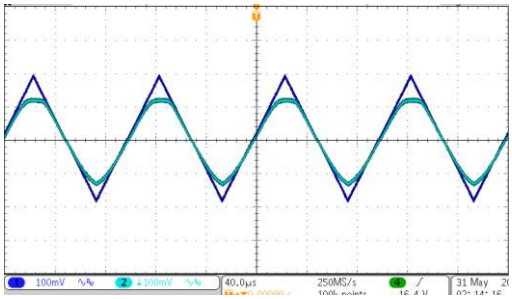

Fig. 8 Experimental output waveform of the transconductor with 400mVpp @ 10kHz triangular single-ended input signal.

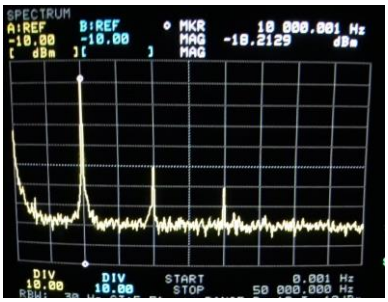

Fig. 9 Measured spectrum with a 0.1Vpp @10kHz sinusoidal single-ended input.

$V_{THN} \approx |V_{THP}| \approx 0.4V$ and nominal supply voltage $V_{supplyTech}=|V_{DD}-V_{SS}|=1.2V$. The circuit was designed to operate in subthreshold with a bias current I_{bias}=100nA with dual supply voltages ±0.2V and V_{DSsat}=0.07V. The bias current leads to gate-source voltages of NMOS transistors with aproximate values $V_{GSNMOS}\approx$0.16V and source-gate voltage of PMOS transistors with values $V_{SGPMOS}\approx$0.14V. Fig. 5 shows a micrograph of the fabricated circuit, while the test bench of the circuit is shown in Fig. 6.

Table I shows the transductor design values employed. The resistance used in the transconductor has a value R=1.3MΩ. The associated area occupied by R was 0.00134mm^2. The chip also has an integrated load resistor R_L=1.3MΩ that is connected between the output of the transconductor and ground. This implements a feedforward amplifier with a gain $A_V=g_{mOTA}R_L = R_L/R = 1V/V$. An on-chip buffer with input capacitance of approximately $C_L\approx$0.2pF was used at the output of the trasconductor. The transconductor works with dual supply voltages of ±0.2V and it was tested with a single-ended input signal V_{s1}, (V_{s2}=0).

$$FOM_{LOTA} = \frac{\left(\frac{V_{inMax}}{V_{Supply}}\right)BW}{P_{Diss}}\left[\frac{MHz}{mW}\right] \tag{15}$$

TABLE II PERFORMANCE COMPARISON WITH OTHER LOW-VOLTAGE TRANSCONDUCTORS

	2007 [17]	2013 [18]	2014 [19]	2019 [20]	This work
Tech. (µm)	0.5	0.18	0.13	0.18	0.13
Driven by	Gate	Gate	Bulk	Bulk	Gate
Supply (V)	±1.5	1.2	0.25	0.3	±0.2
G_M (µS)	10	12.5	0.022	0.255	0.76
Input range (V)	0 - 3	0 - 1.10	--	0-0.3	±0.1
OTA Bandwidth (MHz)	90	14.1	--	0.000334	1.1
Noise (nV / √Hz)	1780	258.4	100(µV*RMS*)	1330 @10Hz^{Sim}	988^{Sim}
THD (dB) @V_{PP} @ Freq (MHz)	-60 @ 6 @ 0.1	-44.2 @ 1 @ 0.1	-45.51 @ 0.1 @ --	-56.47@ 0.1 @ --	-41.61@ 0.2 @ 0.01
PSRR (dB)	35/43	47.8	--	39.9	52^{Sim}
CMRR(dB)	62	--	--	57	70^{Sim}
Power (µW)	3000	85	0.01	0.05	0.36
FoM (MHz/mW)	30	152	--	6.68	1525
Area (mm^2)	0.1	0.0144	0.053(active)	0.035	0.0264

The measured ouput voltage of the circuit operating with ±0.2V is depicted in Fig. 7; the input signal is a 10kHz 200mVpp triangular signal. As it can be seen it has a linear output. The ouput with a rail-rail input signal is shown in Fig. 8. This is limited by the value of voltage V_{DDP}. When V_S has a value equal to V_{DDP} the current I_R is equal to zero (1).

The measured amplitude spectrum of the output upon application of a 10kHz 100mVpp sinusoidal single-ended input signal is shown in

Fig. 9. Under this conditions the transconductor with the resistive load exhibits a SFDR= 42dB, SNR=72dB and THD = 0.83%.

The amplifier's experimental bandwidth was 500kHz. This bandwidth results from the internal pole of the transconductor (approximately 1.1MHz) and the output pole of the transconductor generated by the parallel combination of C_L and R_L (approximately 1 MHz). Table II shows a performance comparison with other published linear transconductor works. No comparison has been done to OTAs used as op-amps in close loop since they are not linear and have a very small differential input range. The FoM used for comparison was proposed by [18] and expressed in (15), where V_{inMax} is the maximum input signal (for 1% THD) and $V_{Supply}=V_{DD}-V_{SS}$.

PVT corners simulations have been performed to characterize the operation of the design under different environmental conditions. It was found that the design is robust to PVT variations: temperature variations 0-85 °C, on the power supply voltage variations V_{DD}±10% and the process corners: tt, ss, ff, sf and fs. The design is robust to process and temperature variations since the circuit's transient and AC responses show negligible changes. Variations in the power supply result in an ouput DC offset with maximum value of 10mV.

VI. CONCLUSION

A method to implement gate-driven ultra-low voltage linear transconductors that are capable to operate with ±0.2V supply voltage and wide input linear range was introduced. The design uses 900nA total biasing current. Despite the low biasing current and supply voltages, it achieves a relatively high transconductor bandwidth of 1MHz. The scheme was experimentally validated with a test chip prototype in 130nm CMOS technology.

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