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3D active edge silicon sensors: Device processing, yield and QA for the ATLAS-IBL production

Cinzia Da Vià [a,*], Maurizio Boscardil [b], GianFranco Dalla Betta [c], Giovanni Darbo [d], Celeste Fleta [e], Claudia Gemme [d], Gabriele Giacomini [b], Philippe Grenier [f], Sebastian Grinstein [g], Thor-Erik Hansen [h], Jasmine Hasi [f], Christopher Kenney [f], Angela Kok [h], Alessandro La Rosa [i,1], Andrea Micelli [j], Sherwood Parker [k], Giulio Pellegrini [e], David-Leon Pohl [l], Marco Povoli [c], Elisa Vianello [b], Nicola Zorzi [b], S.J. Watts [a]

[a] School of Physics and Astronomy, The University of Manchester, Oxford Road, M13 9PL Manchester, UK
[b] Fondazione Bruno Kessler, FBK-CMM, Via Sommarive 18, I-38123 Trento, Italy
[c] DISI, Università degli Studi di Trento and INFN, Via Sommarive 14, I-38123 Trento, Italy
[d] INFN Sezione di Genova, Via Dodecaneso 33, I-14146 Genova, Italy
[e] Centro Nacional de Microelectronica, CNM-IMB (CSIC), Barcelona E-08193, Spain
[f] SLAC National Accelerator Laboratory, 2575 Sand Hill Rd, Menlo Park, CA 94025, USA
[g] Institut de Fisica d'Altes Energies (IFAE) and ICREA, Universitat Autonoma de Barcelona (UAB) E-08193, Bellaterra (Barcelona), Spain
[h] SINTEF MiNaLab, Blindern, N-0314 Oslo, Norway
[i] CERN CH 1211, Geneva 23, Switzerland
[j] Tne University of Udine and INFN, via del Cotonificio 108, 33100 Udine, Italy
[k] University of Hawaii, c/o Lawrence Berkeley Laboratory, Berkeley, CA 94720, USA
[l] Physikalisches Institut der Universität Bonn, Nußallee 12 D-53115, Bonn, Federal Republic of Germany

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ABSTRACT

3D silicon sensors, where plasma micromachining is used to etch deep narrow apertures in the silicon substrate to form electrodes of PIN junctions, were successfully manufactured in facilities in Europe and USA. In 2011 the technology underwent a qualification process to establish its maturity for a medium scale production for the construction of a pixel layer for vertex detection, the Insertable B-Layer (IBL) at the CERN-LHC ATLAS experiment. The IBL collaboration, following that recommendation from the review panel, decided to complete the production of planar and 3D sensors and endorsed the proposal to build enough modules for a mixed IBL sensor scenario where 25% of 3D modules populate the forward and backward part of each stave. The production of planar sensors will also allow coverage of 100% of the IBL, in case that option was required. This paper will describe the processing strategy which allowed successful 3D sensor production, some of the Quality Assurance (QA) tests performed during the pre-production phase and the production yield to date.

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1. Introduction

The pixel Insertable B-Layer (IBL) [1] will be the first detector upgrade in the ATLAS experiment at the LHC in 2014 (phase zero, PH0). Sensors and front-end electronics for the IBL will use state of the art design in term of radiation tolerance and performance making this project a crucial test bench for technology choices in the future high luminosity LHC experiment upgrades. At the moment two more phases are foreseen for such upgrades in the ATLAS experiment after the one which will allow the IBL installation: phase one (PH1) in 2017, where the level1 trigger system should be changed and a novel tracking system installed symmetrically 200 m from the interaction point to study diffractive events at low angles (AFP, Atlas Forward Physics), and a phase two (PH2) in 2022 where the entire tracking system should be substituted. The AFP experiment [2] will use 3D sensors technology for its tracking system. After the difficult decision to move forward the construction of the IBL detector to be ready in time for installation during PH0 and a yearlong qualification campaign in 2011, two sensor designs passed the requirements imposed by the stringent IBL environment: a more conservative planar silicon design with 200 μm slim edges, which will form 75% of its volume, and the novel 3D silicon sensors, double sided

* Corresponding author.
E-mail address: cinzia.da.via@cern.ch (C. Da Vià).
[1] Now at the University of Geneva, Switzerland.

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with full and partially through columns, also with 200 μm slim edges for the remaining 25%. IBL consists of a single pixel layer at 3.2 cm from the LHC beam and will be exposed to an integrated fluence of 5×10^{15} 1 MeV equivalent neutron per square centimetre during its lifetime. Its presence will allow a more precise primary vertex reconstruction and tracking of the outgoing particles after the primary LHC proton beams collision.

3D silicon sensors, where electrodes penetrate fully (full-3D) or partially the silicon substrate can be manufactured using the same micromachining technology used in MEMS (Micro-Electro-Mechanical Systems) to etch deep narrow columns or trenches within the silicon wafer which are consequently filled with dopants to form electrodes of a pin diode. Two main processing techniques have been successfully implemented to date: front side etching full3D with active edges which was the original design proposed at the Stanford Nano-Fabrication facility (SNF)[3,4] and is now fabricated at SINTEF [5]. For full-3D, a support wafer is used to minimise mechanical stress during wafer handling but would require removal at the end of the process. The second is a double side processing where opposite polarity, full or partially through column etching is performed from both wafer sides, and is currently fabricated at CNM [6] and FBK [7]. Fig. 1 schematically illustrates these three different 3D processing approaches.

2. Processing and Quality Assurance tests

The 3D ATLAS R&D Collaboration [8] was formed in 2007 to develop, test and industrialize 3D silicon sensors in various processing facilities in Europe and USA. Composed by ~90 members from 18 research institutions and 4 processing laboratories, it developed since its formation a collaborative rather than competitive strategy to accelerate the transition between the research and development stage and industrialization. For this purpose a common floorplan wafer design was agreed and distributed to all collaborating semiconductor facilities so full mechanical and electrical compatibility could be attained and cost could be reduced during hybridisation with the pixel front end electronics chip. The collaboration originally explored all three processing approaches described in the previous section for the IBL, but finally agreed in using the two simpler double side ones, without the support wafer removal steps and back-side metallisation which allow traditional wire-bonding bias, with slim rather than active edges. This decision was taken to minimise the production risk and enhance system compatibility with planar sensors. After the completion of the first common-floorplan runs, test assemblies were distributed and tested amongst groups in research institutions, so results could be gathered and discussed in parallel, reducing systematic errors. The outcomes could then be fed back to electronics designers to improve the sensor processing parameters. All the four processing facilities involved in the ATLAS 3D Sensor Collaboration started the fabrication of the first batch of 3D sensors with a common wafer layout in spring 2010[8]. This run was intended as a qualification batch for IBL. As starting material, all facilities used silicon substrates coming from the same ingot from TOPSIL. These wafers were Float Zone, double-side polished, p-type, with 100 mm diameter, <1 0 0> crystal orientation, 230 μm thickness, and a very high resistivity in the range from 10 to 30 kΩ cm. The processing times were different for different facilities: in this respect, double-sided 3D sensors provide some advantage since they require a lower number of process steps, so that FBK and CNM batches were completed earlier than the SINTEF and SNF ones. Fig. 2 shows signal efficiencies, defined as the signal ratio after and before irradiation of FE-I4 structures and other structures including strips and diodes, where all electrodes of the same type were connected together. On Fig. 2 bottom most probable values measured on such sensors after bump-bonding and after irradiation to the IBL expected fluence of 5×10^{15} ncm^{-2}($n=1$ MeV equivalent neutron) [9] confirmed the most-probable trend measured on similar structures before and after irradiation. To be noticed the points at $\sim9\times10^{15}$ ncm^{-2} [10] and at 2×10^{16} ncm^{-2} [11] which closely match the requirements for the innermost pixel layers for the High Luminosity LHC phase. This confirms that 3D sensors manufactured in different facilities have similar characteristics after irradiation and productions can indeed be performed at different facilities.

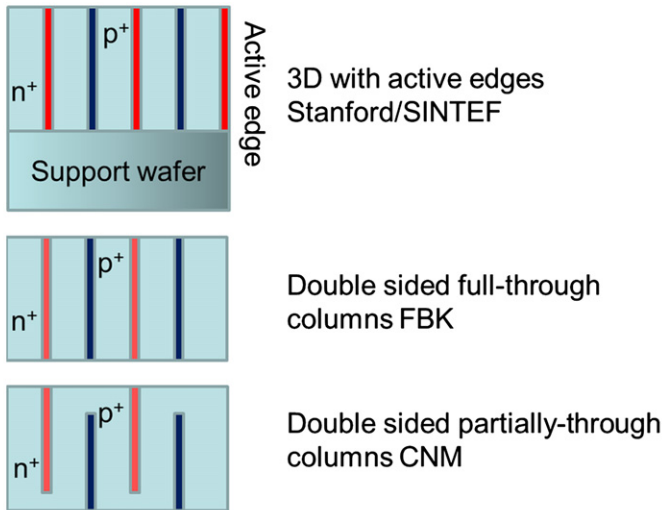

Fig. 1. Sketch of the three 3D sensor options presently studied within the 3D ATLAS R&D Collaboration. Top, full through with active edges. This requires a support wafer to guarantee mechanical stability which is afterwards removed. Middle. Double-side processing full-through with slim edges proposed by FBK. Bottom. Double side processing with partially-through columns proposed by CNM.

After fabrication, QA tests were performed in FBK and CNM to select the good sensors for bump-bonding performing either column by column

Right. Most probable values for a 230 μm 3D sensor extracted for Fig. 2 left and from previous measurements.

current–voltage measurements using aluminium temporary metal strips to link together all 336 pixels in one column (FBK) or current–voltage measurements performed on a dedicated guard ring around the entire sensor's active volume (CNM) with the following specifications:

Parameter	Value
Operation temperature [T_{op}]	20–24 °C
Depletion voltage [V_{depl}]	<15 V
Operation voltage [V_{op}]	≥ $V_{depl}+10$ V
Leakage current at operation voltage [I(V_{op})]	<2 μA (full sensor) <200 nA (guard ring)
Breakdown voltage [V_{bd}]	>25 V
Leakage current "slope" [I (V_{op})/ I (V_{op}–5 V)]	<2

As can be seen from the leakage current specification, a different current limit is selected depending on the measurement method since the guard ring current measurement can only check the quality of the external region of the sensor. However, it was possible to prove that defects are more likely to be localised

nearby the border region, making this test a good representation of the quality of the sensor.

Tests performed after bump-bonding further validated the proposed selection criteria method as can be seen for example in Fig. 3.

For comparison, Fig. 4 shows the current versus bias voltage measured on and FBK sensor using the temporary metal method compared with the one measured on the module connected to the readout electronics after hybridisation. The good reproducibility of the two curves in Figs. 3 and 4 indicate that the wafer selection method using either the guard ring or temporary metal are well suited for 3D sensors quality assurance tests. More details on specifications and QA can be found in [12].

The same assembly reported in Fig. 4 was exposed to a ^{90}Sr radioactive source to check the pixels occupancy and therefore verify the presence of dead or noisy pixels. An image of the collimated source is shown in Fig. 5.

3. D sensors production yield

The 3D sensors IBL production yield for an outcome of 224 good sensors with FE-I4 layout is currently ~60% for ~50 wafers. This is only for so called class 'A' sensors defined as perfect sensors following the selected criteria specification described previously. Class 'B' sensors are still working and will be used for general purpose and irradiation tests. A summary of the 3D IBL production is listed in Table 1.

4. Conclusions

3D sensors compatible with the FE-I4 front end electronics chip designed for the ATLAS IBL project were successfully

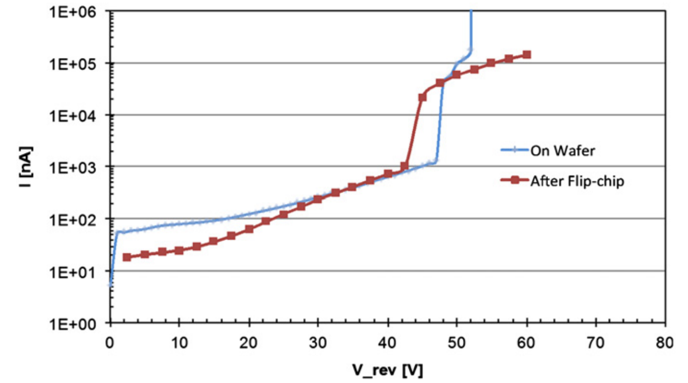

Fig. 4. Current versus bias voltage from and FBK sensor measured on wafer using a temporary metal before bump-bonding and after bump-bonding with the FE-I4 readout electronics chip.

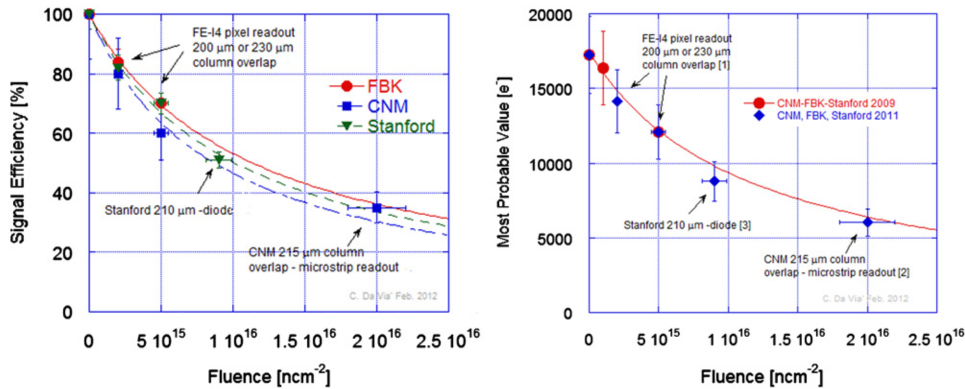

Fig. 2. Left. Signal efficiency (SE) defined as the ratio between the irradiated and non-irradiated signal amplitudes of 3D sensors manufactured at FBK, CNM [9] and Stanford[10] with column overlap ranging from 210 μm to 230 μm and connected either to the FE-I4 readout chip, the Alibava strip readout chip [11] or a one channel diode (where all readout electrodes are connected together) discrete amplification.

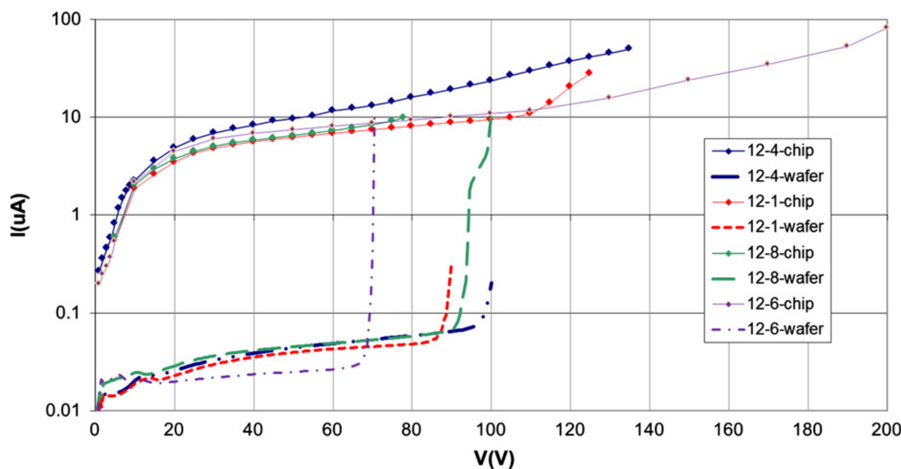

Fig. 3. Guard ring current–voltage characteristics of CNM 3D sensors measured on wafer before bump-bonding and after bump-bonding with the FE-I4 front end chip. The leakage current difference before and after bump-binding is due to the limited volume probed by during the guard-ring test.

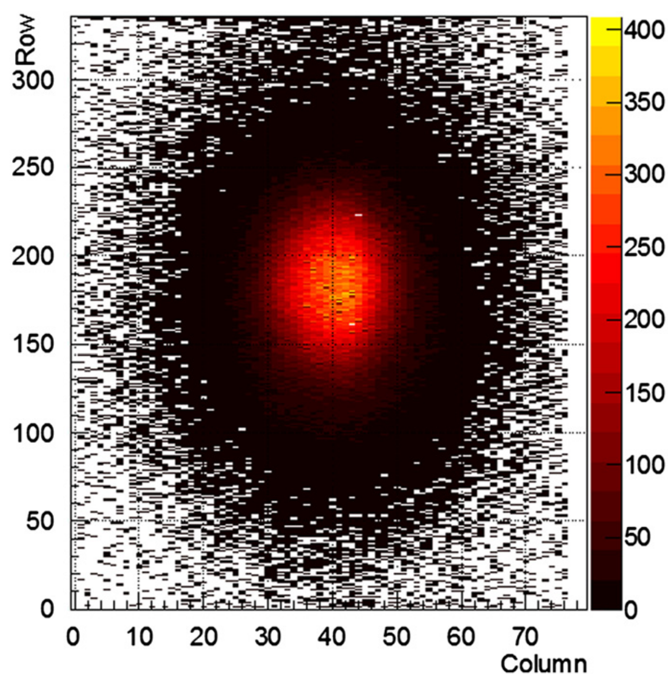

Fig. 5. Image from a ^{90}Sr radioactive source through a pinhole showing the occupancy of the same FBK device shown in Fig. 4. The z-axis on the left indicates the accumulated counts.

Table 1
Summary of the 3D sensors production for the ATLAS IBL.

Batch name	Status	Tested wafers	Selected wafers	*Yield on selected %*	*Number of good sensors*
A10 (FBK)	Completed	20	12	60	58
A11(FBK)	Completed	11	4	44	14
A12(FBK)	March				
A13(FBK)	2012				
CNM1	May 2012	19	18	60	86
CNM2	Completed	17	15	71	85
CNM3	Completed				
CNM4	March2012				
TOTAL	April2012	67	49	62	243
BB[a]			**43**	**65**	**225**

[a] BB = bump-bonded

fabricated in 2011. QA criteria allowed setting selection parameters for good sensors at wafer level prior to bump-bonding. Tests after bump-bonding confirmed the quality of the proposed selection method. Production yield on ~50 wafers is ~60%. 3D sensors completed the fabrication of 224 good sensors for 25% (1 1 2) IBL production with a redundancy of 100% in February, 2012. The IBL will be inserted around the ATLAS beam-pipe at 3.2 cm distance from the beam in Summer 2013.

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