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3D hybrid integration and functional interconnection of a power transistor and its gate driver

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***Abstract* -- 3D packaging and hybrid heterogeneous integration are currently attracting considerable interest in the literature. In most publications, the power dies and their respective gate drivers are interconnected using flex or PCB layers. Apart from a few exceptions, packaging is mainly based on separate power and driver dies, focusing on improving the performance of individual chips. This paper presents a different approach in which the design of the power and gate driver chips takes the interconnection of the two dies into account. This method is used in order to simplify and optimize packaging and interconnections and to improve the overall performance. The basic idea is to flip chip the integrated gate driver directly onto the power die, resulting in the 3D heterogeneous assembly of a vertical power device and a CMOS integrated gate driver. In order to simplify the implementation of this solution, the gate driver supply, its storage capacitor and the control signal insulation unit are also integrated and interconnected in and on the two silicon dies.**

***Index Terms*-- power conversion, semiconductor device packaging, hybrid integrated circuit interconnections**

I. Introduction

Power electronics is pushing towards higher performances and higher power densities thanks to semiconductor integration and innovative packaging, assembly and interconnect solutions. The monolithic and functional integration of the power device, with its gate driver, supply, protections and isolation has been investigated in [1-5] and is particularly suitable in Smart Power and home appliance applications. For higher power and voltage levels, hybrid integration is preferred for its higher flexibility and greater performances are obtained with the association of heterogeneous silicon dies, each of them being optimized for its expected tasks. In this way, the hybrid integration of intelligent power modules have raised the power density levels thanks to new assembly and packaging techniques [7, 8]. Nevertheless, IPEMs, which stand for Integrated Power Electronics Modules, are still based on soldered interconnects in which control/driver and power dies are interconnected to each other through flex or PCB layers [3] [4]. Even in a 3D assembly, these interconnect interfaces generate reliability and EMI coupling problems [6] which may limit the operational bandwidth and mutual functionalities. In most cases, the power device and its driver circuit are assembled in separate packages which introduce parasitic interconnect impedances between the two elements. In some cases, the two devices are assembled in the same package allowing the improvement of their interconnection, even if only planar assembly is usually considered. In this case, the impact of parasitic interconnect impedances is reduced and functionalities can be extended. For example, the driver/control die can integrate a thermal sensor which can offer a valuable image of the power die temperature. Nevertheless, tight functional interaction between control and power dies remain limited and far behind what can be done in functional monolithic integration of Smart Power.

The aim of this paper is to present a customized and highly coupled design of a 600V vertical MOSFET power device and its integrated CMOS gate driver in order to optimize their global packaging but also their functional interactions and positive couplings. At the same time, the selected 3D approach will allow us to minimize the negative impact of parasitic interconnect impedances, which are critical in power device implementations. The objective is then to design the layout and the functions of the two dies in order to allow their assembly based on a flip chip interconnection. The power die acts as the receiver or substrate of the gate driver chip and both silicon dies share several electrical interconnections in order to implement a fully autonomous power device. The global function includes the power device itself, the driver supply, the isolated gate signal transfer unit, the driver amplification stage and the protections. Figure 1 presents the resulting System In Package (SIP) where the power die surface layout is designed to receive, in flip chip, the gate driver chip but also the storage capacitor of the gate driver supply and an additional couple of terminals for the control signal to be transmitted from the remote control to the gate driver. The power and driver dies are not only electrically connected, but also from the mechanical and thermal point of views, making very attractive the global system.

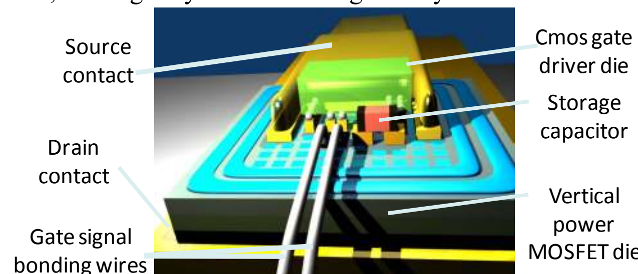

Fig. 1. Possible representation of the 3D hybrid integration of a power device and its electronic environment.

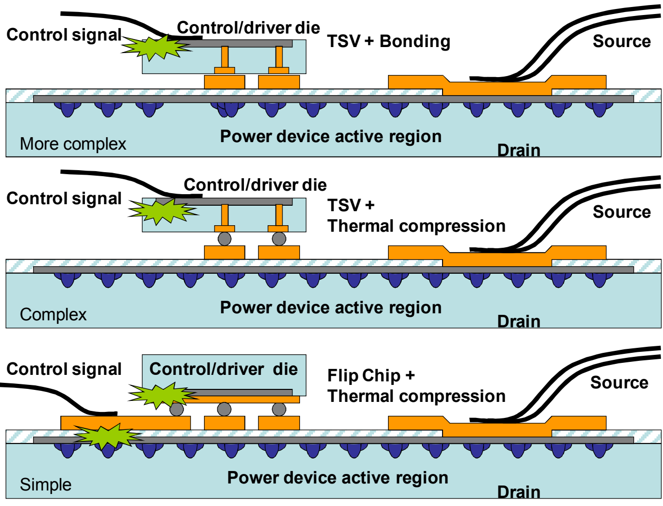

Fig. 2. Interconnection possibilities between the power device and its command using different technological solutions

Figure 2 shows different technological solutions to interconnect the power device with its command. The external connections, i.e. the control signal and the source contact, are carried out with bonding wires soldered on pads at the surface of the power device. The best solution for realizing the interconnection between the power device and the command chip is to create Through Silicon Vias (TSV) in the command die, as it makes the flip-chip of this die non necessary, and could allow optical or electrical receivers of the command signal to be placed directly at the surface of the die. However, this solution is more complex and costly compared to a simple flip-chip using bumps on the external pads of the command chip. As it is simpler and cost-saving, this solution will be first investigated to evaluate the performance of such a 3D power module. If the performance is as good as expected, the TSV solution will be next investigated. The functional description of the power device and control die association clearly shows that both devices are closely interconnected and that their designs are interdependent. The following parts of the papers deals with design, technological and physical issues related to this particular approach.

II. COUPLED DESIGN

A. Presentation

Making the assumption that the driver and power parts can be associated one on top of the other with tight electrical connections, the designer can take advantage of both dies in order to develop the functionalities and performances of the global power switch. Especially, it becomes possible to mix functions from both dies as it is done today in microelectronics in multichip modules and chip on chip assemblies [9].

B. Functional hybrid integration

In order to simplify and to complete the implementation of this hybrid autonomous power device, drivers, supply, protection and isolated control signal units must be included. For this, a specific work has been carried out in order to identify technical solutions which would allow to synthesize a complete system within two semi-conducting dies. It is out of the scope of this paper to present the choice and the design of each function and this is described in more details in [10]. This paper focuses on the interconnection technology and implementation. Nevertheless, figure 3 presents the schematic of the power device and its associated gate driver in order to give an idea of the functional couplings that can be imagined among the control and power dies. In this schematic one can identify the presence of the driver stage [11], the control signal isolation unit based on a coreless transformer integrated in the CMOS die [12] and the introduction of self power supply techniques [13]. The filtering capacitor is also soldered at the surface of the power device. As a result, the power die is designed to receive the control die with numerous electrical interconnections. The only connections with the electrical environment of the autonomous power switch are the drain on the backside of the die, the source at the surface and the pads to connect the external control signal (Figures 1 and 3). These control signal pads are connected to the primary side of a magnetic coreless transformer integrated on the CMOS device through flip chip interconnections. The pads do not have to be referenced at the power switch source potential since the transformer and the pads are isolated thanks to oxide layers : 1.6µm on the power device and 2.6µm between the primary and secondary windings of the coreless transformer. These isolation layers offer up to 1.2kV dielectric isolation which could be satisfactory for many applications. The secondary side of the transformer is connected to a demodulation unit in order to enable the operation of the transformer in the range of 100MHz. The layouts of both devices are presented on figures 4 and 5. On figure 5, one can see the specific surface layout of the power die, with a large surrounding interconnect region for the source pad. At the center of this power die, numerous pads are placed for the flip chip of the CMOS gate driver. Next to it, a couple of pads are clearly visible, which are required for the soldering of the gate driver supply storage capacitor.

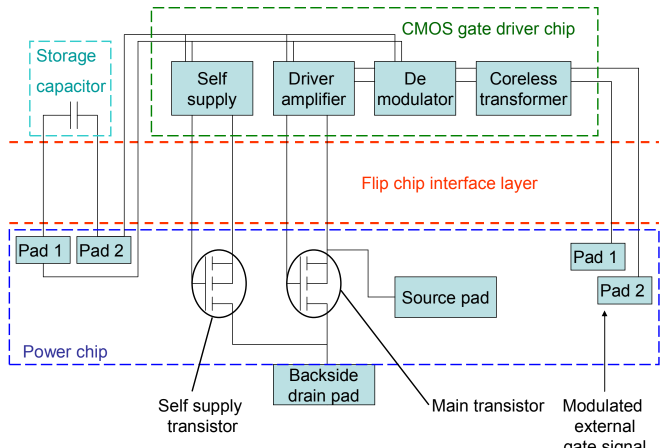

Fig. 3. Schematic diagram presenting the functionalities shared and integrated in both silicon dies and their necessary electrical interconnections.

C. Design and layout

This section of the paper focuses on the layout of the silicon

dies. Their electrical and functional interactions have been developed on the basis of a chip on chip assembly. This requires designing both dies in order to flip chip one on top of the other. Figure 4 and 5 present the layout of both devices. The control dies integrates several functions and numerous pads which will all find a receiving pad on the power die. Most of them are interconnects among the two silicon dies.

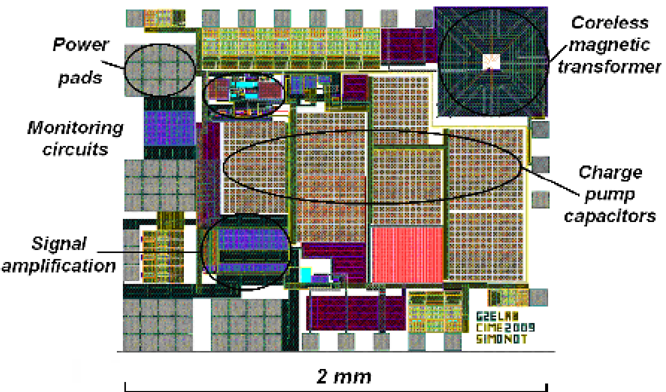

Fig. 4. Layout of the driver/control die with its main functional regions and their necessary electrical interconnections.

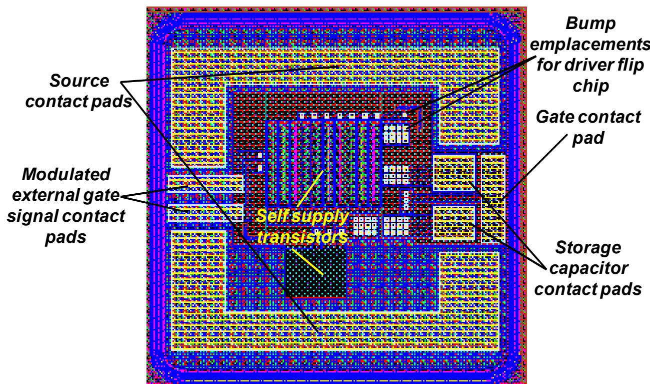

Fig. 5. Layout of the power die with its pads.

As far as the power die is concerned, all receiver pads for the control/driver die can be clearly seen at the center of the die. We can also see the pads necessary to solder the storage capacitor (on the right), the pads necessary to transfer the external gate control signal to be applied to the primary side of the isolated coreless transformer, and the source pads surrounding the control/driver dies. Depending on functionalities shared by the two elements, specific elements can be integrated underneath the central region where the control die is flip chipped. This is the case in figure 5 where two vertical power devices are integrated next to the main switch as parts of the self supply technique implemented in this system. However, this is not a requirement.

The important issue that needs to be related here is that the surface of the power device must be adapted to receive the control/driver die without losing power device active surface and without considerable reduction of source electrical contact. This is carried out with an extension of the power device technological process in order to develop a second metal layer at the surface of the die. This second metal layer will be a "thick" copper layer facilitating the flip chip interconnections but also improving the electron collect at the surface of the power source terminal. As a result, it becomes possible to develop a 3D assembly which is effective from an electrical point of view and which introduces a limited extra cost in the surface of silicon. Of course, this enlarges the technological process but this is done at the wafer level and using collective processes which improve the global reliability while optimizing the production costs. In order to implement such a package, it is necessary to develop specific technological steps. The following section of the paper focuses on the work that is currently undergoing on this issue.

III. 3D HETEROGENEOUS ASSEMBLY

A. *Basic principles*

3D heterogeneous assembly is favorable for the optimization of each function(s) with respect to technological possibilities while optimizing the interconnections among the dies. This approach is currently attracting considerable interest in microelectronics toward the “more than Moore” law where the 3D heterogeneous assembly gives an opportunity to further increase the density of the integrated circuits using the third dimension in SIP configurations. After wire bond and flip chip interconnects, TSV (through silicon via) are under investigation for optimized signal transfer bandwidth. Below is given a set of possible solutions in order to interconnect the power die and its corresponding control/driver chip.

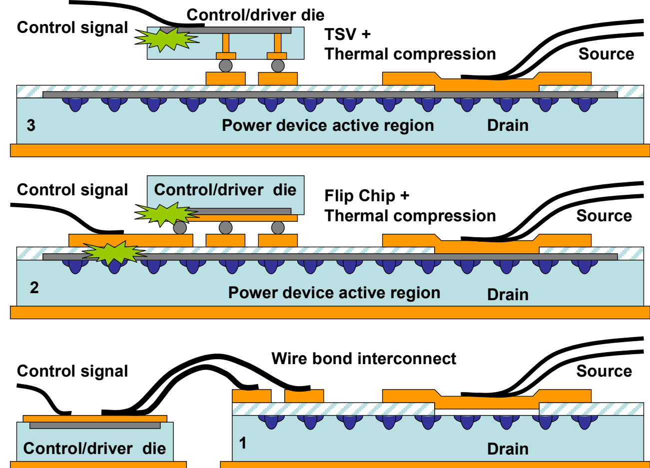

Fig. 6. 1-Planar and wire bond heterogeneous assembly into a same package, simple to implement but with large parasitic impedance. 2-3D heterogeneous assembly with bump interconnections, more favorable but with dielectric constraints of the power die. 3-3D assembly including TSV for dielectric constraint reductions but much more expensive.

In this paper, we will focus on the 3D interconnection based on the flip chip of the control/driver chip on top of the power die. This is the most realistic approach since only two dies are to be interconnected and since it remains reasonable from technological and cost point of views.

B. *Flip chip assembly*

CMOS technology is developed to enable flip chip assembly. Bumps are deposited on the surface of the external pads by collective processes or with the help of a stud bump machine. In our case, since the realization of the control/driver

chips is shared with numerous other designs, the bumps must be deposited after the dicing of each chip. Figure 7 presents a picture of the chip with bumps and a zoom of a high current array of pads.

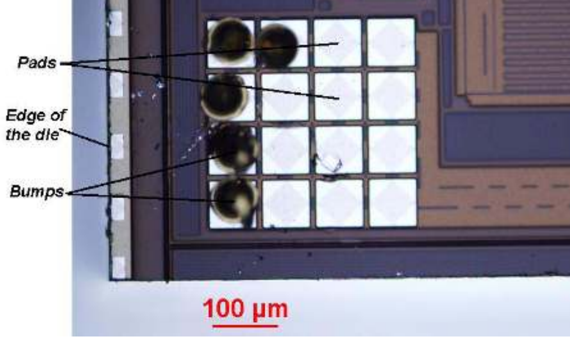

Fig. 7. Deposited bumps on the power pads at the surface of the CMOS gate driver.

Mainly three kinds of bumps are available, aluminum, copper and gold. Gold bumps can be soldered on most conductive materials and are widely available. Nevertheless, numerous gold bumps require the use of thermal compression soldering technique with heavy forces in the range of 100N for 100 pads. As it has been presented, the surface of the power die has been designed accordingly to receive the control/driver CMOS die by flip-chip and it must be prepared for the soldering process. The technological steps needed for this preparation are presented in the following section.

C. *Power device back-end technological issues*

In order to optimize the flip chip of the control/driver chip at the surface of the power die, a special metal layer is added in order to collect in the best manner the current flowing from the source terminal of the power device and to properly interconnect the two dies. For this, a 10µm copper layer is inserted after deposition and etching of a 1.6µm-thick Si_3N_4 layer for the dielectric isolation between the source and the non isolated control signal pads at the surface of the power device. Figure 8 below presents the etch of this specific layer.

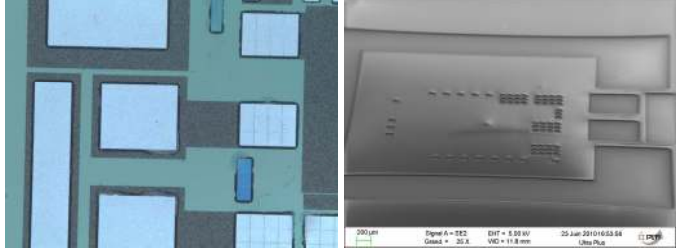

Fig 8. Pictures of the power die back end technological developments. Left : etch of 1.6µm Si_3N_4 dielectric layer, above the aluminum contacts – capacitor contacts, and pads arrays are visible on the picture. Right, deposition and developing of thick photoresist for the copper tracks growth.

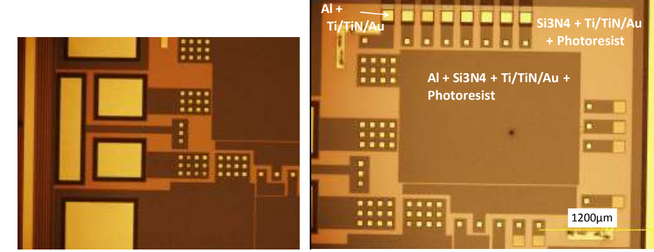

Fig 9. Pictures of the power die back end technological developments before electroplating: deposition of thin layers Ti/TiN/Au and thick photoresist. Left, view of the capacitor contacts. Right, footprint for the flip chipped CMOS chip.

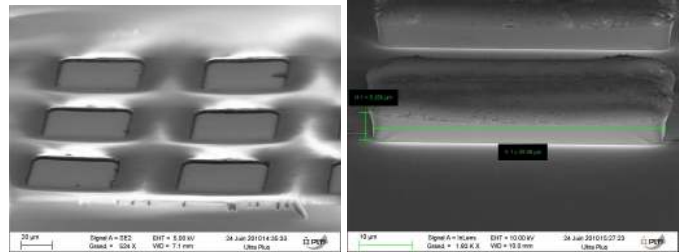

Fig 10. Copper tracks growth into thick photoresist and height after photoresist removal.

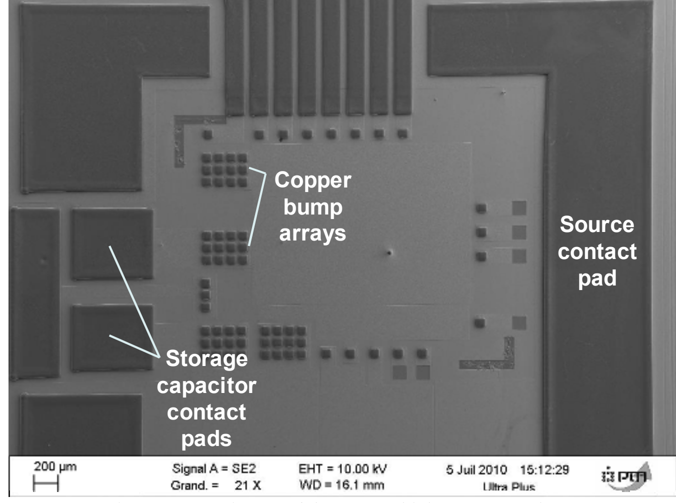

Fig 11. SEM picture of the 10µm thick copper tracks

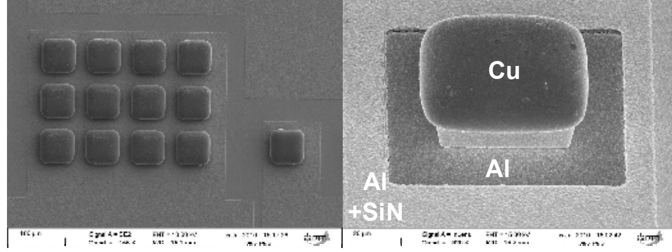

Fig 12. SEM pictures, zoom on the copper pads

This thick copper layer is made by electroplating at wafer level in a photoresist mold. Figures 8, 9, 10 and 11 show the successive steps of the deposition of this layer. At first, a thick photoresist is deposited on the Ti/TiN/Au seed layers and developed. A thin sputtered Cu seed layer can also be deposited instead of the Au layer. Then, the electroplating of copper is made on the wafer, and the copper growth is made only into the photoresist mold as shown in figure 10. Then,

figures 11 and 12 show the copper contacts and pillars which appear after the photoresist removal. The last step of the assembly is the flip chip of the command die on this copper metallization, which is currently under process. Before this assembly, electromagnetic and thermal issues that could happen in such a structure have been studied and simulated. This is detailed in the next section of this article.

IV. ELECTROMAGNETIC AND PHYSICAL ISSUES

A. *Electromagnetic issues*

Hybrid chip on chip assembly relaxes electrostatic couplings compared to monolithic integration. On the other hand, it offers the best possible parasitic interconnect impedance reduction with inductive and resistive impedance in the range of nH and mΩ. This approach makes possible high frequency functional interactions between the driver and the power device and gives the opportunity to drive the power device near its limits. Especially, electromagnetic couplings are reduced, allowing either to reduce the specifications on the driver or to operate the switch with a unipolar gate driving signal.

For example, the reduction of magnetic parasitic noise allows us to split and to optimize the gate driver self supply technique among the two dies without altering the performances of the system. This is essential because the self supply technique under loss free operation [13] operates at power device switching transition and under very high dynamic conditions, making important the reduction of parasitic interconnect impedance. The simulated operation of the function taking into account the reduced parasitic elements between the two dies is given figure 13. The split of the function allows the control of the technique which enhances and optimizes its operation. Nevertheless, this requires minimizing the effect of interconnections, as it can be observed on figure 14 where enlarged parasitic elements between the two dies lead to ineffective behavior and performances.

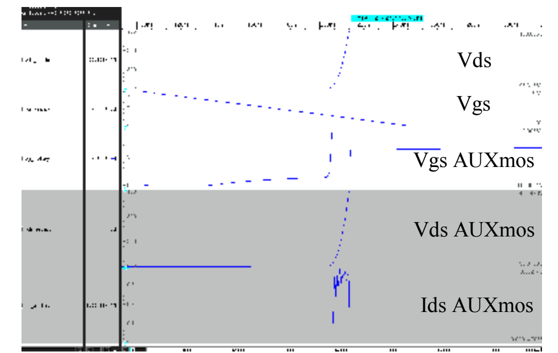

Fig 13. Good operation of the self supply circuit with reduced parasitic elements between the two dies

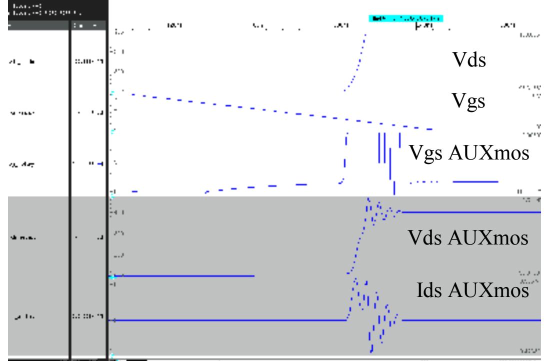

Fig 14. Bad operation of the self supply circuit due to enlarged parasitic elements between the two dies

B. *Thermal issues*

As far as thermal issues are concerned, it is important to notice that the heat generated by the control/driver die will be evacuated through the power device. A simple 1D electro-thermal model can be developed to investigate the temperature distribution on the power and control/driver chips. The structural model of the package is depicted figure 15 below.

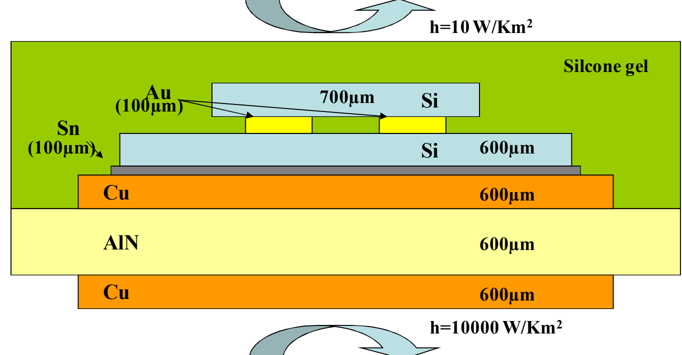

Fig 15. Structural model and dimensions of the package

The most important thermal parameters of the different materials in the package used for the thermal 1D simulation are listed in the table I below. The power to be dissipated is estimated to 70mW for the driver and 10,1W for the power transistor, assuming that commutation losses are equal to conduction losses and for a load current of 5A, a voltage drop across the transistor of 2V during ON state and a duty cycle of 50%. The thermal resistance of the radiator is assumed to be 2 K.W-1.m-1

TABLE I
VALUES OF THE THERMAL PARAMETERS OF THE PACKAGE MATERIALS

	Driver	Bumps	Transistor	Sn	Cu	Al N
Rth [K/W.m]	0.78	0.79	0.09	0.03	7e-3	0.02
Cth [J/K]	7e-3	3e-3	0.03	7e-3	0.1	0.2

Computing the temperature of the power and control/driver die demonstrates that their temperature difference is very small, only 0.1°C for a temperature of the driver chip of 47.1°C. This means that the control/driver die losses are small and that the thermal coupling between the two dies is good enough to cool the top chip trough the power die. This is an interesting point because it allows optimizing the use of the

planar surface for the spread of the heat coming from the power device which is positive. Another computation based on a thermal finite elements analysis with Flotherm from Flomerics shows more realistic but comparable results. The figure 16 below presents the simulation result where it can be seen that the temperature difference between the driver and power chips is in the order of 1°C (the temperature of the driver chip is 52.3°C whereas the hottest point in the power chip is 51.5°C). However, the temperature distribution in the whole structure seems to be good.

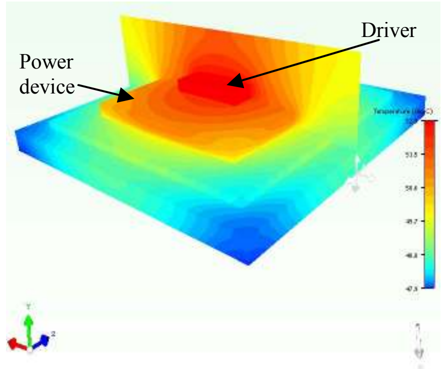

Fig 16. Thermal finite elements analysis of the package structure

C. *Thermo-mechanical issues*

Since the power and the control/driver dies are in silicon, they have identical thermal expansion coefficients. This is a good point for the reliability of the assembly because if their temperatures remain all the time close to each other, this means that reduced forces will be applied to the solder joints. We have seen that in steady state operation, the temperature differences are below one degree which is very good. A first order simulation based on the 1D equivalent model presented above has been carried out in order to investigate this issue under dynamic conditions. The time domain temperature evolution of the two dies is given figure 17 below.

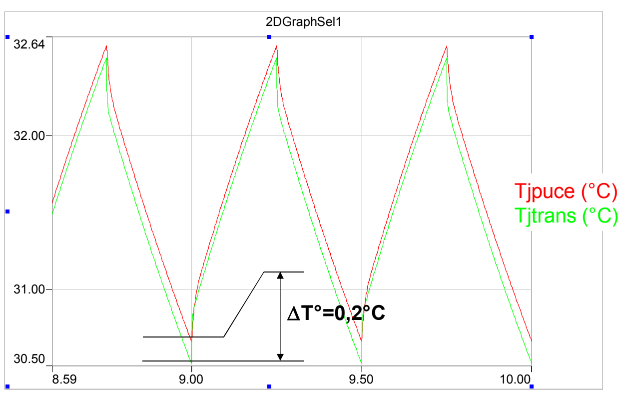

Fig 17. 1D dynamic thermal simulation of the package

It appears that under dynamic conditions, the temperature differences are slightly larger but remain below 1°C. This analysis gives us the opportunity to affirm that the assembly of the control/driver chip on top of the power chip should offer very nice robustness with respect to thermo-mechanical stresses.

V. Conclusion

The paper presents an innovative packaging approach allowing to interconnect in an effective manner the power device and its surrounding electronic environment. Besides the 3D interconnect approach, the paper presents a way to develop positive interactions between the power part and the close control parts. The proximity induced by the 3D integration approach enables tight connections and interactions while decoupling the technological issues related to each part. In this way, it is possible to greatly benefit from proximity effects such as a reduction of the parasitic interconnect impedance and introduction of enhanced functionalities without entering into the possible drawbacks introduced by the monolithic and functional integration. The best of each approach is here considered and used in order to develop a new range of power modules. Perspectives are now to validate the expected advantages introduced by this approach from the electrical side. Then, an important effort will have to be done while focusing on the reliability of the package especially at the soldering level between the two dies.

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