3D MEMS In-Chip Solenoid Inductor With High Inductance Density for Power MEMS Device

Tiantong Xu, Jiamian Sun, Hanxiao Wu, Haiwang Li, Hanqing Li, and Zhi Tao

***Abstract*— In this letter, we report the design and measurement of a 3D solenoid inductor that is embedded in a Si substrate and can integrate an iron core. Various inductor designs were fabricated with good structural integrity and repeatability via a CMOS-compatible MEMS fabrication process. The average inductance and quality factor peak-to-peak variation of the inductors was below 10%, which indicates that the fabrication process is repeatable. Among the inductors without iron cores, the highest quality factor (37.6 at 21 MHz) was found in a 5-turn inductor, and the highest inductance and inductance density (respectively, 86.6 nH and 21.7 nH/mm^2) were found in a 20-turn inductor. Among the iron-core inductors, the 15-turn inductor had an inductance of 1063 nH and an inductance density of 354.3 nH/mm^2, nearly 18 times higher than the same design without an iron core, which is the highest inductance density for a MEMS microinductor to the best of our knowledge. This type of inductor is an important component in RF MEMS and electromagnetic power MEMS devices and can improve their performance and efficiency.**

***Index Terms*— Solenoid inductor, power MEMS, high inductance density, CMOS-compatible fabrication process.**

I. Introduction

THE inductor is the most basic component of electromagnetic devices and the fundamental building block of electronic devices. Micro inductors are now widely used in microsensors [1], microactuators [2], RF MEMS [3], [4], and power MEMS. Power MEMS devices, such as transformers [5], [6], energy harvesters [7], and electromagnetic motors [8], usually require inductors with high inductance for power density and a high quality factor for efficiency. As MEMS devices are becoming increasingly compact, they also require inductors with high current capacity but compact physical dimensions. These demands can be fulfilled by integrating all power electronic components into one chip [9], [10]; higher integration will lower cost, reduce the space needed, and increase power density. Therefore, the inductor fabrication process needs to be CMOS compatible for integration. The reported CMOS-compatible MEMS fabrication technologies can be classified into two categories: on-chip and in-chip inductors. To fabricate on-chip inductors, surface micromachining techniques, such as sacrificial layer [11], [12] and UV-LIGA (Ultra Violet Lithographie, Galvanoformung and Abformung) [13], [14], are mature and widely used. The in-chip inductors can utilize the unused substrate volume and eliminate the inductor height above the substrate surface, which makes them easier to integrate with CMOS devices. Through-silicon-via technology is the most feasible method of fabricating in-chip inductors [15]–[17]. As high-aspect-ratio etching and electroplating is critical for building in-chip inductors, developing fabrication technology for it is still a challenge. Our group has reported the fabricaion process and properties of a silicon embedded inductor which we have been recently working on [18].

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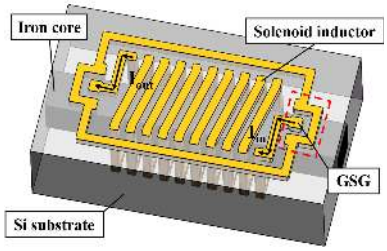

Fig. 1. Structure of the inductor. The input and output currents are indicated by the arrows. Ground-signal-ground (GSG) pads were designed for high-frequency measurements.

II. Design and Fabrication

In our design (Fig. 1.), the solenoid inductor is completely embedded in the silicon substrate through deep Si etching and Cu electroplating. The silicon-steel iron core is placed in the middle of the copper inductor. A SiO_2 layer is created by silicon thermal oxidation between the silicon substrate and the copper coil as the insulation layer.

The fabrication process comprises two stages (Fig. 2.). In the first stage, namely the silicon etching and bonding stage, space is created for the solenoid inductor and iron core; 0.5-mm-thick double-side-polished silicon wafers (resistivity 3.7 Ω·cm) are used as substrates. The process was as follows. 1) Use thermal oxidation to create SiO_2 layers on both sides. 2) Coat SPR700 photoresist on both sides, and expose the horizontal trench, through-hole, and iron core patterns using an EVG mask aligner. 3) Perform a buffered oxide etch to remove the exposed oxide layer. 4) Coat AZ4620 photoresist on the top

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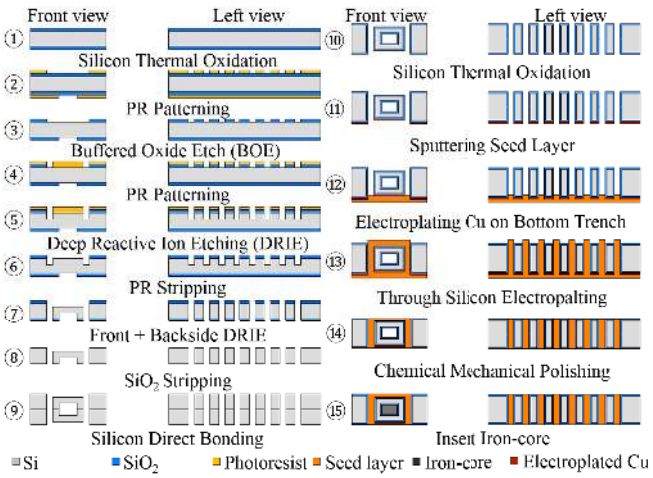

Fig. 2. Inductor fabrication process.

side, and expose the through-hole pattern. 6) Etch the through-holes with an inductively coupled plasma system (SPTS Co.). 7) Use piranha solution to remove the photoresist. 8) Use SiO_2 as the mask layer, etch through-hole and horizontal trench patterns on the top side, and etch iron core and through-hole patterns on the back. 9) Use diluted HF solution to remove all of the SiO_2 layer. 10) Use a bonder (EVG Co.) to conduct a silicon direct bonding process to create the iron-core space inside the substrate.

In the second stage, namely the copper filling stage, an electroplating process is used to create Cu coils. The process was as follows. 10) Use thermal oxidation to produce thick SiO_2 layer as an isolation between inductor and substrate. 11) Use a magnetron sputtering system (Denton Vacuum Co.) to sputter Cu (with Ni as middle layer) on the back as the seed layer. 12) Perform Cu electroplating until it fills the horizontal trenches and seals the through-holes at the back. 13) Cover the backside, preventing further Cu electroplating on this side. A "bottom-up" through-hole electroplating process was conducted to fill the through-holes and topside horizontal trenches. 14) Remove the Cu that had grown above the substrate surface by using a grinding machine (Logitech Co.). 15) Use a dicing machine (Disco Co.) to separate each inductor structure. Insert an iron core (China Baowu Steel Co.) in the center of the solenoid inductor.

III. Experimental Results

Eight different solenoid inductor designs were fabricated successfully with good structural integrity (Fig. 3 (a).). The inductors had four different turns (5/10/15/20) and two different widths (0.5/1 mm). The height of the inductors was 1 mm, the cross-section of the copper coils was a square with a side length of 100 μm, and the gaps between the coils were also 100 μm.

To examine the solid structure of the inductor solenoid more clearly, the silicon substrate of a 10-turn inductor was removed by etching in 25% tetramethyl ammonium hydroxide (TMAH) solution at 75 °C. The sample was then transferred to a Zeiss EVO 18 scanning electron microscope for further

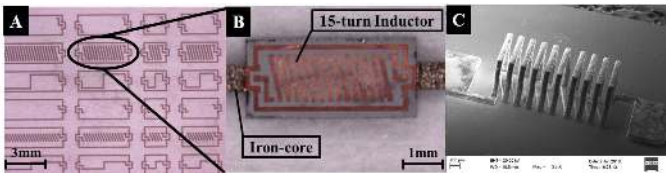

Fig. 3. (a) Top view of inductors before dicing and insertion of the iron core. (b) 15-turn inductor after dicing with iron core inside. (c) Entire exposed solenoid coil structure under SEM.

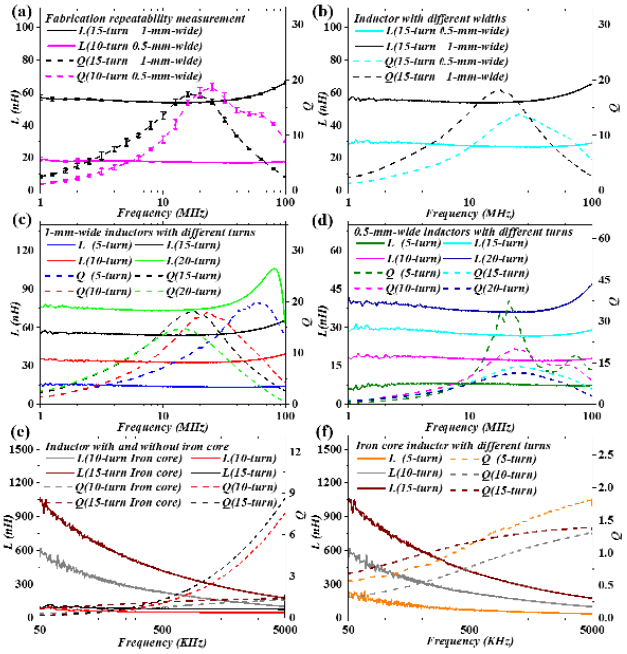

Fig. 4. Frequency-dependent inductance (L) and quality factor (Q) values for selected in-chip solenoid inductors. (a) Fabrication repeatability measurement: two inductor designs from three different process runs were tested. Mean and error bars are plotted. (b) Comparison of the inductor with different widths. (c) Comparison of 1-mm-wide inductors with different numbers of turns. (d) Comparison of 0.5-mm-wide inductors with different numbers of turns. (e) Comparison of inductors with and without iron cores. (f) Comparison of 1-mm-wide iron-core inductors with different numbers of turns.

observation (Fig. 3 (c).). The results show that the inductor structure morphology was fundamentally identical the design pattern and the structural integrity was good.

To test the performance of these inductors, an Agilent N5290A Vector Network Analyzer was used. The test probe was a Cascade ACP40-GSG-250 Air Coplanar Probe in conjunction with the Cascade Summit 12K Probe Station.

First, the performance of in-chip solenoid inductors without iron cores (Fig. 3 (a)) was measured. The testing frequency range was 1 MHz to 100 MHz; measurements were taken at regular intervals of 0.05 MHz (1981 total measurements).

Fig. 4 (a) shows the fabrication repeatability measurements for two inductor designs. For each design, we measured three inductors from different process runs. For all measurement points, the average peak-to-peak variation of the 15-turn 1-mm-wide inductor was 3.07% for inductance and 5.93% for quality factor, and the average peak-to-peak variation of the 10-turn 0.5-mm-wide inductor was 6.90% for inductance

TABLE I
ELECTROMAGNETIC PERFORMANCE OF VARIOUS INDUCTOR DESIGNS WITHOUT IRON CORE

Turns	*Width (mm)*	Q_{peak} *@frequency (MHz)*	*Q > 5 frequency (MHz)*	*L (nH) (Q > 5)*	$L_{density}$ *(nH/mm²)*
5	0.5	37.6 @ 21.0	6.5–100	7.33–8.17	14.7–16.3
10	0.5	20.1 @ 23.0	4.45–100	16.8–18.7	16.8–18.7
15	0.5	13.8 @ 25.2	5.7–100	26.5–29.0	17.7–19.3
20	0.5	11.4 @ 24.25	6.05–79.9	35.8–42.4	17.9–21.2
5	1	19.8 @ 59.85	5.7–100	13.4–14.6	13.4–14.6
10	1	18.0 @ 22.6	4.15–90.4	32.6–38.3	16.3–19.2
15	1	18.2 @ 17.5	2.35–68.75	53.9–60.0	18.0–20.0
20	1	14.7 @ 14.6	2.3–51.05	73.3–86.6	18.3–21.7

TABLE II
ELECTROMAGNETIC PERFORMANCE OF INDUCTORS WITHOUT AND WITH IRON CORES

Turns	*Without iron core*			*With iron core*		
	Q_{peak} *@frequency (MHz)*	*L (nH) (Q > 5)*	$L_{density}$ *(nH/mm²)*	*Q (0.05–5 MHz)*	*L (nH) @0.05 MHz*	$L_{density}$ *(nH/mm²)*
5	19.8@59.85	14.6	14.6	0.57–1.74	229.5	229.5
10	18.0@22.6	38.3	19.2	0.31–1.28	620.8	310.4
15	18.2@17.5	60	20	0.68–1.31	1063	354.3

and 7.13% for quality factor. These relatively small variations indicate that the fabrication process is stable and repeatable. Fig. 4 (b) and (c) compare the electromagnetic performances of inductors with different numbers of turns. The highest Q was found in a 5-turn inductor, for which the peak Q was 37.6 at 21 MHz, with an inductance of 8.17 nH. The highest inductance density was found in a 20-turn inductor, in which the inductance density was 21.7 nH/mm^2 and the inductance was 86.6 nH, whereas the peak $Q$was 14.7 at 14.6 MHz. Fig. 4 (d) shows the influence of width on inductor performance. Performance details for each inductor design are presented in Table I.

Subsequently, the silicon-steel iron cores were inserted into the solenoid inductor, and the performance of the iron-core solenoid inductor was measured. As the performance of silicon steel will obviously decrease at higher frequencies, we decreased the testing frequency range to 0.05–5 MHz, taking measurements at regular intervals of 0.05 MHz (500 data points in all).

Fig. 4 (e) compares the electromagnetic performances of two designs before and after insertion of the iron core. The iron core markedly improves the inductance and inductance density. For the 15-turn 1-mm-wide inductor, the inductance after insertion of the iron core was 1063 nH with an inductance density of 354.3 nH/mm^2, nearly 18 times higher than the same design without the iron core. However, the silicon steel will generate a large induced current in the high frequency and cause serious eddy current loss, causing the inductor to

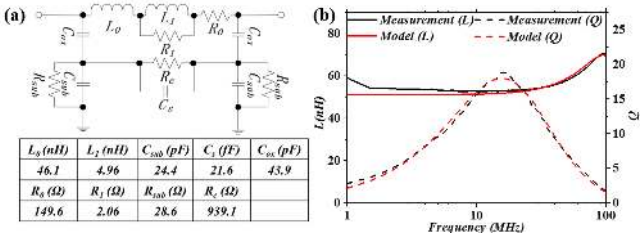

Fig. 5. Equivalent circuit model of a 15-turn 1-mm-wide inductor. (a) Equivalent circuit and extracted parameters. (b) Comparison of measured and modeled parameters.

suffer from a low quality factor. The quality factor of the silicon–steel iron core inductor was approximately one in all measurements. In the future, we will try replacing the silicon–steel core with ferrite to decrease the eddy current loss at high frequency. Fig. 4 (f) compares the iron-core inductors with different numbers of turns. Here the rate of increase in induction is higher than the rate of increase in the number of turns. The performance details for selected inductors with and without iron cores are given in Table II.

Fig. 5 (a) shows an equivalent circuit model of a 15-turn 1-mm-wide inductor. In this model, R_0 and L_0 is the theoretical series resistance and inductance. The combination of L_1 and R_1 represents the variation with frequency due to the skin effect and proximity effect. The C_{ox} represents the coupling capacitance between metal segments and substrate. C_s represents the parasitic capacitances among different parts of metal segments and R_c is the substrate loss resistance. The combination of R_{sub} and C_{sub} represents the parasitic capacitances between inductor and ground metal. The extracted lumped-circuit parameters of the inductor were shown in the table of Fig. 5 (a). Fig. 5 (b) compares the measured and modeled parameters. The result shows modeled parameters are in good agreement with measurements.

IV. CONCLUSION

In this letter, we reported the design of a 3D solenoid inductor that is embedded in the substrate and can integrate an iron core. The fabrication process is CMOS-compatible, any standard CMOS process can be conducted after the inductor was fabricated on the silicon substrate. Eight inductor designs were fabricated with good structural integrity and repeatability. Among the inductors without iron cores, the highest quality factor (37.6 at 21 MHz) was found in a 5-turn inductor, and the highest inductance and inductance density (respectively, 86.6 nH and 21.7 nH/mm^2) were found in a 20-turn inductor. For iron core inductors, an inductance of 1063 nH with an inductance density of 354.3 nH/mm^2 was found in the 15-turn structure, which is the highest inductance density for an MEMS inductor reported thus far, to the best of our knowledge. Based on the structural and performance characteristics of this inductor, we believe that this in-chip solenoid inductor can be used in power MEMS devices, improving the power density and efficiency of these devices. We plan to design and study micro transformers, micro-vibration energy harvesters, and micro electromagnetic motors based on this type of inductor in the near future.

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