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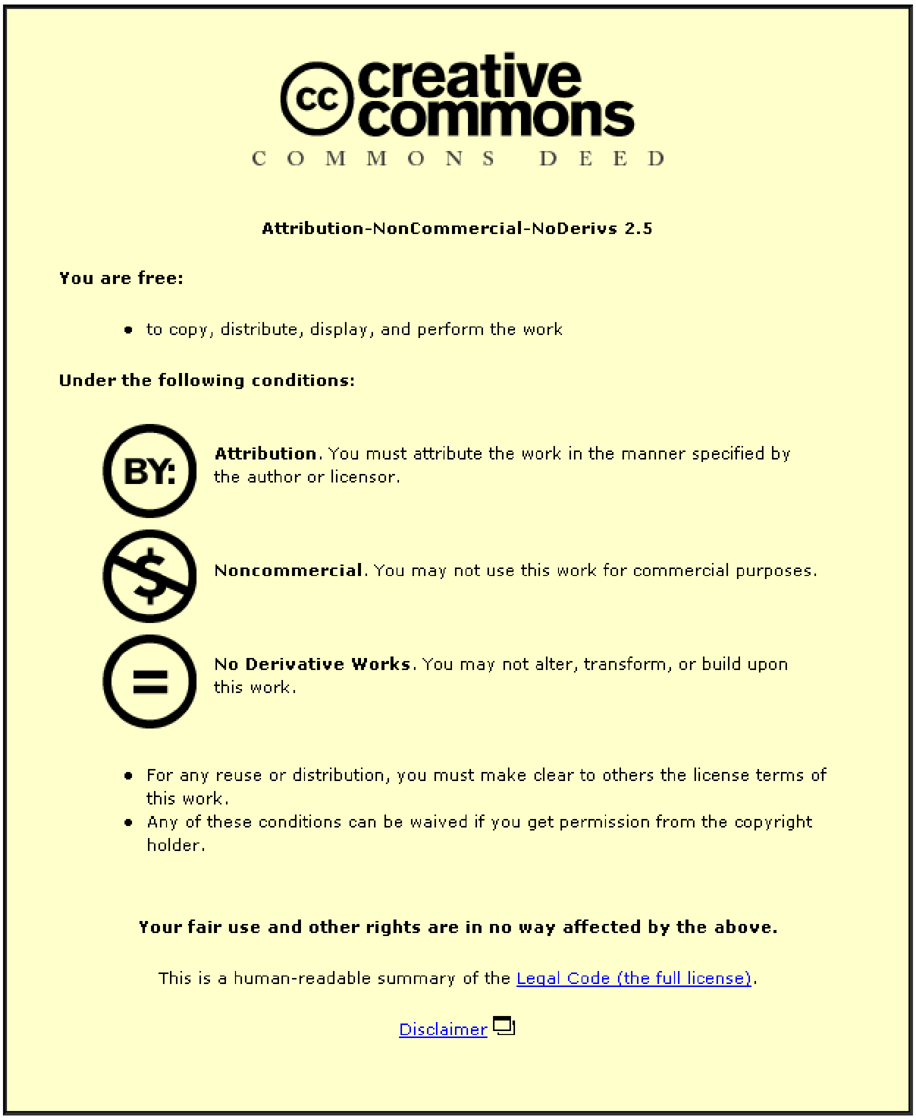

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3D STUDY OF THERMAL STRESSES IN LEAD-FREE SURFACE MOUNT DEVICE

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Abstract: The paper presents the study of non-uniform temperature distributions in a flip chip electronic assembly, and the use of these temperature distributions to analyse the thermal stresses in lead-free solder joints in surface mount devices. The thermal stresses in the solder joints are mainly due to the mismatch in the coefficients of thermal expansions between the component and substrate materials, and temperature gradient in the electronic assembly. The thermo-elasto-visco-plastic finite element analysis is carried out to investigate the extent of thermal stresses induced in solder joints between a surface mount component and a FR4 circuit board (substrate) under conditions of thermal cycling with the chip resistor operating at its full power condition. Three different cases of spatial temperature distributions are considered including one with an experimentally obtained non-uniform temperature distribution. A comparative study of thermal stresses is performed using a near-eutectic SnAgCu solder material for three different thermal cases.

Keywords: Lead-free solder; surface mount device; temperature distribution; thermal stresses; creep

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INTRODUCTION

Solder joints are commonly used in electronic packaging for mechanical support and electrical connection of components. Various technologies are used to create solder joints in electronic packaging depending on the type of electronic products being manufactured. Driven by a desire for miniaturization and increased circuit speed, a surface mount technology (SMT) has been widely adopted in electronic packaging. However, introduction of SMT also brought with it a new era of joints' failures. A major finding of electronic package failures is that the joint material does not demonstrate an adequate ability to sustain deformations due to cyclic variation of temperature during operation [1, 2].

The applications of electronic packages vary from entertainment to aerospace industries. In these applications, solder joints operate under severe temperature conditions compared to their melting temperature - the temperature can change between 218 K to 398 K. This cyclic variation of temperature makes solder joints prone to thermal stresses that can be caused by various reasons. For instance, a body, restricted from its free expansion due to uniform change in temperature experiences thermal stresses as well as a component under a non-uniform change in temperature. Thermal stresses can also be induced due to the mismatch in the coefficient of thermal expansion (CTE) between different components of an assembly [3]. However, in electronic packaging, solder joints experience thermal stresses due to a combined effect of non-uniform temperature distributions in the package when it is powered and the mismatch in CTE between the component and substrate material. The thermal strains in the electronic packaging are cyclic in nature due to the variation in the operating conditions such as powering on and off of the assembly, and cycling variations in the ambient temperature. Therefore, thermal fatigue is one of the major failures in the surface mount solder joints. The problem of fatigue in solder joints is linked to an intermittent character of heat generation during power cycling in the electronic components. The generated heat is dissipated by radiation, convection and conduction. The last mechanism results in the heat flow through the solder joint to the substrate, heating up both. Since the component and substrate materials have different CTEs they experience relative displacement due to expansion. Both the component and substrate are significantly stiffer than the solder joint, so the repeated relative displacements produce a cyclic stress in it and its eventual fatigue failure [1]. This problem has been worsened considerably by the introduction of leadless surface mount devices since the size of the solder joint is very small and there is less compliance between the component and substrate. For instance, leadless devices such as chip capacitors and resistors, as well as ceramic chip carriers, have only a solder fillet to relieve any induced thermal strains. Figure 1 demonstrates the solder joint's crack in the surface mount capacitor due to thermal cycling between 218 K to 398 K [4].

Solder joints are also prone to creep due to high operating homologous temperatures (T_h, the ratio of operating and melting temperature in absolute scale). For most of the solder materials T_h is about 0.6 at the room temperature (RT). Working at such high T_h, the solder usually exhibits very complicated rate- and temperature- dependent mechanical behaviours such as viscous creep, stress relaxation, and plasticity [2, 4, 5]. This results in accumulation of creep damage alongside with thermo-mechanical damage. Predicting the reliability of solder joints under such conditions is complicated since they are at complex states of stress and strain [1, 3]. In addition, an exchange of lead-containing solder materials with lead-free ones added more concerns for the electronic industries with regard to manufacturing of reliable products. Eutectic or near-eutectic SnAgCu alloy used as possible replacement for well-established SnPb solder alloys are considerably less studied. However, the use of experimental techniques such as accelerated tests, for obtaining test data to assess the reliability of solder joints is both time-consuming and difficult to extrapolate to predict operational reliability. Recently, numerical simulations based on finite element analysis became a tool to investigate the reliability of solder joints subjected to thermal cycling. Most simulations deal with reliability for conditions of thermal cycling and power cycling, usually, uniform temperature distributions in the assembly are considered linked to the variation in ambient operating conditions. Thermo-mechanical analysis of a chip-scale package (CSP), assembled using both lead-free and lead-containing solder materials [6], and thermal cycling analysis of flip-chip solder joint reliability [7] are typical examples. However, research into the effect of non-uniform temperature distributions in assemblies due to continuous heat dissipation by the chip resistor along with cyclic variation in the ambient temperature is insufficient. Hence, this paper focuses on effect of actual temperature distributions in the powered flip-chip electronic assembly and finite-element simulations using these temperature distributions for varying ambient temperature. The finite-element model accounts for both plasticity and the creep behaviour of a new lead-free SnAgCu solder alloy. A comparison of 3D evolution of thermal stresses in the solder joint is performed for three different thermal cases including the experimentally measured temperature distribution for powercycling.

EXPERIMENTAL ANALYSIS

In order to obtain the temperature distribution in an electronic assembly, experiments were carried out with a flip-chip electronic assembly for power cycling condition, using an infrared (IR) Thermosensorik camera. An IR technique is a contactless temperature measurement technique where radiation emitted from a surface is captured by a thermal camera and processed for obtaining temperature distribution over that surface. Although the flip-chip assembly used in experiments is different from the component (chip resistor) modelled, the general size and joint distribution make both flip-chip and chip resistor assemblies comparable, allowing the flip-chip experimental results to provide an indication of the temperature gradients in the chip resistor.

Specimen preparation

The flip-chip specimens were silicon-on-silicon multi-chip modules (MCMs) that matched the description of those used in a previous experiment [8]. Both MCMs consisted of a 3 mm × 3 mm × 0.5 mm "heater" chip that bore a large central resistive element (the heater) in addition to small aluminium tracks and 36 connection pads. The "carrier" chip was larger at 6 mm × 6 mm × 0.5 mm and included larger ball grid array pads for external connections, as well as the corresponding pads to match those on the heater chip. The latter was attached to the carrier chip so that a standoff height of 35 μm (without underfill) was achieved. The MCMs were subsequently attached to the substrate by a thermally conductive adhesive pad. A schematic of the assembled specimen is shown in Fig. 2.

The specimens were attached to either a copper or FR4 substrate and sprayed with matt black paint to achieve uniform emmissivity over the surface. The specimens were mounted vertically, powered at 1.2 W, and cooled by free convection. The camera, fitted with the micro lens, was mounted on the tripod, the specimen was powered on for few minutes to stabilize the temperature distribution in the specimen, then micro lens was focused on the specimen and the temperature distribution was captured.

Experimental results and discussion

Experiments were carried out for two power dissipation conditions (0.44 W and 1.2 W) for two specimens, one with FR4 and another with copper as substrate materials [4]. These power dissipation conditions are selected to establish a relation between temperatures of the chip and substrate. The captured temperature distribution for continuous power dissipation of 1.2 W over a chip surface is given in Fig. 3, along with the path used for temperature distribution analysis over the chip. Figure 4 shows the temperature distributions across the width of the chip for both substrates. The effect of the substrate material on the temperature distribution over the chip surface is very clear from the comparison of these temperature distributions. Since copper is a better heat conductor than FR4, more heat is dissipated from the flip-chip assembly to the atmosphere, resulting in lower temperature magnitudes. For both specimens the maximum temperature is observed at the centre of the chip, where a heat-generating resistive element is situated. The distribution of the temperature over the chip surface is nearly symmetric for the chip mounted on copper substrate while that for the chip with a FR4 substrate is asymmetric. This may be due to the manufacturing deficiency with a skewed resistive element. The patches appearing cool in the image may be attributed to non-uniform application of black paint. From the variation of chip and substrate temperature with power dissipation, following relation is deduced,

$$T_{\mathrm{sub}} = 0.18 T_{\mathrm{chip}} + 299.4 \,, \tag{1}$$

where T_{chip} is chip temperature and T_{sub} is substrate temperature.

This experimental study confirms that, as expected, FR4 substrate induces a higher level of temperature in the flip-chip assembly. Also the average temperature gradient, which is a difference between maximum and minimum temperature in the assembly, is higher for specimen with FR4 as a substrate material. Therefore, the temperature distribution obtained for flip-chip assembly with FR4 substrate is used as temperature boundary conditions for thermal analysis, which is later used in structural analysis.

THERMAL ANALYSIS

Finite element analysis is broadly used to study various engineering problems such as new product design, improving the existing products, their reliability, in studies of new materials etc. Due to the legislation introduced across the world to remove the lead content from electronic products, reliability of the new generation of lead-free solders should be thoroughly tested before introduction into products. The finite element technique enables a researcher to simulate the various operating conditions of solder joints and study the structural behaviour such as thermo-mechanical, creep, and low cycle fatigue damage. In finite element analysis the structural problem is represented in terms of a mathematical model that is solved for field variables. In the present work finite element analysis has been used to obtain the temperature distribution in the chip resistor assembly and study the structural response of solder joint for three different thermal cases.

Finite element model

The finite element analysis, both thermal and structural, of a chip standard Panasonic 1206 resistor was implemented with commercial software ANSYS. The geometric dimensions of different components of this resistor assembly are shown in Fig. 5. Due to the construction of the chip resistor assembly, which is symmetric, only one half of its geometry is shown for a side view (Fig. 5a) and considered for finite element modelling. A 3D finite element model is considered for the thermal stress study to capture the entire 3-dimensional distribution of the temperature and its effect on the thermal stress integrity of the solder joint.

Figure 6 shows the meshing used in the assembly as well as the critical region. Since the solder joint is our area of interest, a finer mesh pattern has been used there. The finite element model is built with 8-noded hexahedral elements. ANSYS employs an error approximation technique based on the Zienkiewicz-Zhu scheme. In this scheme, an initial stress error contributed by each element at each node is calculated as follow [9]:

$$\left\{\Delta\sigma_n^i\right\} = \left\{\sigma_n^a\right\} - \left\{\sigma_n^i\right\} \tag{2}$$

where $\left\{\Delta\sigma_n^i\right\}$ is the stress error vector at node n for element i, $\left\{\sigma_n^a\right\}$ is the averaged stress vector at node n, $\left\{\sigma_n^i\right\}$ is the stress vector of node n of element i.

Then, the stress bounds are estimated considering the above error:

$$\sigma_j^{mnb} = \min\left(\sigma_{j,n}^{a} - \Delta\sigma_n\right), \tag{3}$$

$$\sigma_j^{mxb} = \max\left(\sigma_{j,n}^{a} + \Delta\sigma_n\right); \tag{4}$$

where σ_j^{mnb} is the nodal minimum of stress quantity (SMNB), σ_j^{mxb} is the nodal maximum of stress quantity (SMXB).

An error estimation study was carried out at the fillet region of the solder joint to assess the mesh quality for the creep analysis. In this study a linear static analysis was conducted for different mesh patterns and related element dimensions, and the maximum nodal stress (SMX) in the fillet of solder joint was assessed together with its bound SMXB. The mesh was considered to be suitable with regard to convergence when the difference between the magnitudes of the ratio of SMXB and SMX for two consecutive iterations for the mesh pattern achieved the prescribed level. There are two main regimes of heat transfer in electronics packages with respective types of variations of thermal stresses – transient (power on/off) and steady-state (during operation). In both cases, for the theory of isotropic thermal stresses and strains, the temperature distribution $T(x, y, z, t)$ in the package is calculated by solving the heat conduction equation (with prescribed initial and boundary conditions that are described below [10]):

$$\nabla^2 T = \frac{\rho C_v}{k}\frac{\partial T}{\partial t} - \frac{W}{k} \tag{5}$$

where $\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$; $T \equiv T(x, y, z, t)$ is instantaneous absolute temperature; C_v is heat capacity per unit mass; ρ is mass density; k is the heat conduction coefficient;

W is heat generation per unit time per unit volume.

Result and discussions

Thermal stresses are the major cause of concern in the reliability of solder joints, as they operate in high temperature conditions compared to their melting temperature. Hence it is important to model the exact thermal field corresponding to the in-field conditions for the structural analysis. The discussed experimental work gives only the surface temperature of the chip assembly. In order to obtain the internal temperature distribution in the chip resistor assembly a simple thermal analysis is carried out considering only a conduction heat transfer. For this thermal analysis surface temperatures obtained from the experiment are used as boundary conditions. The chip resistor can operate in the temperature range between 398 K and 218 K. Therefore, the maximum temperature a chip can achieve is 398 K when it is operating at its maximum power. Considering this chip temperature (T_{chip}), the substrate temperature (T_{sub}) was calculated using Eq. (1). The difference between temperatures of the substrate and chip gives the temperature gradient on the assembly when chip is operating at its maximum power condition. The thermal analysis was carried out for two extreme ambient temperatures 398 K and 218 K with maintaining the same temperature gradient in the assembly due to the fact that the chip resistor is continuously dissipating heat at its maximum power.

Figure 7 shows the thermal zones used for the application of boundary conditions based on the experimental measurements. Table 1 gives the temperature levels used for different zones of the resistor assembly for the ambient temperature 398 K and 218 K. For example, to apply the temperature boundary condition due to heat generated by resistive element, an area covered by it (zone I in Fig. 7) on the top surface of the component is selected. Similarly temperature zones are selected based on the temperature data collected from the experimental work and respective temperature distributions are applied. A linearly varying temperature is applied on the bottom surface of the substrate, which is between zone H and I to replicate the reality when chip resistor is powered on. The obtained temperature distributions after thermal analysis are shown in Figs. 8 (a) and (b) for ambient temperature 398 K and 218 K, respectively. These two temperature profiles are used in the subsequent structural analysis as parts of the thermal history.

THERMAL STRESS ANALYSIS

Material properties

The chip resistor assembly consists of a chip component made of alumina, a solder joint, a copper pad and a FR4 substrate. Since the material properties of the solder alloy greatly varies with the temperature, temperature-dependent elasto-plastic material properties of Sn3.8Ag0.7Cu (SAC) alloy [11,12] has been used for solder joint, which is given in Table 2. In this finite-element simulation, the solder material is modelled with the bilinear kinematic hardening (BKIN) material model. The model’s name is derived from the way a stress-strain curve is modelled and the type of hardening rule used for the plastic flow. In the model, both elastic and plastic regions are represented by two straight lines with different slopes. The slope of the plastic part is linked to the tangent modulus, which is given in Table 2. The kinematic strain hardening is used to include the Bauschinger effect due to cyclically varying thermal loads. The material properties of 96% alumina (Al_2O_3) were used for the chip component body, whilst high-conductivity copper and FR4 material properties were used for pad and substrate respectively.

There is a significant amount of research regarding the constitutive equations for creep deformation in both lead and lead-free solder materials. For instance, Wiese *et al.* [13] studied the creep behaviour of Sn4.0Ag0.5Cu for both bulk solder and flip chip solder joints. Their study identified two types of creep mechanisms for steady-state deformation linked to the climb-controlled (at low stresses) and combined glide/climb (at high stresses) dislocation behaviour. Similar studies were carried out by Schubert *et al.* [14] and Zhang *et al.* [15], and both identified two regimes of the stress-strain rate behaviour. Both modelled the steady-state creep rate with a classical hyperbolic sine creep law:

$$\dot{\varepsilon}_{\mathrm{cr}} = A_1 \left[\sinh\left(\alpha\sigma\right)\right]^n \exp\left(-\frac{Q}{RT}\right) \tag{6}$$

where constant $A_1 = 277984$ s^{-1}, a multiplier to equivalent stress $\alpha = 0.02447$ MPa^{-1}, a stress exponent $n = 6.41$, the activation energy $Q = 54041$ J/(K·mole), the gas constant $R = 8.314$ J/mol, $\dot{\varepsilon}_{\mathrm{cr}}$ is a steady state creep strain rate, σ is the equivalent stress.

This law reduces to a power law in the low stress area ($\alpha\sigma < 0.8$) and to an exponential model in the high stress area ($\alpha\sigma > 1.2$) [16-18]. The hyperbolic sine creep model is adequate for most lead and lead-free solder materials, and it is used in the present study to simulate the viscous behaviour of the solder joint due to its high operating temperatures. The creep parameters, obtained by Schubert *et al.* for Sn3.8Ag0.7Cu solder material, are used in the creep analysis [14, 16].

Thermal loading and boundary conditions

To properly estimate the effect of the real spatially non-uniform temperature distributions on evolution of thermal stresses, three cases of thermal boundary conditions are applied to the resistor assembly in the finite element elasto-plastic and creep analysis. Each case represents a various type of accounting for thermal conditions within the same thermal history consisting of the reflow process and dwell at room temperature before thermal cycling. The reflow simulation in terms of cooling from the melting point gives an amount of residual stress induced in the solder joint when the temperature of the assembly brought down from 490 K to the room temperature. A typical thermal history used in thermal stress analysis is given in Fig. 9, with duration of the total temperature cycle (DEFGH) 1320 sec. Point H in Fig. 9 denotes the end of the first thermal cycle and the begin of the next one. All the subsequent cycles have the same thermal history as DEFGH. Following are the three different cases used in the finite element analysis of continuously heat dissipating chip with a varying ambient temperature during thermal cycles after reflow and the dwell at the room temperature.

Case A: In this case, spatially uniform temperature distributions are assumed the entire resistor assembly, e.g. during hot dwell (DE) the entire assembly is at 398 K, while during the cold dwell (FG) it is at 218 K.

Case B: In this case, Eq. (1) is used to obtain the temperature of the substrate in dependence of that on the component. For instance during hot the dwell (DE) a uniform temperature of 398 K is applied to the chip component, solder joint and copper pad, while the substrate's temperature is 321.5 K. During the cold dwell (FG) the chip component, solder joint and copper pad are at 294 K and the substrate temperature is 218 K. It is assumed that the assembly has the same temperature gradient as for the hot dwell due to continuous heat dissipation at its maximum power.

Case C: In Case C, the actual temperature gradient based on the thermal FE analysis for the chip resistor operating at its full load and the varying ambient temperature is considered. Hence, the temperature profile shown in Fig. 8(a) is used for the hot dwell (DE) and the one in Fig. 8(b) is used for the cold dwell (FG).

A symmetry boundary condition is applied on the symmetry faces (Fig. 6) of the assembly to represent the structural symmetry and to prevent a rigid body motion. The bottom nodes on the symmetry plane are also constrained to prevent the rigid body motion in the Y-direction.

Results and discussions

In our finite element analysis, the chip resistor is subjected to 5 temperature cycles (see Fig. 9). The results of simulations are presented only for the solder joint, since it is our area of interest. The reflow process is commonly used in surface mount devices to create solder joints. In this process the whole assembly passes through an oven where the maximum temperature is above the melting point of the lead-free solder alloy. Hence, it is important to know the stress induced in the solder joint due to cooling of the assembly in the reflow process from 390 K to room temperature. Different components of the thermal stresses in the solder joint are studied after the reflow and shown in Fig. 10. The distributions of the thermal stresses show that the fillet of the solder joint is the area of stress concentration and the magnitude of the residual stress induced in the solder joint is above the yield stress of the SAC solder alloy at room temperature - 38 MPa. As expected, σ_{xx} is the dominant stress component due to the contraction of the assembly with decrease in temperature, which also results in shear stress σ_{xy}. The variation of the component stress σ_{xx}, at location of stresses with maximum magnitude (compressive in this case) in the fillet (point 'O' in Fig. 10a), over the dwell at room temperature and temperature cycles was studied and is shown in Fig. 11(a). The room-temperature dwell results in a relatively quick decrease of residual stresses during the first 10 min. due to the relaxation process. The latter decelerates after this initial stage of the dwell, resulting in 62% decline after first hour. The stress variation is presented only for 3 cycles due to a transition to a quasi-stable configuration after first four thermal cycles. The evolution of the component stress demonstrates the effect of three different thermal boundary conditions. The magnitudes of stress are similar for Cases B and C; however Case A induces compressive stresses of higher magnitude than in B and C. Another important observation is that in the case of the uniform temperature distribution (Case A) the relaxation of stress at cold dwell is absent due to a lower homologous temperature ($T_{\mathrm{h}} = 0.44$). But at hot dwell all three cases show comparable extents of relaxation due to higher T_{h}. As temperature cycling progresses the stress levels at hot dwell practically coincide for all three cases. The evolution of shear stresses in the solder joint is also studied for the maximum stress location in the fillet (point 'P' in Fig. 10d). The Fig. 11(b) demonstrates the variation of shear stresses for reflow, relaxation at room temperature and 3 temperature cycles. The general character and main features of the shear stress evolution are similar to those for the stress component σ_{xx}, with Case A exhibiting higher stress levels and Case C lower stress levels. Here also no relaxation of stress at cold dwell is observed in case of Case A, and stress levels converge for all three cases at hot dwell as the cycle progresses.

Since the stress levels induced in the solder joint are in plastic region, they cause an irreversible strain in it. At the same time, deformation in the solder joint due to creep also contributes to the permanent strain. Therefore inelastic strain, caused by a combined effect of plasticity and creep, was calculated for the solder joint at point ‘P’ in the fillet. Figure 12 shows the evolution of inelastic strain for Cases A, B and C. All three cases correspond to thermal ratcheting after the reflow and dwell at room temperature: each thermal cycle results in the incremental increase in the levels of inelastic strains. As expected, the accumulated inelastic strain (permanent) strain at the end of 5 temperature cycles is maximum for Case A, while that in Case C is minimum. The inelastic strain accumulation after five thermal cycles is 33% and 40% lower for Cases B and C, respectively, than that in Case A. In the latter case, there is no inelastic strain accumulation at cold dwell due to low homologous temperature, resulting in the absence of stress relaxation. In contrast the inelastic strain accumulation takes place for both hot and cold dwells in Cases B and C. However, the amount of accumulation is greater for cold dwell than that of hot dwell due to higher level of stress in the solder joint during cold dwell.

Conclusions

In this paper, the experimental work is aimed at determination of the temperature profiles in the working flip-chip assembly. It is demonstrated that the real spatial temperature distributions are not uniform, resulting in thermal gradients in the assembly. Finite element simulations are used to study the effect of non-uniformity as opposed to the standard assumption of uniform temperature distributions in microelectrinics components when they are powered. This is implemented in terms of three variants of thermal boundary conditions, linked to experimental results. Their effect on thermal stresses and inelastic strain accumulation in the surface-mount solder joint is studied. From the three cases considered, the non-uniform temperature distribution (Case C) in the resistor assembly demonstrates the lowest stress levels as well as inelastic strain accumulation while the uniform temperature distribution (Case A) demonstrates the highest ones. Obviously, the common assumption of the uniform temperature field in powered component overestimates thermal ratcheting for the studied loading history. Therefore, it is very important to consider the actual temperature distribution rather than a uniform one in the finite-element simulation to study stress and strain conditions in the solder joint.

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Figure captions

Figure 1: Solder fillet cracking in thermal cycling test between 218 K to 398 K on 1812 size ceramic capacitors [4]

Figure 2: Schematic of specimens used in experiments

Figure 3: Temperature distribution (in K) in a chip mounted on FR4 substrate at 1.2 W

Figure 4: Effect of substrate on temperature distribution in the chip for free convection

Figure 5: Geometrical details of chip resistor assembly: side view (a) and front view (b)

Figure 6: Meshing of chip resistor assembly

Figure 7: Zones of thermal boundary conditions: side view (a) and top view (b)

Figure 8: 3D temperature distributions (in K) in chip resistor assembly at ambient temperature 398 K (a) and 218 K (b)

Fig 9: A typical thermal history used in thermal stress analysis: Cooling from 490 K (AB) - 48 sec; dwell at room temperature (BC) - 3600 sec; ramp CD - 300 sec; hot & cold dwell (DE, FG) - 300 sec; ramps EF & GH - 360 sec

Figure 10: Distribution of thermal stresses in solder joint after reflow: (a) σ_{xx}; (b) σ_{yy}; (c) σ_{zz}; (d) σ_{xy}

Figure 11: Evolution of component stress σ_{xx} (a) and shear stress σ_{xy} (b)

Figure 12: Accumulation of inelastic strain

Table 1: Temperature levels at different zones for two extreme ambient temperatures

Thermal Zone	Boundary conditions at ambient temperature 398 K	Boundary conditions at ambient temperature 218 K
I	398	294.5
J	386	282.5
K	382	278.5
L	384	280.5
M	379	275.5
N	376	272.5
O	328	224.5
P	343	239.5
Q	321.5	218

Table 2: Material properties for SAC solder [11, 12, 19]

Temperature (K)	Young's modulus (MPa)	CTE (ppm/K)	Yield stress (MPa)	Tangent modulus (MPa)
298	44400	21.2	38	154
348	30700	21.7	30	134
423	18800	23.0	17	132

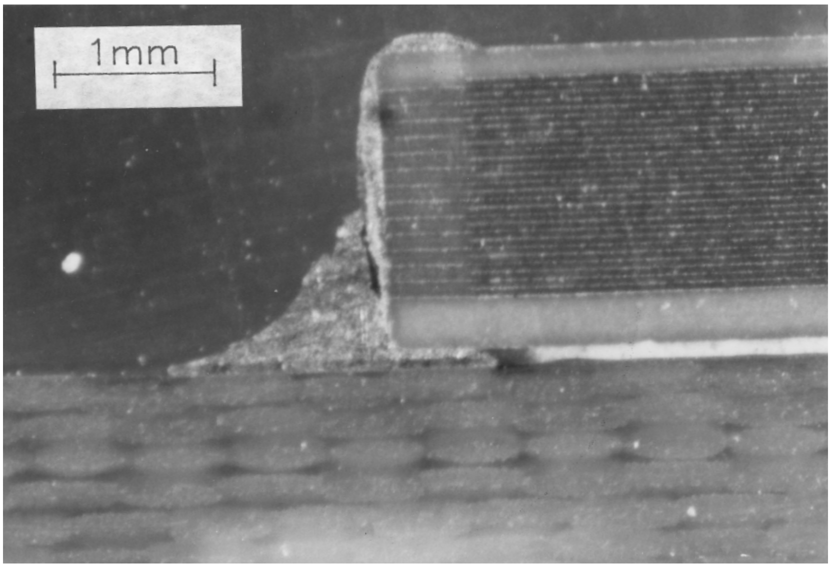


Figure 1

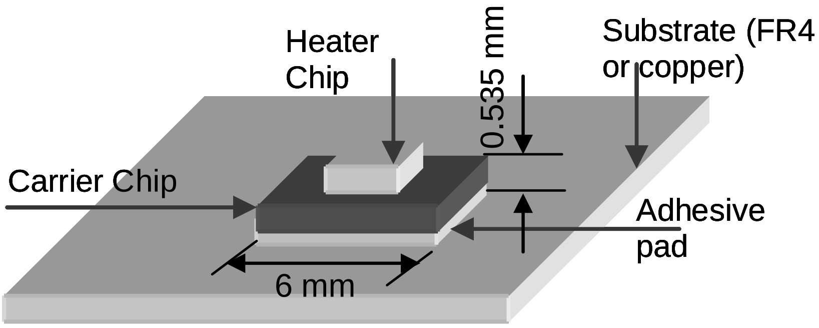

Heater Chip
0.535 mm
Substrate (FR4 or copper)
Carrier Chip
Adhesive pad
6 mm

Figure 2

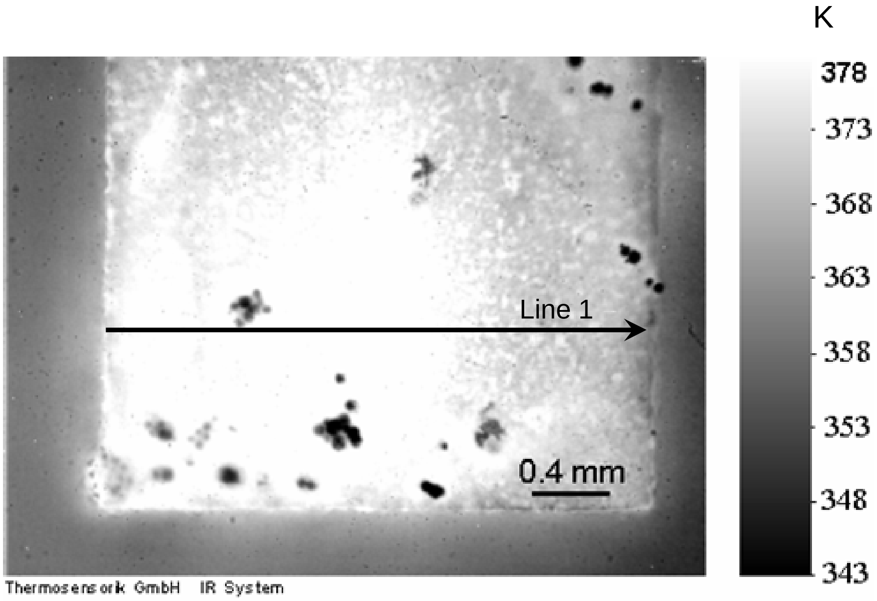

K
378
373
368
363
358
353
348
343
Line 1
0.4 mm
Thermosensorik GmbH IR System

Figure 3

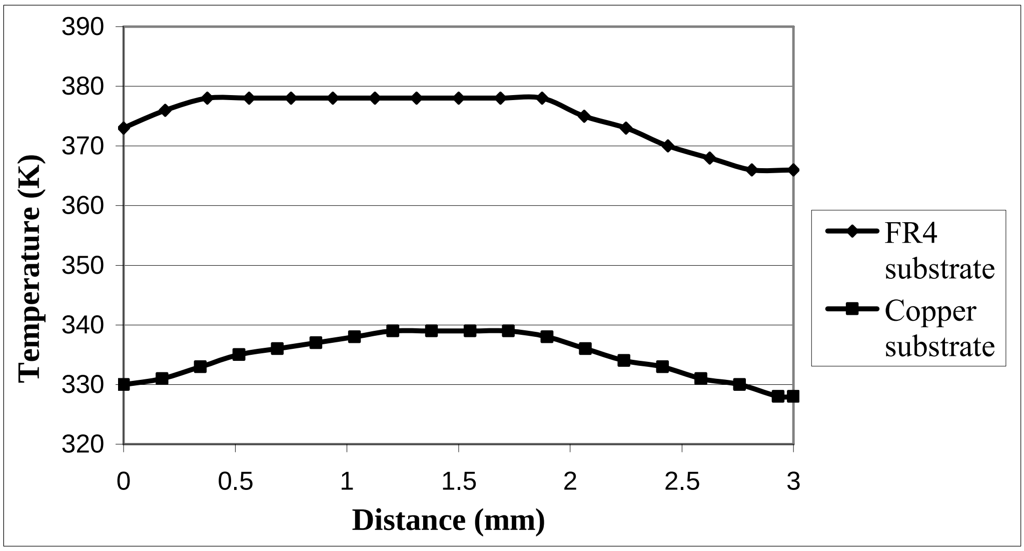
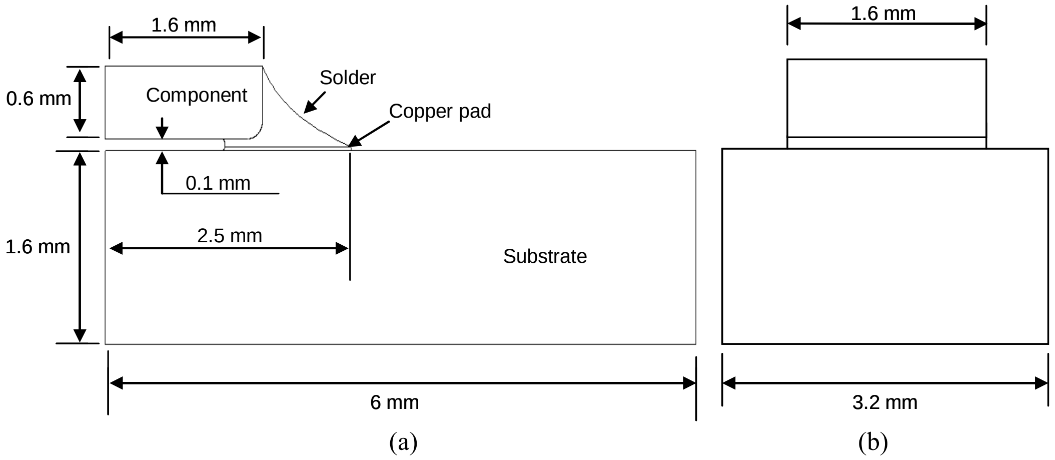

390
380
370
360
350
340
330
320
Temperature (K)
0
0.5
1
1.5
2
2.5
3
Distance (mm)
FR4 substrate
Copper substrate

Figure 4


1.6 mm
0.6 mm
Component
Solder
Copper pad
0.1 mm
1.6 mm
2.5 mm
Substrate
6 mm
1.6 mm
3.2 mm

(a) (b)

Figure 5

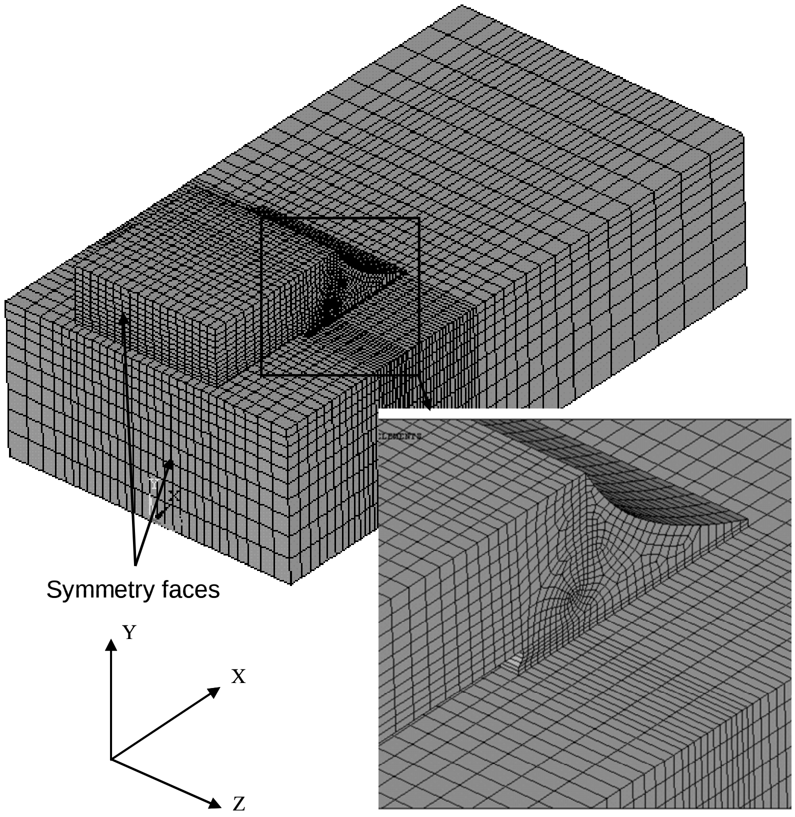
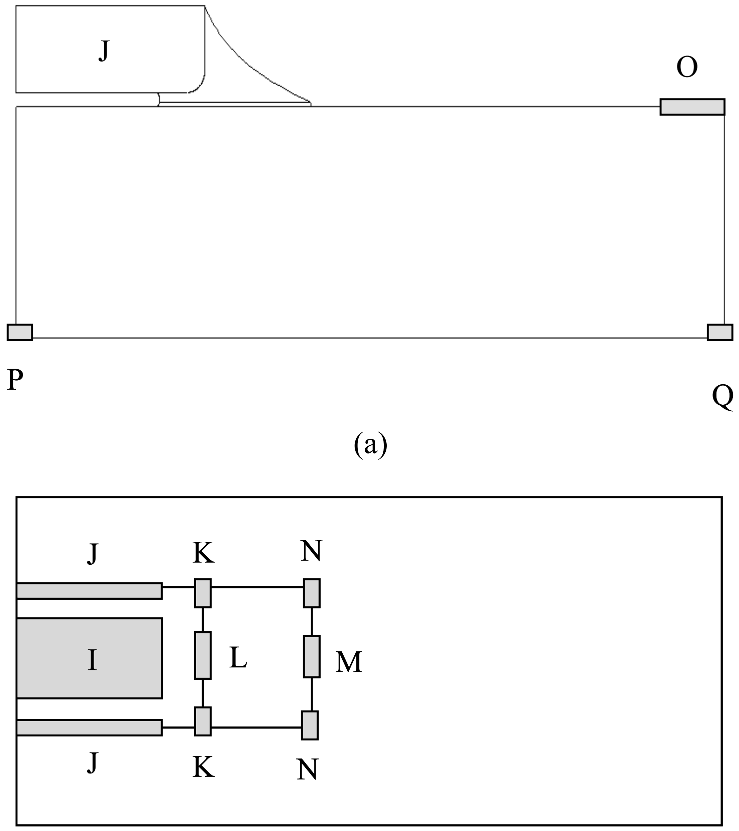

Symmetry faces
Y
X
Z

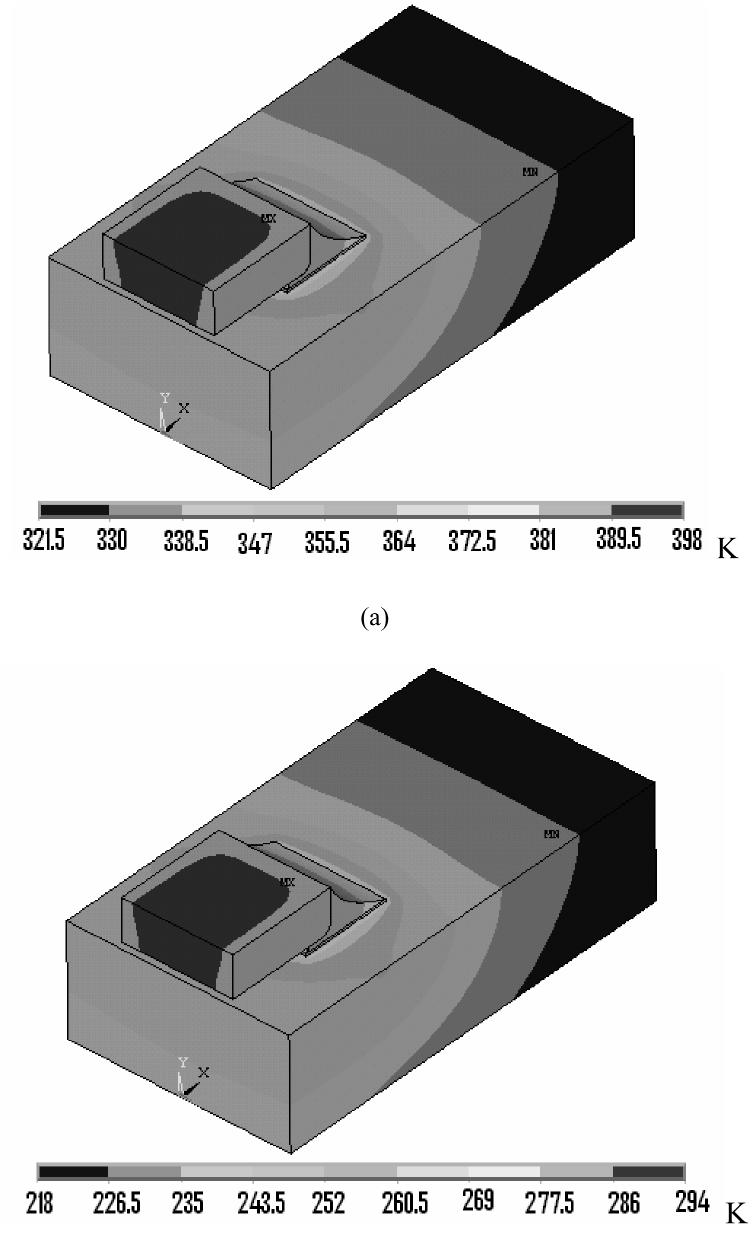
Figure 6


J
O
P
Q
J
K
N
I
L
M
J
K
N

(a)

(b)

Figure 7


MN
MX
Y
X
321.5
330
338.5
347
355.5
364
372.5
381
389.5
398
K
MN
MX
Y
X
218
226.5
235
243.5
252
260.5
269
277.5
286
294
K

(a)

(b)

Figure 8

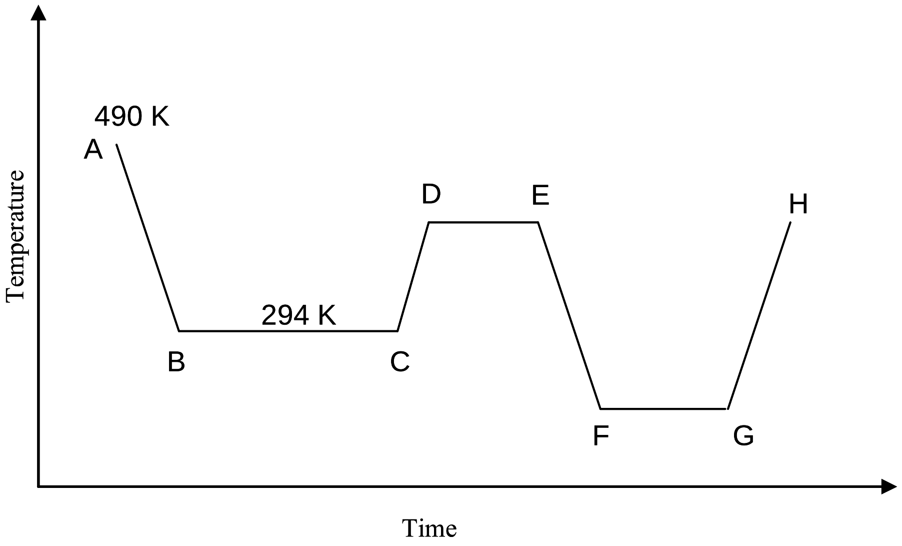
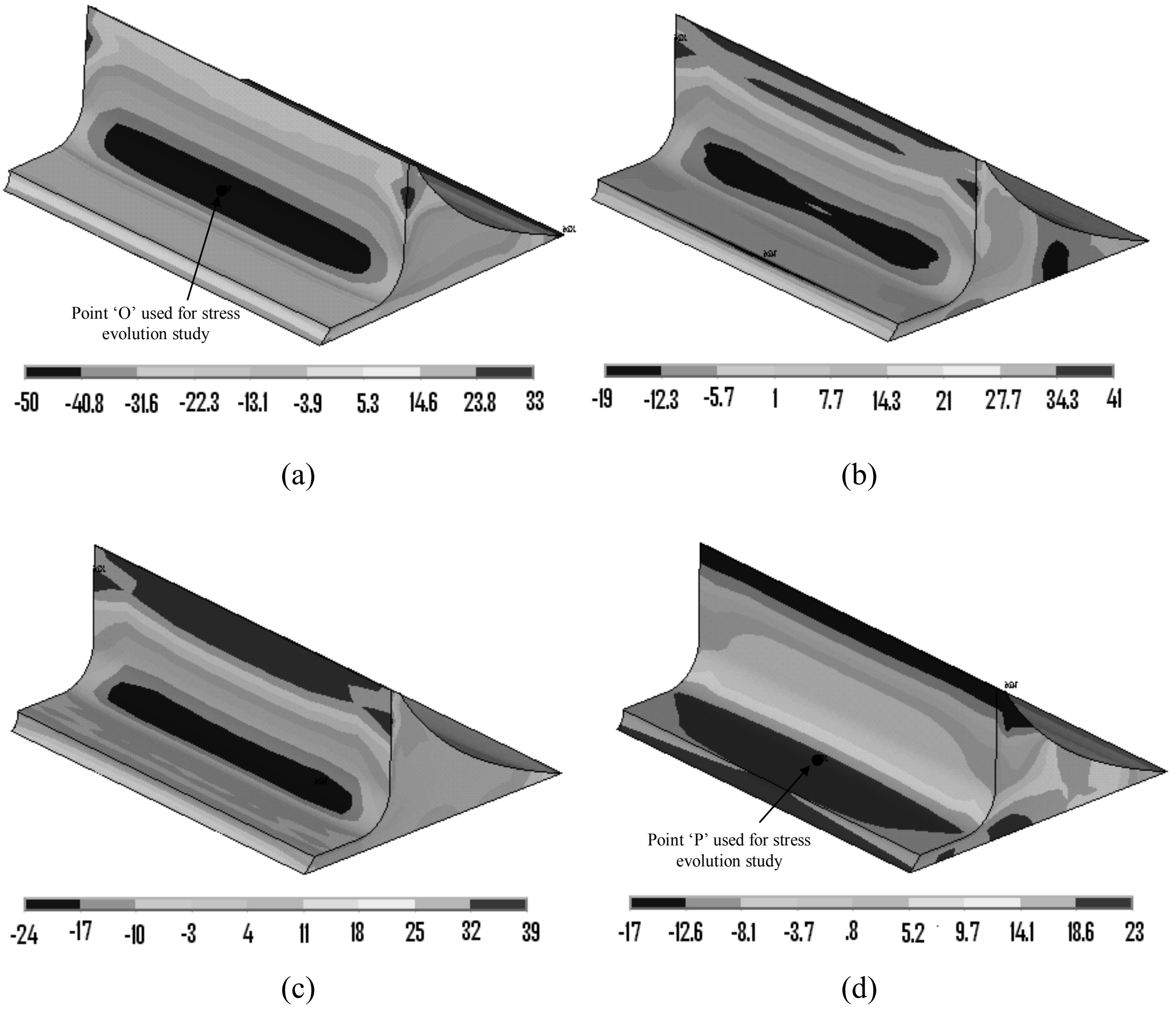


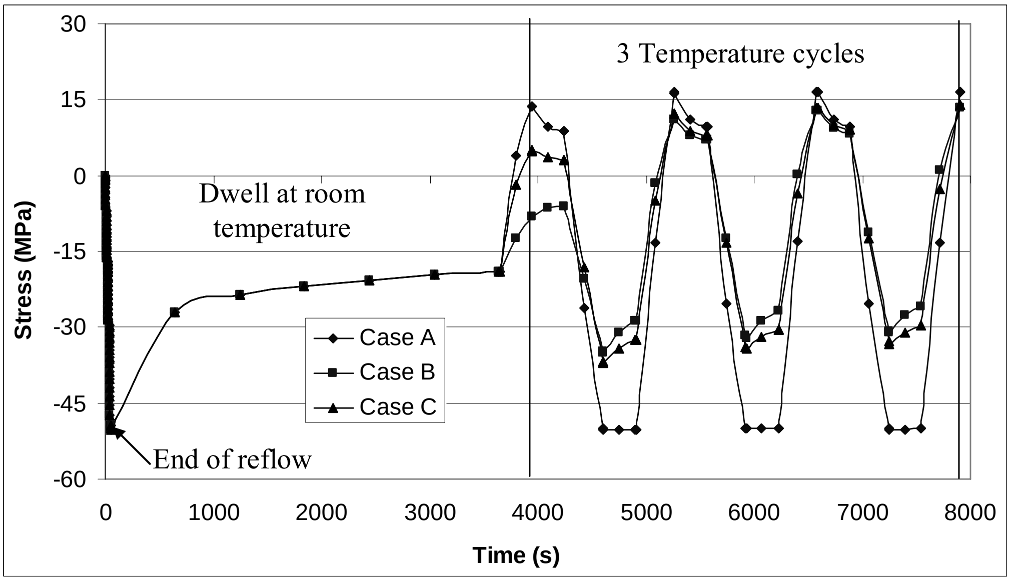
Figure 9



(a) (b)

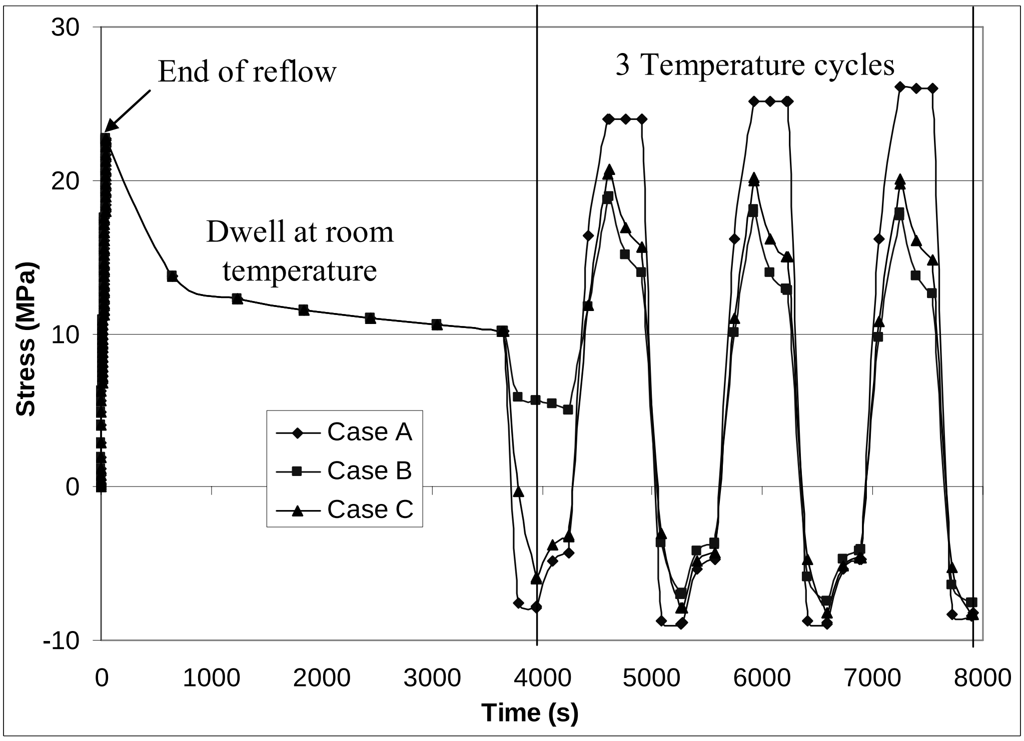
(c) (d)

Figure 10



30
15
0
-15
-30
-45
-60
Stress (MPa)
0
1000
2000
3000
4000
5000
6000
7000
8000
Time (s)
3 Temperature cycles
Dwell at room temperature
End of reflow
Case A
Case B
Case C

(a)



30
20
10
0
-10
Stress (MPa)
0
1000
2000
3000
4000
5000
6000
7000
8000
Time (s)
End of reflow
3 Temperature cycles
Dwell at room temperature
Case A
Case B
Case C

(b)

Figure 11

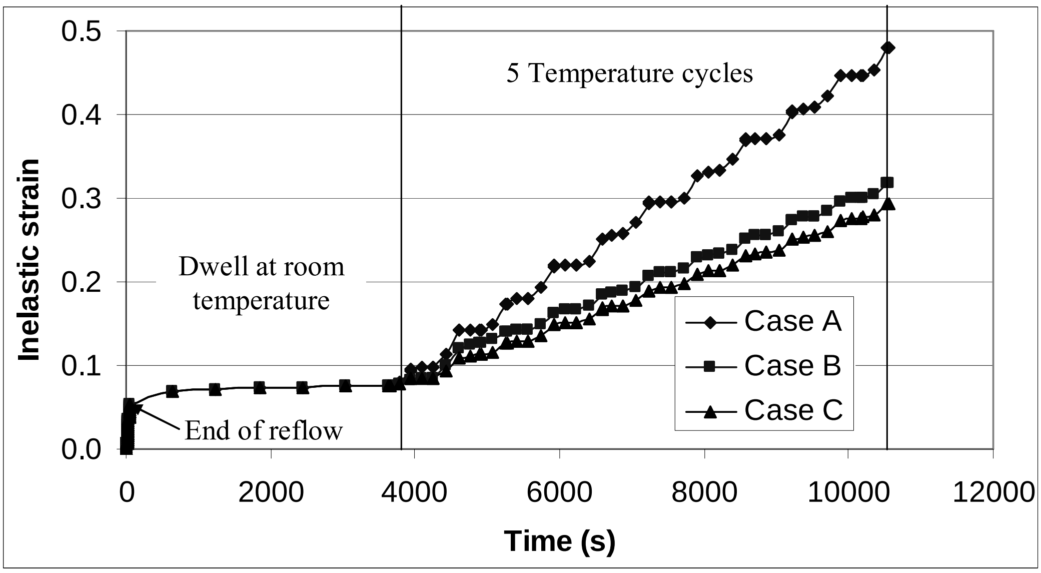

0.5
0.4
0.3
0.2
0.1
0.0
Inelastic strain
0
2000
4000
6000
8000
10000
12000
Time (s)
5 Temperature cycles
Dwell at room temperature
End of reflow
Case A
Case B
Case C

Figure 12