# 4.4 kV β-Ga<sub>2</sub>O<sub>3</sub> Power MESFETs with Lateral Figure of Merit exceeding 100 MW/cm<sup>2</sup>

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Abstract—Field-plated (FP) depletion-mode MOVPE-grown β-Ga<sub>2</sub>O<sub>3</sub> lateral MESFETs are realized with superior reverse breakdown voltages and ON currents. A sandwiched SiN<sub>x</sub> dielectric field plate design was utilized that prevents etching-related damage in the active region and a deep mesa-etching was used to reduce reverse leakage. The device with L<sub>GD</sub> = 34.5 µm exhibits an ON current (I<sub>DMAX</sub>) of 56 mA/mm, a high I<sub>ON</sub>/I<sub>OFF</sub> ratio > 10<sup>8</sup> and a very low reverse leakage until catastrophic breakdown at ~ 4.4kV. The highest measurable  $V_{BR}$  recorded was 4.57 kV (L<sub>GD</sub> = 44.5  $\mu$ m). An LFOM of 132 MW/cm<sup>2</sup> was calculated for a V<sub>BR</sub> (= V<sub>DS</sub> - V<sub>GS</sub>) of ~ 4.4kV. The reported results are the first >4kV-class Ga<sub>2</sub>O<sub>3</sub> transistors to surpass the theoretical FOM of Silicon. These are also the highest IDMAX and lowest Ron values achieved simultaneously for any β-Ga<sub>2</sub>O<sub>3</sub> device with  $V_{BR}$  > 4kV to date. This work highlights that high breakdown voltages (VBR), high lateral figure of merit (LFOM) and high ON currents can be achieved simultaneously in β-Ga<sub>2</sub>O<sub>3</sub> lateral transistors.

*Index Terms*—Ga<sub>2</sub>O<sub>3</sub>, MESFETs, MOVPE, regrown contacts, breakdown, kilovolt, lateral figure of merit, passivation, field plates.

## I. INTRODUCTION

**B**eta-Ga<sub>2</sub>O<sub>3</sub>, a unipolar ultra-wide bandgap (UWBG) semiconductor ( $E_g = 4.6-4.9$  eV), has gained increasing importance as a material with tremendous promise to enable power-efficient next generation high voltage power devices. In the last decade of research, β-Ga<sub>2</sub>O<sub>3</sub> material system has witnessed several milestones in bulk and epitaxial single crystal growth, doping, device design, and processing[1]–[4], [4]–[11]. β-Ga<sub>2</sub>O<sub>3</sub>-based devices with breakdown voltage up to 8 kV and critical breakdown fields exceeding the theoretical limits of SiC and GaN have been demonstrated[7], [12], [13]. While substantial progress has been made in β-Ga<sub>2</sub>O<sub>3</sub> devices,

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understanding its material and device physics to take full advantage of its intrinsic properties is still far from mature.

Several field management techniques have been demonstrated in Ga<sub>2</sub>O<sub>3</sub> devices to enhance the average breakdown fields and blocking voltages - the most popular technique being the field-plate (FP) design. But most of these devices suffer from either high reverse leakage that leads to a premature breakdown or low ON currents (and high R<sub>ON</sub>) due to the non-ideal FP process flow involving etching in the gate region [7], [8]. In this letter, we demonstrate over 4 kV-class all-MOVPE-grown β-Ga<sub>2</sub>O<sub>3</sub> lateral MESFETs with a gate FP design using SiNx field plate/passivation dielectric that achieves high ON currents, low reverse leakage, and LFOM exceeding 100 MW/cm<sup>2</sup>, simultaneously. We address the critical metrics of V<sub>BR</sub> (breakdown voltage), R<sub>on,sp</sub> (specific onresistance), and ON current (I<sub>DMAX</sub>) at the same time – with significant improvement over the state-of-the-art reports[7], [8], [12], [14], [15].

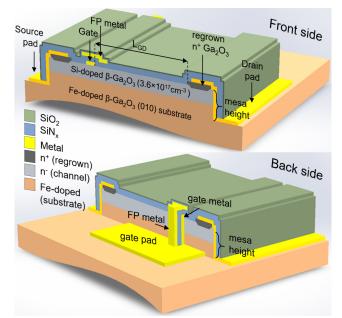


Fig. 1. 3D cross-section schematic of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFET showing the FP design. The bottom figure shows the gate FP metal is electrically connected to the gate pad outside the mesa.

## II. DEVICE GROWTH AND FABRICATION

Growth of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel (230 nm thick Si-doped ~3.6×10<sup>17</sup> cm<sup>-3</sup>) on a Fe-doped (010) bulk substrate was performed by using Agnitron Technology's Agilis 700 MOVPE reactor with TEGa, O<sub>2</sub>, and silane (SiH<sub>4</sub>) as precursors and argon as carrier gas. The 10×15 mm<sup>2</sup> (010)

bulk substrate (Novel Crystal Technology, Japan) was cleaned using HF for 30 mins prior to epilayer growth. SF<sub>6</sub>/Ar ICP-RIE dry etching was utilized for mesa and contact region recessing. The mesa etching was intentionally extended deeper into the substrate, and the total mesa etch height was measured to be ~ 500 nm. The device mesa isolation and the source/drain MOVPE-regrown ohmic contacts fabrication details can be found elsewhere [16]–[20]. Ti/Au/Ni (20 nm/100 nm/30 nm) was evaporated on the regrown n+ contact regions followed by a 450 °C anneal in N<sub>2</sub> for 1.5 mins. For the Schottky gate, Ni/Au/Ni (30 nm/100 nm/30 nm) metal stack was evaporated to complete the MESFET structure.

The gate field plate design involved a sandwiched dielectric structure as shown in Figure 1. A 170 nm thick  $SiN_x$  film was sandwiched between the gate metal and the FP metal (evaporated Ti (10 nm)/Au (150 nm) /Ni (50 nm)) using sequential metal evaporation and PECVD  $SiN_x$  deposition steps. The FP metal was shorted to the gate pad placed away from the device mesa (in the third dimension shown in Figure 1). This FP design avoids dry etching plasma-related damage in the active region. The field plate extension (L<sub>FP</sub>) was 3.2 and 3.5 µm for devices with gate-to-drain length (L<sub>GD</sub>) of 35 and 45 µm. The device mesa was fully passivated using a (50 nm)  $SiN_x/(50 nm) SiO_2$  bilayer passivation.

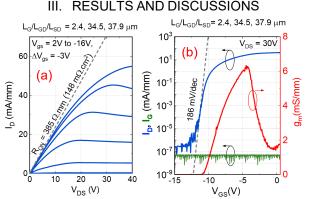


Fig. 2. (a) Output and (b) transfer curves for the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFETs with L<sub>GD</sub> = 34.5  $\mu$ m.

From Hall measurement, the channel charge and mobility were measured to be 5.7×10<sup>12</sup> cm<sup>-2</sup> and 95 cm<sup>2</sup>/Vs respectively  $(\mathbf{R}_{sh,ch} = 11.7 \text{ k}\Omega/\Box)$ . From transfer length measurements (TLM), the channel  $R_{sh,ch}$  was 11.5 k $\Omega/\Box$  and the total contact resistance to the channel was  $R_C = 1.4 \ \Omega$ .mm. The metal to regrown contact layer ( $R_{sh,n+} \sim 130 \ \Omega/\Box$ ) specific contact resistance was of the order ~  $10^{-6} \Omega \cdot \text{cm}^2$ . Fig. 2(a) & 2(b) show the DC output and transfer curves for a MESFET with dimensions  $L_{GS}/L_G/L_{GD} = 1.0/2.4/34.5 \ \mu m$ , measured using Keithley 4200 SCS. The reported device dimensions were verified by top-view SEM imaging. The maximum ON current  $(I_{DMAX})$  and ON-resistance  $(R_{ON})$  measured were ~56 mA/mm and 385  $\Omega$ .mm at a gate bias (V<sub>GS</sub>) of 2 V. The contact resistance to the channel,  $R_C$ , was a negligible part of the total device  $R_{ON}$ . The devices show sharp pinch-off at a  $V_{GS} = -13V$ and low reverse leakage  $(I_{ON}/I_{OFF} > 10^8)$  and negligible gate leakage). A maximum transconductance and sub-threshold swing of 6.2 mS/mm and 186 mV/dec was extracted respectively. The low gate and source-drain leakage indicated minimal surface and bulk-related leakage in these devices.

The breakdown measurements were performed with the wafer submerged in FC-40 Fluorinert dielectric liquid using a Keysight B1505 power device analyzer with N1268A UHV expander. Fig. 3(a) shows the three-terminal breakdown characteristics (at  $V_{GS} = -20$  V) of the MESFET device with  $L_{GD}$  of 34.5 um. A breakdown voltage  $V_{BR}$  (=  $V_{DS} - V_{GS}$ ) of 4415 V was measured. The device with  $L_{GD}$  of 44.5  $\mu m$ exhibited a V<sub>BR</sub> of 4567V (not shown). All the devices exhibited very low leakage of 10-100 nA/mm until catastrophic breakdown was observed. The measured reverse leakage currents in Figure 3(a) was limited by the noise floor of the N1268A UHV measurement set-up. Minimizing the reverse leakage was key to achieving the high V<sub>BR</sub> values and improved L<sub>GD</sub>-V<sub>BR</sub> linearity. Firstly, the long HF substrate cleaning before the epilayer growth helped in suppressing the parasitic channel at the epilaver/substrate interface that is believed to come from residual Si impurities from the substrate polishing or ambient exposure. As shown from C-V measurements in Figure 3(b), the channel charge profile showed sharp decay near the substrate, indicating the absence of any active parasitic channel. A backside depletion of the channel  $\sim 50$  nm from the substrate was observed which is consistent with the  $E_f$  pinning at the Fe trap level ( $E_C - E_{Fe} \sim$ 0.8 eV) in the substrate [21]. We hypothesize that the deeper mesa etching was important to eliminate any fringing leakage paths around the device mesa. The low reverse leakage and identical pinch-off voltage values from CV and FET transfer characteristics indicate that these two design steps were very effective in suppressing parasitic channel/charge conduction.

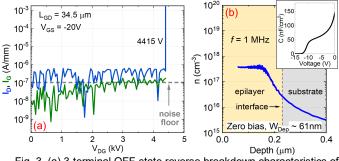


Fig. 3. (a) 3-terminal OFF-state reverse breakdown characteristics of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFET with L<sub>GD</sub> = 34.5  $\mu$ m. (b) channel charge profile extracted from C-V measurements (inset: capacitance-voltage profile).

Figure 4(a) shows the variation of VBR and IDMAX as a function of L<sub>GD</sub>. The breakdown voltage values exhibit a very linear increase up to  $L_{GD}$  = 10  $\mu m$  (V<sub>BR</sub> ~ 2.5 kV) and the devices were able to exhibit 2.5 MV/cm average breakdown field ( $V_{BR}/L_{GD}$ ). Beyond  $L_{GD}$  of 10 µm, the breakdown voltage starts to enter a saturation region and the VBR saturates at around 4.5 kV and does not increase much for  $L_{GD}$  of 35  $\mu m$  to 45 µm. From Sentaurus TCAD simulations, it was estimated that all the devices with  $L_{GD} \leq 10 \ \mu m$  had a punch-through (PT) field profile *i.e.* electric field does not go to zero at the drain contact, at their respective breakdown voltages whereas devices with  $L_{GD} > 10 \ \mu m$  had non-punchthrough (NPT) field profile at breakdown. It can also be seen that the NPT devices  $(L_{GD} > 10 \ \mu m)$  show larger device-to-device variation in  $V_{BR}$ compared to the PT devices ( $L_{GD} \le 10 \ \mu m$ ). Figure 4(b) shows the variation of IDMAX with LGD and shows almost a linear change. It is to be noticed that IDMAX values showed very little

device-to-device variation unlike the  $V_{BR}$  values. This observation indicates that although the contribution from bulk-related leakage paths cannot be completely ruled out, the process variation over the 10  $\times 15~mm^2$  sample could also lead to the spread in the  $V_{BR}$  values. The low device-to-device dispersion in ON currents also indicate that the epi-film conductivity (charge & mobility) is fairly uniform. From TCAD simulations (not shown here), the peak field accumulated in the FP edge in the SiN\_x layer and hence dielectric leakage/breakdown could also be limiting the  $V_{BR}$  and causing the saturation in  $V_{BR}$ .

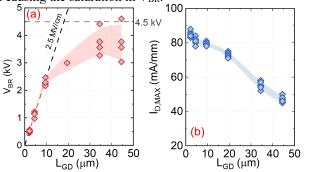


Fig. 4 (a)  $V_{\text{BR}}$  and (b)  $I_{\text{DMAX}}$  measured in our  $\beta\text{-}Ga_2O_3$  MESFETs as a function of  $L_{\text{GD}}$ . (shaded region shows device-to-device variation and is a guide to the eye).

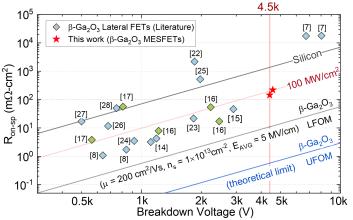


Fig. 5: Differential  $R_{on,sp}$ -V<sub>BR</sub> benchmark plot of our  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFET with the literature reports [8], [14], [15], [22]–[28].

The lateral figures of merit  $(V_{BR}^2/R_{on,sp})$  of these devices were estimated, where Ron,sp is RON normalized to the device active region ( $L_{SD}$  +2 $L_T$ ).  $L_T$  corresponds to the Transfer Length of the whole ohmic contact (metal to channel) including the regrown layer resistance  $(2L_T = 0.6 \mu m)$ extracted from patterned TLM patterns on the same wafer. An LFOM of 132 MW/cm<sup>2</sup> was estimated for the device with L<sub>GD</sub> = 34.5  $\mu$ m (V<sub>BR</sub> = 4.4 kV, R<sub>on,sp</sub> = 148 m  $\Omega$ ·cm<sup>2</sup> and L<sub>SD</sub>= 37.9 um). The device with  $L_{GD} = 45 \ \mu m$  exhibited a maximum LFOM of 96 MW/cm<sup>2</sup> ( $V_{BR} = 4.57 \text{ kV}$ ,  $R_{on,sp} = 219 \text{ m}\Omega \cdot \text{cm}^2$ and  $L_{SD} = 47.9 \ \mu m$ ). These values are benchmarked with the existing literarture reports on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral FETs. It can be seen that the devices reported here are the first > 4 kV class  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET devices to surpass the theoretical unipolar FOM of Silicon. Furthermore, our reported Ron,sp are the lowest for any β-Ga<sub>2</sub>O<sub>3</sub> FET exceeding a breakdown volatge of 4 kV. The V<sub>BR</sub>-L<sub>GD</sub> linearity is expected to be further improved by eliminating any parasitic bulk/surface leakage paths, passivation including extreme permittivity materials [29]. The

 $V_{BR}$ - $R_{on,sp}$  trade-off can be further improved by utilizing accumulation channels, improved channel/buffer stack engineering to improve channel mobility in conjunction with minimizing reverse leakage to prevent premature breakdown.

### IV. CONCLUSION

In summary, we demonstrate a 4.4 kV class  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral MESFET with an LFOM of 132 MW/cm<sup>2</sup> and ON current of 56 mA/mm – the first > 4 kV-class  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistor to surpass theoretical UFOM of Silicon. This demonstration shows great promise for MOVPE-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs in the low to medium voltage power-device applications.

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