4-Bit Ripple Carry Adder of Two-Phase Clocked Adiabatic Static CMOS Logic: A Comparison with Static CMOS

Nazrul Anuar
Graduate School of Engineering
Gifu University, 1-1 Yanagido,
Gifu-shi, Gifu Japan 501-1193
Email: n3814101@edu.gifu-u.ac.jp

Yasuhiro Takahashi
Faculty of Engineering
Gifu University, Japan 501-1193
Email: yasut@gifu-u.ac.jp

Toshikazu Sekine
Faculty of Engineering
Gifu University, Japan 501-1193
Email: sekine@gifu-u.ac.jp

***Abstract*—This paper demonstrates the low-energy operation of a two-phase clocked adiabatic static CMOS logic (2PASCL) on the basis of the results obtained in the simulation of a 4-bit ripple-carry adder (RCA) employing 2PASCL circuit technology. Energy dissipation in the 2PASCL RCA is 71.3% lesser than that in a static CMOS RCA at transition frequencies of 10-100 MHz.**

I. Introduction

Recently, clock and logic speeds have been increased for enhancing the performance of mobile and wireless devices; hence, it is important to design integrated circuits (ICs) that help achieve high energy efficiency. The power consumption in digital circuits, which mostly use complementary metal-oxide-semiconductor (CMOS) devices, is proportional to the square of the power supply voltage; therefore, voltage scaling is one of the important methods used to reduce power consumption. To achieve a high transistor drive current and thus improve the circuit performance, the transistor threshold voltage must be scaled down in proportion to the supply voltage. However, scaling down of the transistor threshold voltage, V_t results in a substantial increase in the subthreshold leakage current [1].

In recent years, adiabatic computing has been applied to low-power systems, and several adiabatic logic families have been proposed for low power logic applications [2]–[10]. The energy dissipated in adiabatic circuits is considerably lesser than that in static CMOS circuits; hence, adiabatic circuits are promising candidates for low-power circuits that can be operated in the frequency range in which signals are digitally processed. However, diode-based logic families have several disadvantages such as low output amplitude and power dissipation across the diodes in the charging path.

In this study, we compare the power consumption in a two-phase clocked adiabatic static CMOS logic (2PASCL) circuit [7] and a conventional CMOS circuit. We simulate a simple logic circuit, an inverter and a 4-bit ripple-carry adder (RCA) using 2PASCL and CMOS circuit technologies. We choose RCA as it has a longer propagation path than other do adders.

A novel method for reducing energy dissipation in a 2PASCL involves; the design of a charging path without diodes. In this case, during charging, current flows only through the transistor. Thus, a 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through the diode and the transistor. With the aforementioned 2PASCL circuit, we can achieve high amplitude and, reduce energy dissipation. In addition, to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

The rest of this paper is divided into five sections. Section II describes the differences between CMOS and adiabatic logic circuits. In Section III, the structure and operation of a 2PASCL circuit are explained. Section IV describes the simulation of a 2PASCL inverter and an RCA and a comparison of the energy dissipation in 2PASCL and CMOS circuits. Section V discusses the advantages and disadvantages of 2PASCL and Section VI includes concluding remarks.

II. CMOS Circuits vs. Adiabatic Logic Circuits

A. CMOS Circuits

Power dissipation in conventional CMOS circuits primarily occurs during device switching. As shown in Fig. 1, both pMOS and nMOS transistors can be modeled by including an ideal switch in series with a resistor in order to represent the effective channel resistance of the switch and the interconnect resistance. The pull-up and pull-down networks are connected to the node capacitance C_L, which is referred to as the load capacitance in this paper.

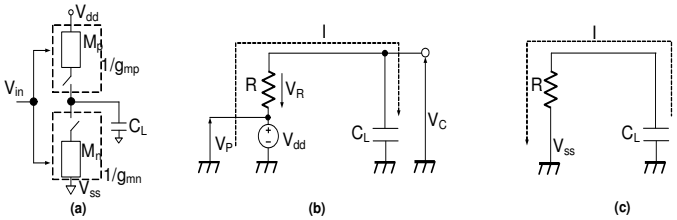

Fig. 1. (a) A model of CMOS showing ideal switch in series with resistor. (b) Charging activity. (c) Discharging activity.

When the logic level in the system is "1," there is a sudden flow of current through R. $Q = C_L V_{dd}$ is the charge supplied by the positive power supply rail for charging C_L to the level of V_{dd}. Hence, the energy drawn from the power supply is $Q \cdot V_{dd} = C_L V_{dd}^2$ [3]. By assuming that the energy drawn from the power supply is equal to that supplied to C_L, the energy stored in C_L is stated to be one-half the supplied energy, i.e., $E_{stored} = (\frac{1}{2}) C_L V_{dd}^2$. The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is $E_{charge} + E_{discharge} = C_L V_{dd}^2$.

From the aforementioned equation, it is apparent that energy consumption in a conventional CMOS circuit can be reduced by reducing V_{dd} and/or C_L. By decreasing the switching activity in the circuit, the power consumption $(P = \frac{dE}{dt})$ can also be proportionally suppressed.

B. Adiabatic Logic Circuits

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word "adiabatic" (Greek *adiabatos*, which means impassable) indicates a state change that occurs without loss or gain of heat. During adiabatic switching, all the nodes are charge/discharge at a constant current to minimize energy dissipation. This is accomplished by using AC power supplies to charge the circuit during specific adiabatic phases and subsequently discharge the circuit to recover the supplied charge.

The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. Figure 2 shows the manner in which energy is dissipated during a switching transition in adiabatic logic circuits. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the used of a time-varying voltage source instead of a fixed voltage supply.

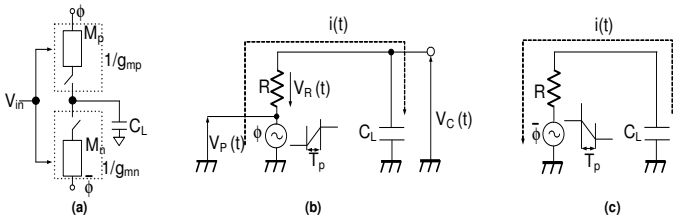

Fig. 2. (a) Model of adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks. (b) Charging activity. (c) Discharging activity.

The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfer over the entire time available. Hence, if $\hat{I}$ is considered as the average of the current flowing to C_L, the overall energy dissipated during the transition phase can be reduced in proportion to

$$\hat{I}^2 R T_p = \left(\frac{C_L V_{dd}}{T_p}\right)^2 R T_p = \left(\frac{R C_L}{T_p}\right) C_L V_{dd}^2. \qquad (1)$$

Theoretically, during adiabatic charging, when T_p, the time for the driving voltage ϕ to change from 0 V to V_{dd} is long, energy dissipation is nearly zero.

When $\overline{\phi}$ changes from HIGH to LOW in the pull-down network, discharging via the nMOS transistor occurs. From Eq. (1), it is apparent that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it during subsequent computations. Systems based on the abovementioned theory of charge recovery are not necessarily reversible.

III. 2PASCL

Figure 3 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [7]. A two-diode circuit is used, where one diode is placed between the output node and the power clock, and the other diode is adjacent to the nMOS logic circuit and connected to another power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches.

The proposed system uses a two-phase clocking split-level sinusoidal power supply, wherein ϕ and $\overline{\phi}$ replace V_{dd} and V_{ss}, respectively. One clock is in phase and the other is inverted. The voltage level of ϕ exceeds that of $\overline{\phi}$ by a factor of $V_{dd}/2$. By using these two split-level sinusoidal waveforms, the peak-to-peak voltage of each being 0.9 V, the voltage difference between the current-carrying electrodes can be minimized, and consequently power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to ϕ and $\overline{\phi}$ respectively.

Since the criteria for maintaining thermal equilibrium, in which the voltage between the current-carrying electrodes is zero when the transistors are in the ON state [4] are satisfied, the energy accumulated in C_L is not dissipated. Results of the simulation performed with a simulation program with the integrated circuit emphasis (SPICE) circuit simulator reveal that adiabatic circuits powered by the split-level sinusoidal consume less energy than does a trapezoidal clock power supply, even if the rise and fall times of the trapezoidal waveforms are set to their maximum values. Moreover, sinusoidal waveforms can be generated with higher energy efficiency than trapezoidal waveforms [8].

The circuit operation is divided into two phases: *evaluation* and *hold*. In the *evaluation* phase, ϕ swings up and $\overline{\phi}$ swings down. On the other hand, in the *hold* phase, $\overline{\phi}$ swings up and ϕ swings down. Let us consider the inverter logic circuit demonstrated in Fig. 3. The operation of the 2PASCL inverter is explained as follows.

1) *Evaluation* phase:
   a) When the output node Y is LOW and the pMOS tree is turned ON, C_L is charged through the pMOS transistor, and hence, the output is in the HIGH state.

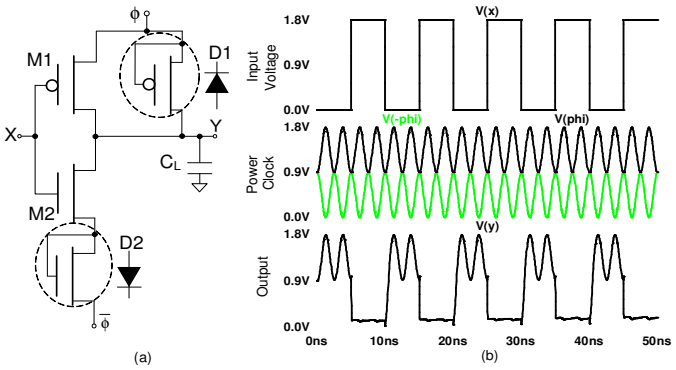

Fig. 3. (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency X=100 MHz, ϕ = $\overline{\phi}$ = 400 MHz.

b) When node Y is LOW and nMOS is ON, no transition occurs.
c) When the output node is HIGH and the pMOS is ON, no transition occurs.
d) When node Y is HIGH and the nMOS is ON, discharging via nMOS and D2 causes the logic state of the output to be "0" [10].

2) *Hold* phase:

a) When node Y is LOW and the nMOS is ON, no transition occurs.
b) At the point when the preliminary state of the output node is HIGH and the pMOS is ON, occurs discharging via D1 occurs.

The number of dynamic switching transition occuring during the operation of the 2PASCL circuit decreases as charging/discharging of the circuit nodes does not necessarily occur during every clock cycle. Because of this, node switching activities are suppressed to a significant extent and consequently, energy dissipation is also reduced. One of the advantages of the 2PASCL circuit is that it can be made to behave as a static logic circuit.

IV. Simulation Results and Discussion

A. Inverter Circuit

In this study, we investigate logic functions and energy dissipation of a simple logic gate, a 2PASCL inverter.

1) Simulation Conditions: The simulation in this study was performed using SPICE circuit simulator with a 0.18-μm, 1.8-V standard CMOS process. The width and length, W/L of nMOS and pMOS logic gates used was 0.6 μm/0.18 μm. A load capacitance (C_L) of 0.01 pF was connected to the output node Y. The frequency of the power supply clock was set to a value exactly four times the transition frequency. Simulations were carried out for the following purpose:

a) Logic functions: Evaluation of the 2PASCL inverter at a transition frequency of 100 MHz.

b) Energy dissipation: Comparison of energy dissipation per cycle between the 2PASCL and CMOS circuits at transition frequencies of 10, 20, 40, 80, and 100 MHz.

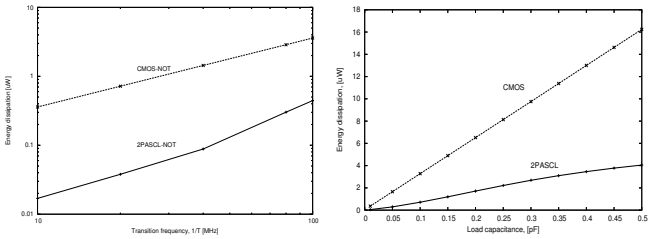

Fig. 4. Energy comparison of 2PASCL inverter vs. CMOS. at different transition frequencies (left), and at different load capacitance (right).

c) Load capacitance: Energy dissipation comparison in the 2PASCL and CMOS logic circuits for C_L values of 0.01, 0.02, 0.05, 0.1, 0.2, 0.3, 0.4, and 0.5 pF.

2) Simulation Results:

a) Output waveforms: The SPICE simulation results obtained for the 2PASCL inverter are shown in Fig. 3 (b). The top graph shows the input signals, which are CMOS-compatible rectangular pulses. The middle graph shows the driving voltage of the split-level sinusoidal supply clock, and the last graph shows the output waveform.

The energy dissipation is calculated by integrating the product of voltage and current; $E = \int_0^T (\sum_{i=1}^{n}(V_{pi} \times I_{pi}))\, dt$, where T is the period of the primary input signal; V_p, is the power supply voltage; I_p, the power supply current; and n, the number of power supply [10]. The energy obtained in joules is then converted to watts by multiplying it with the input frequency.

b) Comparison of energy dissipation: The comparison graph shown in Fig. 4 (left) reveals that with the 2PASCL inverter, up to 97% of the power dissipated from the CMOS inverter can be saved. Previous results [7] also show that the 2PASCL inverter offers the lowest energy dissipation among all other adiabatic inverter logic circuits.

c) Energy dissipation at different value of C_L: The simulation results show that energy dissipation in the 2PASCL inverter is significantly lower than that in CMOS circuit when C_L is 0.01-0.5 pF, as shown in Fig. 4 (right).

B. 4-Bit RCA

1) Simulation Conditions: For the next energy dissipation evaluation, a 2PASCL-based full adder (FA) is simulated. As shown in Fig. 7 (left), the FA consists of XOR and NAND gates. Our proposed schematics are as shown in Fig. 5 and Fig. 6.

To verify the practical applicability of the proposed 2PASCL circuit, we design and simulate a 4-bit (RCA) as illustrated in Fig. 7 (right). To enhance the accuracy of performance evaluation, we simulate the frequency characteristics of power consumption for the RCA of the 2PASCL circuit and compare the results with those obtained for the CMOS RCA circuit. We record the energy dissipation values at the same time period for both these circuits.

2) Simulation Results: We also confirm the functionality of the 4-bit 2PASCL RCA circuits. The results (Fig. 8) show that lesser energy dissipation occurs in the 2PASCL circuit with the split level sinusoidal clocking voltage than in the

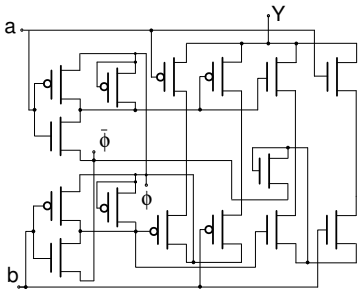

Fig. 5. Schematic for XOR logic of 2PASCL.

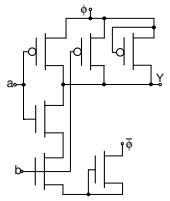

Fig. 6. Schematic for NAND logic of 2PASCL.

conventional static CMOS RCA. Further, it is apparent that energy dissipation is very less in the 2PASCL RCA when the simulated transition frequency is 10-100 MHz as shown in Fig. 9.

V. Discussion

While the 2PASCL circuit has advantages such as low power dissipation and high fan out, its main disadvantage is floating outputs, which are attributed to the alternate hold phases that exist during the circuit operation. Furthermore, there is a risk of current leakage (although small) as the gates are slowly switched ON. These problems will be addressed in our future research. The configuration of the two complementary low-power split-level sinusoidal power supply clocks is not discussed in this paper. The design of the power supply circuit will be proposed in a future study.

VI. Conclusion

This paper describes the simulation of a 4-bit 2PASCL (RCA) and its comparison with a CMOS RCA on the basis of adiabatic charging and energy recovery. The simulation results show that power consumption in the 2PASCL RCA considerably lesser than that in a CMOS RCA. For instance, when the input frequency is 10-100 MHz, the 2PASCL RCA dissipates only 28.7% of the energy dissipated by a static CMOS RCA. Further, the energy dissipated by a 2PASCL inverter remains low when the load capacitance is increased. Comparison of the present results with those obtained for the simulation of 2PASCL circuit with the other logic gates such as inverter chains, NOR gates, and flip flops reveals that the proposed adiabatic logic circuits is advantageous flor ultra low-energy computing applications.

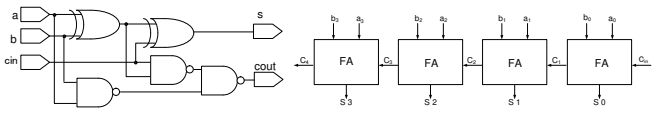

Fig. 7. Full Adder (FA) (left) and 4-bit Ripple Carry Adder (RCA) (right).

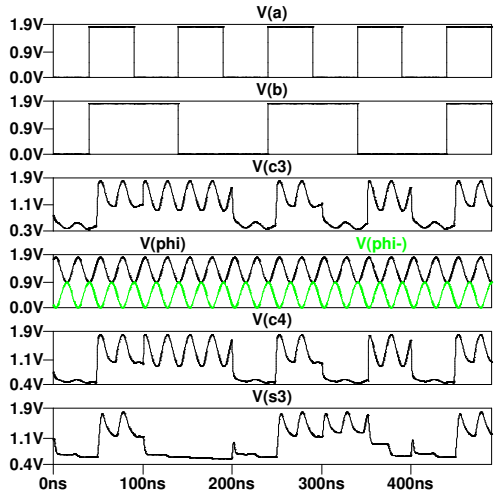

Fig. 8. Output waveforms for ripple carry adder of 2PASCL from the simulation result. ($a_0 = a_1 = a_2 = a_3$, $b_0 = b_1 = b_2 = b_3$).

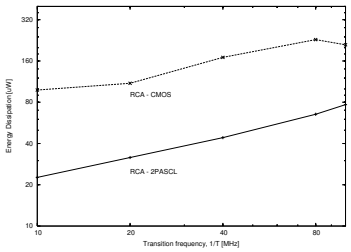

Fig. 9. Energy dissipation comparison of 2PASCL 4-bit RCA and CMOS 4-bit RCA at different transition frequency.

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