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5.8-kV Implantation-Free 4H-SiC BJT with Multiple-Shallow-Trench Junction Termination Extension

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***Abstract*—Implantation-free 4H-SiC BJTs with multiple-shallow-trench junction termination extension (ST-JTE) have been fabricated. The maximum current gain of 40 at a current density of 370 A/cm^2 is obtained for the device with active area of 0.065 mm^2. A maximum open-base breakdown voltage (BV) of 5.85 kV is measured, which is 93% of the theoretical breakdown voltage. A specific on-resistance (R_{ON}) of 28 mΩ.cm^2 was obtained.**

***Index Terms*—4H-SiC, multiple-shallow-trench JTE, implantation-free, high-voltage BJT.**

I. Introduction

SILICON carbide bipolar junction transistors (BJTs) in the 3–7-kV range with low on-resistance (R_{ON}) are very attractive devices for industrial applications due to their low loss and fast switching speed. Besides, gaining lower on-resistance results in lower loss which is as important as improving the breakdown voltage to its theoretical value. Several termination techniques have been developed and optimized to approach the ideal breakdown voltage and improve the termination efficiency [1-12]. Among them, implantation-free devices with low R_{ON} have the advantage of preventing life-time-killing defects and current degradation caused by ion implantation [10]. These devices are based on etched junction termination extensions (JTEs) in which the remaining dose of the JTEs is controlled by the etching depth. Table I summarized the recent results reported for SiC BJTs.

In this letter, an implantation-free 4H-SiC BJT with multiple-shallow-trench JTE (ST-JTE) termination is demonstrated. The effect of material and etching uncertainties is investigated by numerical simulation and compared with experimental data. The fabricated ST- JTE device has three advantages. First, it is completely free of ion implantation and the following high temperature activation annealing to avoid any further defects caused by it. Second, compared with multi-implanted or graded-etched JTEs, the trench structures are

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TABLE I. PERFORMANCE COMPARISON BETWEEN THE ST-JTE AND RECENT SIC POWER BJTS.

Ref. / Size*	BV (kV)	R_{ON} (mΩ.cm^2)	Gain	Termination Efficiency (%)
[3] / S	3.2	28	28	40
[4] / S	6	28	3	--
[5] / S	23.5	321	63	78
[6] / S	9.2	49	7	--
[7] / L	1.8	4.4	40	--
[8] / L	2.3	4.5	35	85
[9] / L	1.8	2.8	117	--
[10] / S	2.8	4	55	75
[10] / L		6.8	52	
[11] / L	10.5	110	75	91
[12] / L	2.7	4	132	> 90
This work / S	5.85	28	40	93

* "S" FOR SMALL-AREA (< 0.5 MM^2) LOW-CURRENT (I < 1 A) AND "L" FOR LARGE-AREA (> 2.5 MM^2) HIGH-CURRENT (I > 5 A) BJTS.

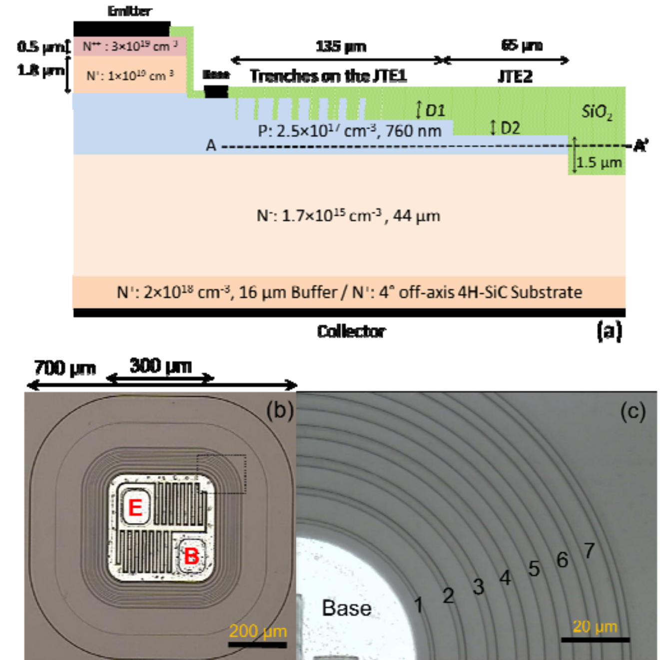

Fig. 1. (a) Schematic cross-sectional view of the 4H-SiC with trenched JTE (ST-JTE), (b) optical microscopic image of the ST-JTE BJT with seven trenches, and (c) magnified optical microscopic image of the trench structures. The trenches are formed on the first JTE with the depth of 300 nm.

simultaneously formed by the first JTE with no extra mask, which makes it a simpler and cheaper structure to fabricate; meanwhile prevents any further misalignment issue. Third, the maximum BV of 5.85 kV is obtained which is 93% of the theoretical value [13]. Higher termination efficiency is yet achievable by increasing the number of trenches and squeezing the trenches which requires lithography with higher resolution.

II. Device Structure and Fabrication

The cross-sectional schematic view of the ST-JTE is shown in Fig. 1(a). The total area of the device is 0.49 mm^2. The width of the emitter and base fingers are 10 and 4 µm, respectively (see Fig. 1(b)). Trench structures gradually decreasing in dimensions have been formed on the first JTE (see Fig. 1(c)). Depending on the design, the depth of the trenches can be controlled by the etching of the other layers with no additional mask. Considering the lithography limit to 1 µm, the number, width, and spacing of the trenches are also optimized to reach the optimized electric field spreading. The optimized result is obtained for the ST-JTE with seven trenches as deep as 300 nm; whereas the spacing gradually increases from 1 µm to 7 µm and the width is gradually decreasing from 9 µm to 3 µm.

A 100-mm 4H-SiC n^+-substrate with five different epilayers on top is used (see Fig. 1(a)). A 2.5-µm layer of SiO_2 is deposited and patterned as the hard mask. Then, inductively coupled plasma (ICP) deep etching is used to form the emitter and mesa. Afterward, reactive ion etching (RIE) is used to accurately form the JTEs with the depth of D_1 = 300 nm and D_2 = 160 nm, respectively. Trench structures are simultaneously formed by the etching step of the first JTE with the same depth. As a result, the etching uniformity of ±5% is achieved, which significantly improved the yield of the wafer. Also, extra etchings are performed to investigate the dose dependency of the breakdown voltage. Subsequently, sacrificial oxidation was done in O_2 for 1 h. After removal of the thermally grown oxide, 50 nm SiO_2 was deposited by PECVD and annealed at 1100 °C in N_2O environment for 3 h as the passivation layer. A Ni layer with a thickness of 140-nm was deposited and patterned on the emitter and back-side collector. Contacts were annealed in Ar at 950 °C for 1 min. A 110-nm Ni/Ti/Al metal stack with the thickness 0.1/0.15/0.85 was deposited and patterned on the base layer and annealed in N_2 at 815 °C for 2 min to form the p-contacts [14]. To improve the current spreading through the contacts, 500 nm of Al was deposited and formed on the n- and p-contacts. Using TLM structures, a contact resistivity of 1.4×10^{-5} $\Omega.cm^2$ and 1.5×10^{-4} $\Omega.cm^2$ are measured for the emitter and base contact, respectively. Subsequently, a thick oxide was deposited as the insulator layer and the contact windows were opened. Finally, 2.5-µm Al was sputtered and patterned to form the emitter and base electrodes.

III. Results and Discussion

The I_C–V_C characteristic of the ST-JTE device in forward and blocking mode is shown in Fig. 2. A maximum current gain of 40 at I_C = 0.24 A (J_C = 370 A/cm^2) and V_{CE} = 4.3 V at I_C = 0.1 A are achieved. The current flow in the thick collector layer is analyzed by 2-D simulation and the estimated equivalent active area of the device is 0.065 mm^2. Therefore, the specific on-resistance of R_{ON} = 28 mΩ.cm^2 was calculated considering the current spreading effect. It should be noted that the on-resistance of the device is expected to be higher when scaled up to large-area since the small-area BJT benefits from significant current spreading in the collector layer. The forward voltage drop at J_C = 100 A/cm^2 is 2.6 V. The maximum open-base breakdown voltage of 5850 V and 4650 V are measured for the ST-JTE and double-JTE, respectively. These correspond to 93% and 75% of the theoretical value, respectively, which prove the efficiency of the ST-JTE structure. Therefore, less termination area is required for the ST-JTE device leading to reduction of total device cost.

The remaining dose of the dopants in the JTEs is controlled by the etching process. Fig. 3 illustrates the BV versus the p-layer dose for ST-JTE compare with conventional double-JTE. It is apparent that the ST-JTE BJTs have much less sensitivity to the etching variation. Also, simulation results show that higher number of trenches results in wider stable dose range which will result in higher yield of the wafer. The maximum breakdown voltage variation (ΔBV) of 700 V and1700 V is measured for the ST-JTE and conventional double-JTE for

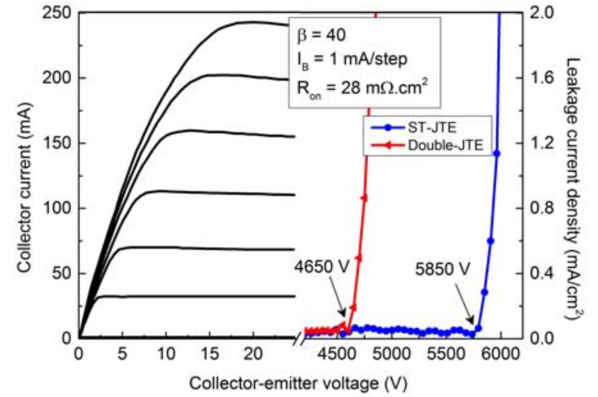

Fig. 2. *I-V* forward characteristics of the ST-JTE device and comparison of the breakdown voltages of the ST-JTE and conventional double-JTE device.

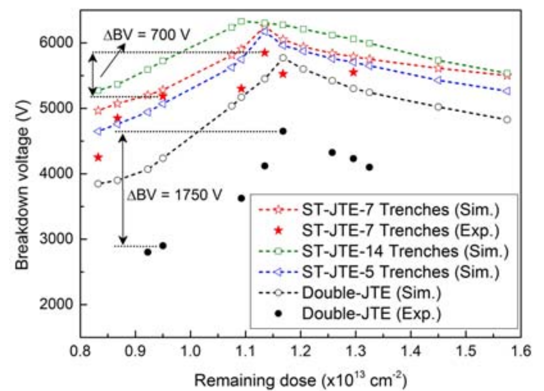

Fig. 3. Experimental and simulated breakdown voltages of the ST-JTE and double-JTE devices as a function of the remaining dose of

the JTE1. The dose range for the ST-JTE structures are much wider than that of the double-JTE.

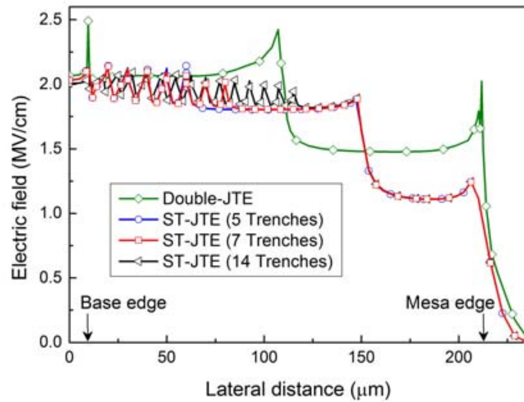

Fig. 4. Simulated electric field distribution along the device at the cutline of AA′ for the applied reverse voltage of 6 kV.

20% variation in the remaining dose of the p- layer, respectively. Among the 26 measured ST-JTE devices, 80% blocks more than 4.5 kV and the yield of high blocking ST-JTE BJTs (> 5 kV) is about 55%.

The influence of charges at the oxide/SiC interface on the breakdown voltage of SiC devices has been reported [15]. The amount of charges in a certain area varies by forming the trenches. Therefore, taking the presence of these charges into account, the optimum effective dose of 1.15×10^{13} cm^{-3} is found for the first JTE by simulation. Fig. 4 compares the simulated electric field for the ST-JTEs with different number of trenches with conventional double-JTE structure at their optimum dose for the applied reverse voltage of 6 kV. It is apparent that the electric field is shared by the multiple trenches leading to alleviated peaks in the electric field. Therefore, these trenches prevent the field crowding and shield the high field at the JTE and mesa corners. Thus the electric field in the ST-JTE is more uniform which results in higher efficiency of the termination technique. Also, it is apparent that higher number of trenches with smaller widths results in better electric field distribution. Considering the lithography limit to 1 µm, the optimized result is obtained for the ST-JTE with seven trenches. The smallest dimension required for realizing the ST-JTE with 14 trenches is 0.5 µm compare with 1 µm for the device with seven trenches. One can expect that a finer photolithography improves the termination efficiency and sensitivity to the etching and doping variation (remaining dose) of the p-layer. However, it is recommended not to design too narrow trenches with dense spacings.

The performance of the ST-JTE BJT compared with that of the best reported BJTs are summarized in Table I. The maximum open-base BV of 5850 V and R_{ON} of 28 mΩ.cm^2 are obtained, respectively, which is very close to the 4H-SiC unipolar limit. The termination efficiency of the ST-JTE device is among the highest values reported to date.

IV. Conclusion

An implantation-free 4H-SiC BJT with multiple-shallow-trench JTE structure (ST-JTE) is presented. A specific on-resistance (R_{ON}) of 28 mΩ.cm^2 is obtained for the device with active area of 0.065 mm^2. A maximum open-base breakdown voltage (BV) of 5.85 kV is measured which corresponds to 93% of the ideal value. No extra mask is required to form these trenches which result in a simpler process without any further misalignment issue.

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