500 °C Bipolar Integrated OR/NOR Gate in 4H-SiC

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***Abstract*— Successful operation of low-voltage 4H-SiC n-p-n bipolar transistors and digital integrated circuits based on emitter coupled logic is reported from −40 °C to 500 °C. Nonmonotonous temperature dependence (previously predicted by simulations but now measured) was observed for the transistor current gain; in the range −40 °C – 300 °C it decreased when the temperature increased, while it increased in the range 300 °C–500 °C. Stable noise margins of ∼1 V were measured for a 2-input OR/NOR gate operated on −15 V supply voltage from 0 °C to 500 °C for both OR and NOR output.**

***Index Terms*— Bipolar junction transistor (BJT), emitter coupled logic (ECL), high-temperature integrated circuits (ICs), OR/NOR gate, silicon carbide (SiC).**

I. Introduction

THANKS to its wide bandgap [1] silicon carbide (SiC) provides significant advantages for high-temperature applications, which can make the difference in many important applications [2]. Complementary metal–oxide–semiconductor (CMOS) digital gates were first demonstrated up to 300 °C in 6H-SiC [3], and more recently up to 400 °C in 4H-SiC together with analog circuits [4]. JFET-based digital gates in 6H-SiC have recently reported operation up to 550 °C [5]. The performance of this JFET-based inverter, however, degrades when the temperature rises; its high noise margin (NM) is noticeably reduced at higher temperatures. High-temperature bipolar ICs have been also demonstrated in 4H-SiC. Digital ICs were first reported based on transistor–transistor logic up to 355 °C [6], and more recently based on emitter coupled logic (ECL) [7]. In comparison with the aforementioned JFET inverter, the NMs reported for the ECL-based OR/NOR gates are stable and ∼1 V from 27 °C to 300 °C [7].

This letter reports the successful operation from −40 °C to 500 °C of an integrated OR/NOR gate, which uses the same design reported in [7], and bipolar transistors with improved high temperature performance and current gain (β) increasing >300 °C.

II. Fabrication

In this letter, a six-layer epistructure ($n^{++}/n^{+}/p/n^{-}/n^{+}/p$) was grown in a continuous run on a 2-in n-type 4H-SiC wafer.

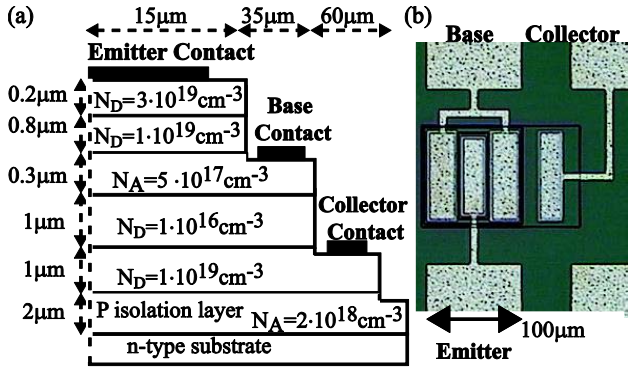

Fig. 1. Fabricated n-p-n transistor. (a) Cross-sectional view. (b) Optical image.

Cross-sectional view and optical image of the fabricated SiC n-p-n transistors are shown in Fig. 1(a) and (b), respectively.

The fabrication process started by forming emitter, base, and collector mesas by means of reactive ion etching. After sacrificial oxidation in N_2O ambient, surface passivation was performed with 50-nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 followed by postoxide deposition anneal in N_2O at 1250 °C [8]. Two different metal stacks (Ni and Ni/Ti/Al for n- and p-type, respectively) were deposited, patterned, and annealed to form ohmic contacts to emitter, base, and collector layer (more details can be found in [7] and [8]). A 1-μm-thick PECVD SiO_2 layer was deposited as intermediate dielectric, whereas a stack of Ti/TiW/Al (30/70/1000 nm) was sputter deposited and patterned to realize all interconnects.

The fabricated OR/NOR gate, whose optical image is shown in Fig. 2, consists of 10 n-p-n transistors and 11 integrated resistors, with a total area of ∼1 mm^2. The isolated n-p-n [Fig. 1(b)] is 162.5 μm × 105 μm with emitter area of 30 μm × 90 μm. The integrated resistors have been realized in the emitter or base layer, according to designed resistance size [7].

III. Results and Discussion

Static characteristics of test devices and logic gates were measured by direct wafer probing using different hot chucks for the two temperature ranges −40 °C–27 °C and 27 °C–500 °C.

Sheet resistance of emitter, base, and high-doped collector layer was estimated by means of transfer length method measurement. At room temperature, the sheet resistance was measured to be 170 Ω/square, 84 kΩ/square, and 300 Ω/square in the emitter, base, and collector layer, respectively.

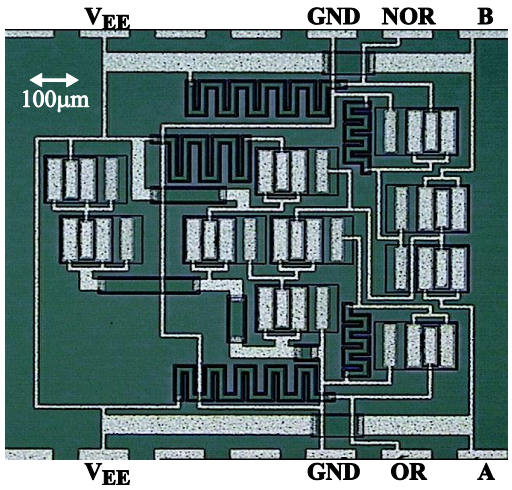

Fig. 2. Optical image of the fabricated 2-input ECL OR/NOR gate (1000 μm × 1117 μm).

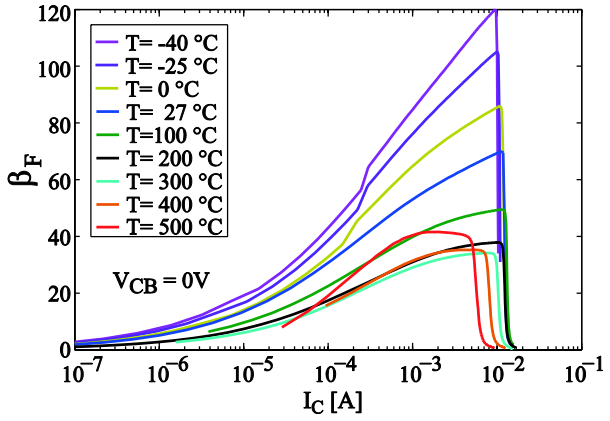

Fig. 3. Current gain plot measured with $V_{BC} = 0$ V at different temperatures.

A. Device Performance

Fig. 3 shows the forward current gain plot (β versus I_C) measured at $V_{BC} = 0$ V from −40 °C to 500 °C. At 27 °C the current gain (β) reaches its maximum value of 70 at $I_C = 11$ mA and abruptly drops for higher collector current because of high injection in the low doped collector and forward biasing of the base–collector junction. Device saturation is caused by the lateral flow of I_C in the heavily doped collector layer, which constitutes the major contribution to the collector resistance R_C [7]. At 27 °C, the collector resistance (extracted from I_C–V_{CE} characteristic at $V_{CE} = 2$ V) is measured as 300 Ω.

Temperature dependence of the collector resistance and current gain of the n-p-n transistor is shown in Fig. 4. For a fixed base–collector voltage ($V_{BC} = 0$ V) β first drops down from 120 to 34 when the temperature rises from −40 °C to 300 °C, and then increases again to 42 at 500 °C. This behavior can be attributed to two competing mechanisms that affect β when the temperature rises: reduction of the emitter injection efficiency due to increased ionization degree of base dopants and increase of carrier lifetime [9]–[11]. From the constant slope of β versus 1000/T, in the range −40 °C to 300 °C, we can calculate an effective activation energy for β of ∼46 meV. Physical device simulations, using an activation

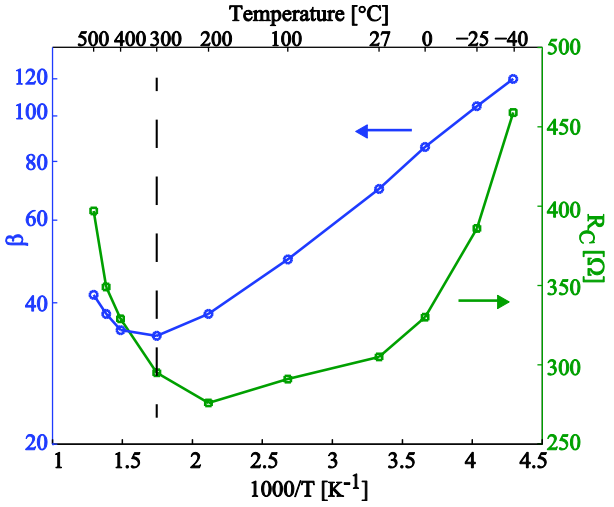

Fig. 4. Temperature dependence of the BJT current gain (at $V_{BC} = 0$ V) and collector resistance (extracted from the $I_C - V_{CE}$ characteristic at $V_{CE} = 2$ V).

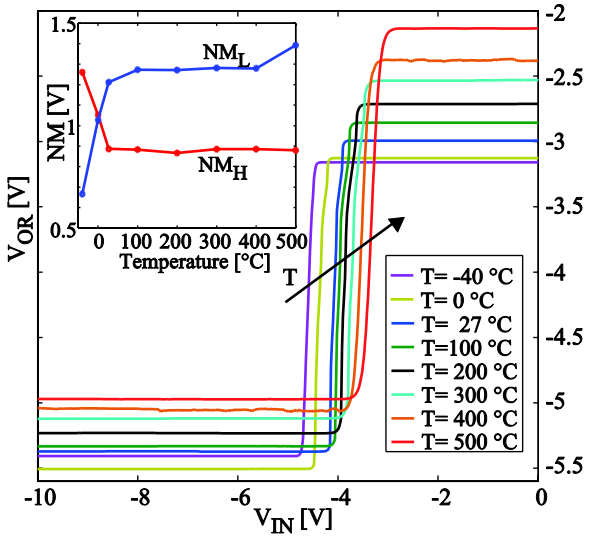

Fig. 5. Measured V_{IN}–V_{OR} characteristic at −40 °C, 0 °C, 27 °C, 100 °C, 200 °C, 300 °C, 400 °C, and 500 °C, and related NMs.

energy of 191 meV for Al dopants, yield an effective activation in close agreement to this. For higher temperature, the positive gain temperature coefficient and near to constant slope could be related to a power law dependence for the minority carrier lifetime. Compared with other available data and simulations [10], [11], our results extend the temperature range both to lower and higher temperatures and hence enable a reliable fitting. The nonmonotonous R_C temperature dependence is the result of two opposing phenomena that influence the sheet resistance of the heavily doped collector layer [7] when the temperature rises: increase of dopant ionization degree and reduction of majority carrier mobility.

B. Circuit Performance

The OR/NOR gate was tested with a supply voltage (V_{EE}) of −15 V by applying the input signal, swept between −10 to 0 V, at one input (A or B) leaving the other one open. Measured voltage transfer characteristics and related NMs at −40 °C, 0 °C, 27 °C, 100 °C, 200 °C, 300 °C, 400 °C, and 500 °C are shown in Figs. 5 and 6, for OR and NOR output,

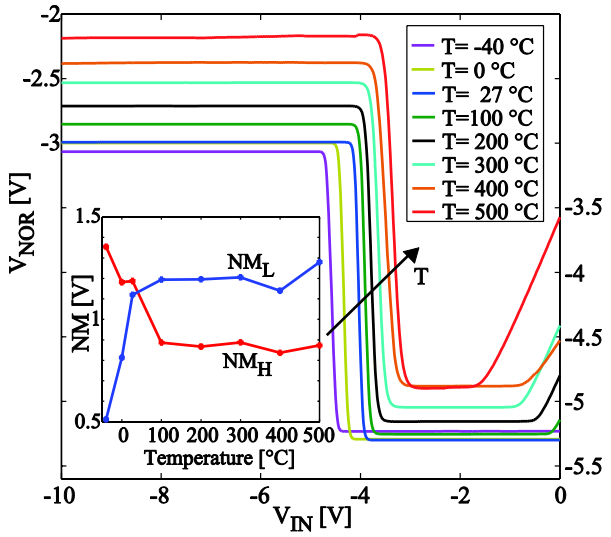

Fig. 6. Measured V_{IN}–V_{NOR} characteristic at −40 °C, 0 °C, 27 °C, 100 °C, 200 °C, 300 °C, 400 °C, and 500 °C, and related NMs.

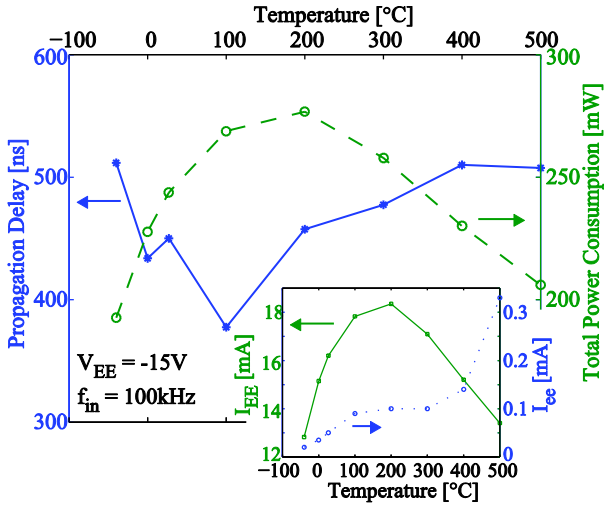

Fig. 7. Temperature dependence of average propagation delay (T_P), total power dissipation (P_D), and static and dynamic components of the current consumption (I_{EE} and I_{ee}, respectively) in the range −40 °C–500 °C.

respectively. Both OR and NOR measured high voltage levels, as well as the logic threshold, move toward positive voltage when the temperature increases, in agreement with previous reported results [7]. The low voltage levels, instead, show a nonmonotonous behavior when the temperature rises from −40 °C to 27 °C. OR and NOR NMs are stable and ∼1 V from 0 °C to 500 °C. At −40 °C instead, the low NM (NM_L) is ∼0.5 V whereas high NM (NM_H) is ∼1.3 V for both OR and NOR outputs.

Propagation delay (T_P) and total power consumption (P_D) at each temperature were estimated from switching measurements performed with $V_{EE} = -15$ V and an input signal having logic levels compatible with those of the output signals and frequency of 100 kHz. As shown in Fig. 7, both T_P and P_D exhibit a nonmonotonous temperature behavior since both of them are strongly affected by changes in resistor resistance and bipolar junction transistor (BJT) β. In fact, as confirmed by static and dynamic current consumption shown in the inset of Fig. 7, P_D is mainly determined by its static component, and this tracks changes in bias currents throughout the circuits. In the range −40 °C–500 °C $P_D \cdot T_P$ is ∼100 nJ, closely to what is reported for JFET-based SiC logic gates [12].

IV. Conclusion

The successful operation of BJTs and of an integrated bipolar OR/NOR gate has been demonstrated in 4H-SiC up to 500 °C. Thanks to the improved device performance, and the use of a temperature compensation network the NMs are stable and ∼1 V from 0 °C to 500 °C, and slightly degrade at lower temperatures; while the power-delay product per gate is ∼100 nJ in the whole temperature range. Furthermore, increased gain > 300 °C significantly extends the possible temperature range of operation. The reported IC technology is a promising candidate for high-temperature applications, although development of reliable high-temperature ohmic contacts and metallization system and interlayer dielectric is still an open challenge.

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