INSTITUTE OF PHYSICS PUBLISHING NANOTECHNOLOGY
Nanotechnology **16** (2005) 1058–1061 doi:10.1088/0957-4484/16/8/010

6 nm half-pitch lines and 0.04 μm^2 static random access memory patterns by nanoimprint lithography

Michael D Austin[1], **Wei Zhang**[1], **Haixiong Ge**[1], **D Wasserman, S A Lyon and Stephen Y Chou**[1]

Department of Electrical Engineering, Princeton University, Princeton, NJ 08544, USA

E-mail: chou@princeton.edu

Received 10 February 2005, in final form 18 March 2005
Published 12 May 2005
Online at stacks.iop.org/Nano/16/1058

Abstract
A key issue in nanoimprint lithography (NIL) is determining the ultimate pitch resolution achievable for various pattern shapes and their critical dimensional control. To this end, we demonstrated the fabrication of 6 nm half-pitch gratings and 0.04 μm^2 cell area SRAM metal interconnects with 20 nm line half-pitch in resist by NIL. The mould for the 6 nm half-pitch grating was fabricated by cleaving a GaAs/$Al_{0.7}Ga_{0.3}As$ superlattice grown on GaAs with molecular beam epitaxy, and selectively etching away the $Al_{0.7}Ga_{0.3}As$ layers in dilute hydrofluoric acid. The mould for the 0.04 μm^2 SRAM metal interconnects was fabricated in silicon dioxide using 35 kV electron beam lithography with polystyrene as a negative resist and a reactive ion etch with the resist as mask. Imprints from both moulds showed excellent fidelity and critical dimension control.

Advances in microelectronics and nanotechnology increasingly demand lithography to have a smaller pitch (the centre-to-centre distance between two features). Unlike the feature size, which can be further reduced after lithography by 'over-etching', the pitch is limited by the physics of a lithography method and is fixed once patterned. Today's lithography for semiconductor integrated circuits (ICs) manufacturing at the '90 nm node' has a pitch of 240 nm. How much further the pitch can be reduced without replacing photolithography is a hot topic for debate. The smallest pitch demonstrated by other forms of lithographies, such as electron beam lithography (EBL) [1–3], scanning probe lithography [4], extreme ultra-violet (EUV) [5], and ion beam [6], is ∼15 nm. However, these patterning techniques are too slow or too costly for manufacturing requirements, and the quality of the features degrades substantially with decreasing pitch.

Here, we report the fabrication of 6 nm half-pitch (HP) gratings in a polymer resist using nanoimprint lithography (NIL), a high-throughput and low-cost process, well suited for mass production. This pitch is, to the best of our knowledge, the smallest created by lithography using a mask. In addition, we demonstrate the fabrication of complex patterns for the metal interconnects of static random access memory (SRAM) cells of area 0.04 μm^2 and 20 nm HP.

Fundamentally different from conventional lithography, nanoimprint lithography (NIL) patterns nanostructures in a resist by physical deformation of the resist using a mould. NIL is immune to many factors that limit conventional photolithography resolution, such as diffraction, scattering and interference in the resist, backscattering from a substrate, and the developer chemistry. Due to these advantages, various 'printing' lithographies with a mould have been developed [7–9], and sub-10 nm feature size has been demonstrated [10–13].

To explore the limits of NIL pitch resolution, we used an unconventional method to create a NIL mould: a series of GaAs/$Al_{0.7}Ga_{0.3}As$ superlattices were grown on a GaAs substrate using molecular beam epitaxy (MBE) and the $Al_{0.7}Ga_{0.3}As$ was selectively etched away from a cleaved edge in a dilute solution of hydrofluoric acid (HF), creating a GaAs periodic grating [11, 14, 15]. The periodicity of the grown superlattices ranged from 80 nm down to 2 nm, although our scanning electron microscope (SEM) analysis could only

[1] Authors associated with the Nanostructure Laboratory.

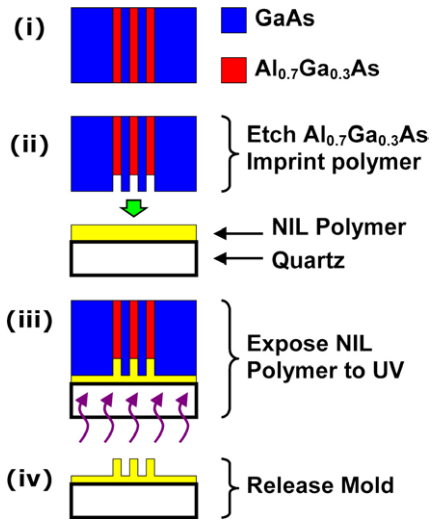

Figure 1. Schematic diagram of the UV curable nanoimprint lithography (UV-NIL) process. (i) A special NIL mould was made by selectively etching $Al_{0.7}Ga_{0.3}As$ from the cleaved edge of a GaAs/$Al_{0.7}Ga_{0.3}As$ superlattice grown by molecular beam epitaxy (MBE). (ii) A liquid resist film spun on a quartz substrate was imprinted by the mould. (iii) The resist was cured (polymerized) by back-face exposure to UV light. (iv) The mould was released from the substrate, leaving the resist patterned on the quartz substrate.
(This figure is in colour only in the electronic version)

confirm the presence of gratings on the mould with a HP of 4 nm or greater. The edge of the mould was pressed into a thin layer of photo-curable resist liquid spin-coated on a quartz substrate, and the resist was cured with UV light (figure 1). The imprints were performed with the UV-NIL operation mode of the NX-2000 tool and NXR-2010 resists from Nanonex Corporation.

Critical to achieving the high-quality imprints, and thereby improving on our previously published results [11] in both resolution and area, was the mould preparation and imprint process. Briefly: the GaAs sample was cleaved into 2 mm × 2 mm samples so that one side of the sample was free of damage from the cleave. The sample was then washed in acetone with ultrasonic agitation to remove dust particles and inspected under a microscope for defects. Mould samples with defect-free edges were then etched in HF:DI at 1:600 with ultrasonic agitation for 1 min, rinsed in DI, dried with N_2 gas, and stored individually in anhydrous ethanol. The samples were then put inside a glove-box with less than 1 ppm H_2O and O_2 content for surface treatment with 17 mM octanethiol solution for several (3–7) days, until ready for use. Before imprinting, the moulds were rinsed in pure ethanol, acetone, methanol, and finally isopropanol, dried with N_2 gas, and baked at 80 °C for 5 min. The quartz wafers were prepared by removing dust with a CO_2 'snow' cleaning system (Applied Surface Technologies), rinsed with acetone, methanol, isopropanol, dried with N_2 gas, baked at 80 °C for 5 min, and finally spin-coated with imprint resist.

Inspection with a SEM verified that gratings down to 6 nm HP were successfully imprinted into the resist (figure 2). Although not the narrowest lines so far imprinted [12], these lines were densely packed and the GaAs grating mould ensured that the linewidth and half-pitch were constricted to 6 nm. The imprinted gratings extended several hundreds of microns

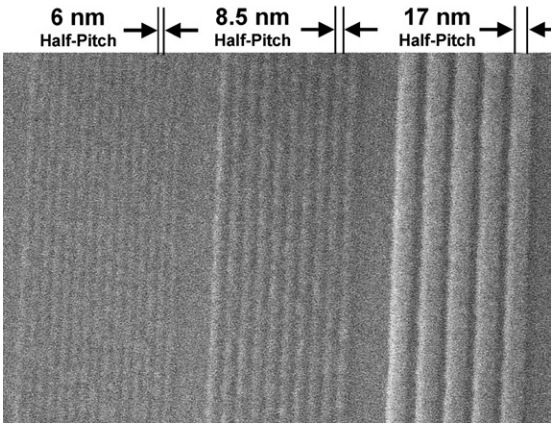

Figure 2. SEM image of polymer resist patterned with 6, 8.5, and 17 nm half-pitch gratings fabricated by imprinting with a cleaved GaAs MBE mould.

without defects. Considering that each monomer in the resist has a length of 1.4 nm, and the radius of gyration of the cured polymer chain is half the imprinted linewidth, there were on average nine monomers across the 6 nm resist line, demonstrating that polymerization of the resist can occur even under extremely restricted spatial dimensions.

Currently, our limited SEM resolution and thermal damage to the polymer during inspection prevented us from observing any gratings with a HP less than 6 nm. However, it may be possible to observe sub-6 nm HP with improvements in microscopy and the minimization of resist melting. Furthermore, improved SEM image contrast could be obtained by increasing the sub-6 nm half-pitch grating mould depth—though doing this without mechanically damaging the mould and/or polymer during separation would be challenging.

Previously [11], we reported the fabrication of 5 nm features with NIL. However, these features were sparsely patterned on the mould, and critical dimension (CD) control was not investigated. Here we explore the smallest pitch of complex patterns typically used by the semiconductor industry and their CD control during NIL. To this end, we tested NIL in the patterning of the metal interconnects of SRAM cells of 0.04 μm^2 area and 20 nm line HP.

Fabrication of the NIL mould for the SRAM metal interconnects is a challenge, since the complex shape of these patterns requires the use of conventional programmable nanolithography, and the pitch of these patterns is close to the limits of current EBL capabilities. To produce a NIL mould with 20 nm HP and excellent CD control, we used polystyrene (PS) as a negative EBL resist [16] and then as an etch mask for RIE of the mould. PS was selected over (PMMA) poly(methyl methacrylate), a positive EBL resist commonly used for NIL mould fabrication [10, 11], as PMMA is a poor etch mask and requires further processing of pattern transfer to Cr with lift-off. We found that the proximity effect made dense EBL patterning with a PMMA lift-off step increasingly difficult without degrading the line-width control.

A thin film of PS was prepared on a silicon substrate with 200 nm thermally grown silicon dioxide. The PS of 2000 M_w molecular weight and polydispersity index of 1.06 was dissolved in chlorobenzene at 1% by weight and spun onto the

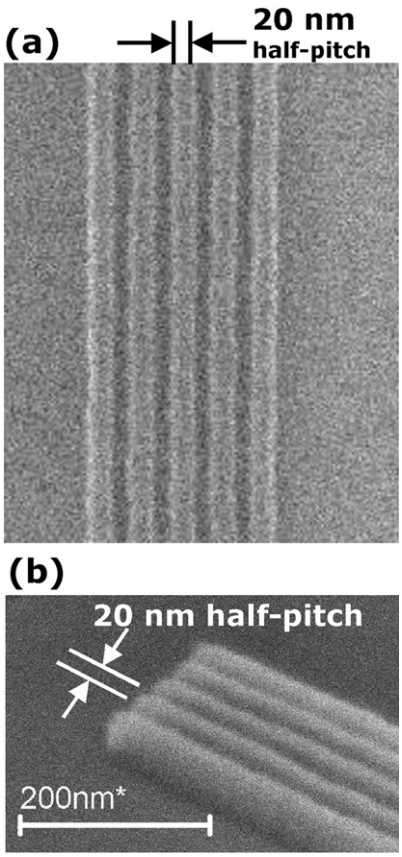

Figure 3. (a) Scanning electron microscope (SEM) image of 20 nm half-pitch polystyrene (PS) lines fabricated by 35 kV electron beam lithography (EBL) on a thermally grown silicon dioxide substrate. (b) SEM image of the 20 nm half-pitch lines shown in (a) after reactive ion etching (RIE) of the silicon dioxide substrate using the PS as an etch mask to fabricate a mould for nanoimprint lithography (NIL).

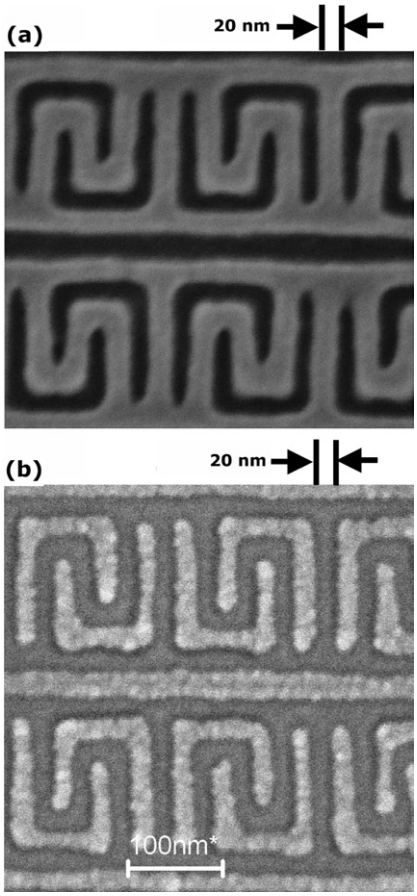

Figure 4. SEM images of (a) imprint resist with 0.04 μm^2 cell area SRAM metal interconnect patterns obtained by UV-NIL showing a line half-pitch of 20 nm; and (b) the Cr structures obtained by pattern transfer of the resist pattern shown in (a) with a Cr lift-off process.

substrate at 3000 rpm to a thickness of 32 nm. After coating, the sample was baked at 120 °C for 12 h and cooled with pure nitrogen gas. EBL patterning was done with a modified JEOL JSM-840-A at 35 kV, a line dosage of 40 nC cm^{-1}, and a beam current of 5 pA from a tungsten hair-pin filament. The samples were developed in *p*-xylene for 90 s, and then rinsed in isopropanol for 30 s producing 20 nm HP PS lines (figure 3(a)).

After PS development, the mould was fabricated by transferring the PS patterns into the silicon dioxide by an RIE etch. A CHF_3 plasma of 150 W etched 45 nm of silicon dioxide with an etch selectivity of the SiO_2 to the unexposed 2000 M_w PS of 2.5:1. The etch rate of the resist cross-linked by the e-beam is unknown, although it is almost certainly less than the unexposed 2000 M_w PS. After etching, the PS etch mask was removed in a bath of H_2O:H_2O_2:NH_4OH at 5:1:1 at 80 °C for 5 min producing the silicon dioxide mould (figure 3(b)).

The mould patterns selected for a metal interconnect layer of an SRAM cell array were based on a typical integrated circuit design [17]. The mould was pressed into 50 nm of NXR-2010 resist on a 30 nm sublayer film of PMMA on a quartz substrate with a pressure of 15 lbs in^{-2}. The resist was cured using UV light irradiated from the back. The mould was then separated, leaving the resist patterned with an SRAM metal layer cell array on the quartz substrate (figure 4(a)). We then further transferred the resist patterns to metal. An RIE etch removed the residual imprint and underlayer resist (see [10, 11] for details); this was followed by 15 nm of Cr evaporation and lift-off, resulting in Cr patterns on the quartz (figure 4(b)).

SEM analysis of figure 4(a) showed that the imprinted patterns for a 0.04 μm^2 SRAM cell area have a line HP of 20 nm and are free from defects with minimal line thickness variation. CD measurements and analysis showed that the imprinted polymer line patterns have an average width of 21.5 nm with a one-sigma variation of 1.3 nm. These results are due to the mould fabrication process which minimizes line edge roughness and the ability of the resist to reproduce the mould features with high fidelity.

The SRAM interconnect patterns achieved by NIL have a cell area 14 times less than that of those patterned by the current state-of-the-art photolithography [18]. Although other aspects of NIL still need to be tested, these results further show that NIL can meet the pitch resolution requirements set by the semiconductor industry for all future generation nodes [19].

Acknowledgments

This work was partially supported by DARPA and ONR.

References

[1] Vieu C, Carcenac F, Pepin A, Chen Y, Mejias M, Lebib A, Manin-Ferlazzo L, Couraud L and Launois H 2000 Electron

beam lithography: resolution limits and applications *Appl. Surf. Sci.* **164** 111–7

[2] Lister K A, Casey B G, Dobson P S, Thoms S, Macintyre D S, Wilkinson C D W and Weaver J M R 2004 Pattern transfer of a 23 nm-period grating and sub-15 nm dots into CVD diamond *Micro. Eng.* **73/74** 319–22

[3] Hiroshima H, Okayama S, Ogura M, Komuro M, Nakazawa H, Nakagawa Y, Ohi K and Tanaka K 1995 Nanobeam process system: an ultrahigh vacuum electron beam lithography system with 3 nm probe size *J. Vac. Sci. Technol.* B **13** 2514–7

[4] Dobisz E A and Marrian C R K 1991 Sub-30 nm lithography in a negative electron-beam resist with a vacuum scanning tunneling microscope *Appl. Phys. Lett.* **58** 2526–8

[5] Chapman H N *et al* 2001 First lithographic results from the extreme ultraviolet engineering test stand *J. Vac. Sci. Technol.* B **19** 2389–95

[6] Jiang X M, Ji Q, Ji L L, Chang A and Leung K N 2003 Resolution improvement for a maskless microion beam reduction lithography system *J. Vac. Sci. Technol.* B **21** 2724–7

[7] Xia Y N, Tien J, Qin D and Whitesides G M 1996 Non-photolithographic methods for fabrication of elastomeric stamps for use in microcontact printing *Langmuir* **12** 4033–8

[8] Bailey T, Choi B J, Colburn M, Meissl M, Shaya S, Ekerdt J G, Sreenivasan S V and Willson C G 2000 Step and flash imprint lithography: template surface treatment and defect analysis *J. Vac. Sci. Technol.* B **18** 3572–7

[9] Loo Y L, Willett R L, Baldwin K W and Rogers J A 2002 Additive, nanoscale patterning of metal films with a stamp and a surface chemistry mediated transfer process: applications in plastic electronics *Appl. Phys. Lett.* **81** 562–4

[10] Chou S Y, Krauss P R and Renstrom P J 1996 Imprint lithography with 25-nanometer resolution *Science* **272** 85–7

Chou S Y, Krauss P R, Zhang W, Guo L and Zhuang L 1997 Sub-10 nm imprint lithography and applications *J. Vac. Sci. Technol.* B **15** 2897–904

[11] Austin M D, Ge H, Wu W, Li M, Yu Z, Wasserman D, Lyon S A and Chou S Y 2004 Fabrication of 5 nm linewidth and 14 nm pitch features by nanoimprint lithography *Appl. Phys. Lett.* **84** 5299–301

[12] Hua F *et al* 2004 Polymer imprint lithography with molecular-scale resolution *Nano Lett.* **4** 2467–71

[13] Xu Q B, Mayers B T, Lahav M, Vezenov D V and Whitesides G M 2005 Approaching zero: using fractured crystals in metrology for replica molding *J. Am. Chem. Soc.* **127** 854–5

[14] Chen Y and Williams R S 2002 Nanoscale patterning for the formation of extensive wires *US Patent No Specification* 6407443 B2

[15] Melosh N A, Boukai A, Diana F, Gerardot B, Badolato A, Petroff P M and Heath J R 2003 Ultrahigh-density nanowire lattices and circuits *Science* **300** 112–5

[16] Manako S, Fujita J, Ochiai Y, Nomura E and Matsui S 1997 Nanometer-scale patterning of polystyrene resists in low-voltage electron beam lithography *Japan. J. Appl. Phys.* **36** 7773–6

[17] Borodovsky Y, Schenker R, Allen G, Tejnil E, Hwang D, Lo F C, Singh V, Gleason R, Brandenburg J and Bigwood R 2002 *Lithography Strategy for 65 nm Node Photomask Japan Conf. Talk (April, 2002)* ftp://download.intel.com/research/silicon/BorodovskyPhotomaskJapan0402pres.pdf

[18] http://www.intel.com/pressroom/archive/releases/20040830net.htm

[19] The international technology roadmap for semiconductors (ITRS) lithography specifications for 2004 http://www.itrs.net/Common/2004Update/2004_07_Lithography.pdf-Note: node specifications are based on random access memory (RAM) cell patterning