60-GHz CMOS Phase-Locked Loops

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Acronyms

| AMOS | Accumulation metal oxide semiconductor | | | |
|-------|---|--|--|--|
| CMOS | Complementary metal oxide semiconductor | | | |
| СР | Charge pump | | | |
| DCM | Distributed capacitance model | | | |
| DM-FD | Dual modulus frequency divider | | | |
| DSP | Digital signal processing | | | |
| DUT | Device under test | | | |
| DVCO | Distributed voltage controlled oscillator | | | |
| EMF | Electromotive force | | | |
| FCC | Federal Communication Commission | | | |
| FF | Flip-flop | | | |
| FOM | Figure of merit | | | |
| FSR | Frequency of self resonance | | | |
| FTR | Frequency tuning range | | | |
| GaAs | Galium arsenide | | | |
| HBT | Heterojunction bipolar transistor | | | |
| HDMI | High definition multimedia interface | | | |
| HDTV | High definition television | | | |
| IC | Integrated circuit | | | |
| IF | Intermediate frequency | | | |
| ILFD | Injection locked frequency divider | | | |
| ISF | Impulse sensitivity function | | | |
| ISS | Impedance standard substrates | | | |
| LPF | Low pass filter | | | |
| LO | Local oscillator | | | |
| MC | Modulus control | | | |
| MCML | MOS current mode logic | | | |
| MIM | Metal-insulator-metal | | | |
| PFD | Phase frequency detector | | | |
| PDA | Personal digital assistant | | | |
| | | | | |

| PLL | Phase-locked loop |
|------|-------------------------------------|
| PM | Phase margin |
| PMP | Portable media player |
| PN | Phase noise |
| Q | Quality factor |
| RF | Radio frequency |
| RFD | Regenerative frequency divider |
| RFIC | Radio frequency integrated circuits |
| SA | Spectrum analyzer |
| SCL | Source coupled logic |
| SFD | Static frequency divider |
| SG | Signal generator |
| SiGe | Silicon germanium |
| SoA | Silicon on anything |
| SOI | Silicon on insulator |
| TSPC | True single phase clocking |
| TWD | Travelling wave divider |
| UWB | Ultra wide-band |
| VCO | Voltage controlled oscillator |
| VNA | Vector network analyzer |
| WLAN | Wireless local area networks |
| WPAN | Wireless personal area networks |
| | |

Chapter 1 Introduction

Abstract This chapter lays the foundation for the work presented in latter chapters. The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted. Furthermore, the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book.

Keywords Wireless communication \cdot 60 GHz \cdot Millimeter wave integrated circuit design \cdot Phase-locked loop \cdot CMOS

Communication technology has revolutionized our way of living over the last century. Since Marconi's transatlantic wireless experiment in 1901, there has been tremendous growth in wireless communication evolving from spark-gap telegraphy to today's mobile phones equipped with Internet access and multimedia capabilities. The omnipresence of wireless communication can be observed in widespread use of cellular telephony, short-range communication through wireless local area networks and personal area networks, wireless sensors and many others.

The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications. Coupled with the availability of low cost radio frequency (RF) components and mature integrated circuit (IC) technologies, rapid expansion and implementation of these systems is witnessed. The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers. In addition, stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems.

At the same time, driven by customer demands, the last 2 decades have also experienced unprecedented progress in wireless portable devices capable of supporting multi-standard applications. The allure of "being connected" at anytime anywhere and desire for untethered access to information and entertainment "on the go" has set the ever increasing demand for higher data rates. As shown in Fig. 1.1, contemporary systems are capable of supporting light or moderate levels of

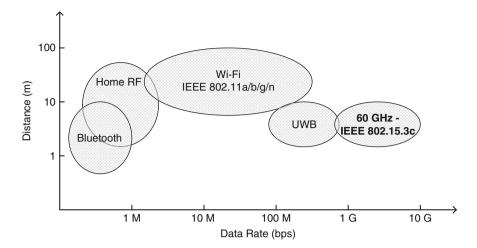


Fig. 1.1 Data rate and distance comparison for different WPAN and WLAN technologies

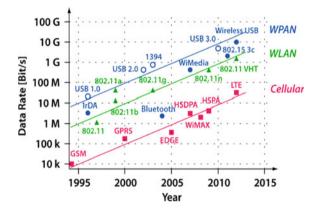


Fig. 1.2 Increasing data rate trend according to Edholm's law [2]

wireless data traffic, as in Bluetooth and wireless local area networks (WLANs). However, they are unable to deliver data rates comparable to wired standards like gigabit Ethernet and high-definition multimedia interface (HDMI) [1]. Furthermore, as predicted by Edholm's law [2], the required data rates (and associated bandwidths) have doubled every 18 months over the last decade. This trend is shown in Fig. 1.2 for cellular, wireless local area networks and wireless personal area networks for last 15 years.

The current standards and applications operating between 1 and 6 GHz have their market for long distance communication; however, in order to address the spectrum congestion and data rate issues mentioned above, new solutions have to be explored. As stated by Shannon [3], the maximum available capacity of a communication system increases linearly with channel bandwidth and logarithmically with the signal-to-noise ratio. Therefore, the obvious choice is to look upwards in the frequency spectrum where more bandwidth could be available.

An intermediate solution offered was the introduction of ultra-wide band (UWB) in 2002 by the Federal Communications Commission (FCC). It offers the frequency spectrum from 3.1 to 10.6 GHz and a minimum required bandwidth of 500 MHz for its applications. Although UWB partially solves the bandwidth issue and can potentially support high data rates, there are some limitations hindering its popularity. Firstly, international coordination is difficult to achieve among major countries and IEEE standards are not accepted worldwide. Secondly, as UWB is an overlay system over the existing 2.4 and 5 GHz unlicensed bands used for already deployed WLANs, the inter-system interference is a major concern. In order to safeguard the existing wireless systems in different regions, local regulatory bodies have defined their own requirements for UWB making world-wide harmonization of UWB almost impossible. Furthermore, to avoid interference, the allowed transmit power is low giving rise to reliability concerns. Thirdly, current multi-band orthogonal frequency division multiplexing (MB-OFDM) based UWB systems can provide data rates uptil 480 Mbps which can only support compressed video. Uncompressed high-definition television (HDTV) can easily require 2 Gbps or more data rate, which although possible by enhancing MB-OFDM UWB, increases the complexity, cost and power consumption many folds. Lastly, variation of the received signal strength over the entire UWB spectrum poses sensitivity problems for the receiver [4, 5].

The above constraints of interference, transmit power and low data rate motivated the exploration of completely unoccupied frequency band in the millimeter wave (mm-wave) regime and 60 GHz appeared as one of the promising candidates for the purpose.

In 2001, spurred by the increasing demand of high data rate applications and limitations of current wireless technologies, a 7 GHz contiguous bandwidth was allocated world-wide by the FCC. There was an immediate interest, both in academia and industry, to investigate the opportunities and possibilities using this large chunk of bandwidth. The fact that this band was unlicensed further helped in triggering the research effort. The regional regulatory bodies allocated local frequency bands with slight shift and defined the maximum effective isotropic radiated power (EIRP). Table 1.1 lists these two parameters for different regions.

The maximum allowed EIRP at 60 GHz is much higher than other existing WLANs and WPANs. This is essential to overcome the higher space path loss (according to classic Friis formula) and oxygen absorption of 10–15 dB/km as shown in Fig. 1.3 [6]. These two loss mechanisms dictate the use of 60 GHz for short range multi-gigabit per second transmission. The attenuation also means that

| Table 1.1 Regional spectrum | Region | Frequency band (GHz) | Max. EIRP (dBm) |
|---|------------|----------------------|-----------------|
| allocation and emission power requirements | Europe | 59–66 | 57 |
| power requirements | Canada/USA | 57–64 | 43 |
| | Korea | 57–64 | 43 |
| | Japan | 59–66 | 57 |
| | Australia | 59.4-62.9 | 51.8 |

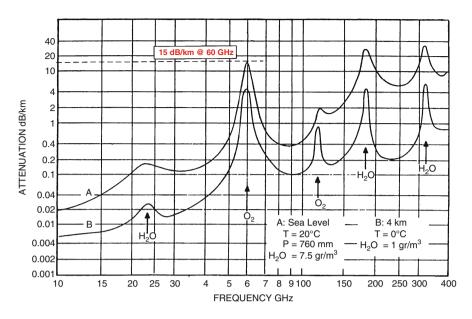


Fig. 1.3 Gaseous absorption at 60 GHz [6]

the system provides inherent security, as radiation from one particular 60 GHz radio link is quickly reduced to a level that does not interfere with other 60 GHz links operating in the same vicinity. Furthermore, this reduction enables the ability for more 60 GHz radio-enabled devices to successfully operate within one location.

Using the 60 GHz band for high data rate and indoor wireless transmission, a multitude of potential applications can be envisioned. The high definition multimedia interface (HDMI) cable could be replaced by a wireless system, transmitting uncompressed video streams from DVD players, set-top boxes, PC's to a TV or monitor. Current wireless HDMI products utilize the 2.5 and 5 GHz unlicensed spectrum where bandwidth is limited. As a result, these systems implement either lossy or lossless compression, significantly adding component and design cost, digital processing complexity and product size. Typical distance between these gadgets is 5-10 m and this communication can be point-to-point or point-to-multipoint. Depending on the resolution and pixels per line, the data rate required can vary from several hundred megabit per second (Mbps) to a few gigabit per second (Gbps). For instance, a typical high definition television (HDTV) offers a resolution of 1.920×1.080 with a refresh rate of 60 Hz. Assum-ing RGB video format with 8 b per channel per pixel, the required data rate is approximately 3 Gbps [1]. The future HDTV generation is expected to offer higher refresh rates as well as higher number of bits per channel scaling the required data rate beyond 5 Gbps. Therefore, transmitting HDTV transmission using 60 GHz remains an attractive test-case in the research field. Similarly, video and audio streams from personal digital assistant (PDA), portable media player (PMP) and laptops can also be transferred wirelessly to a display device.

In an office or home environment, 60 GHz radio links can essentially replace the clutter of cables of standards like USB, IEEE 1394, gigabit Ethernet and multimedia delivery. A PC can "talk" to all the external peripherals including printers, DVD writers, camcorders, digital cameras, external hard-disks and so forth. Wireless gigabit Ethernet and wireless ad hoc networks using 60 GHz are attractive applications for a conference room or library environment. A commercial application, particularly interesting for youth, is the so-called "Kiosk file downloading" in which users can download movies, games etc from a kiosk placed at locations like airports, railway-stations, market places and so on. These application examples are summarized in Fig. 1.4.

In addition to home and office, 60 GHz vehicular applications are also gaining much attention. They can be partitioned in three classes namely [4, 5]:

- Intra-vehicle wireless networks can be considered as a subset of WPANs that exist completely within a vehicle. The possibility of broadband communication within an automobile or aircraft by removing wired connections is desirable for manufacturers. The 60 GHz band is especially suited for intra-vehicle applications due to the containment within the vehicle and reduced ability to interfere with other vehicular networks.
- Inter-vehicle wireless networks are different from the intra-vehicle networks due to the outdoor propagation environment in the former. Applications like delivery of traffic information and range extension of mobile broadband networks are possible using inter-vehicle networks at 60 GHz.
- Vehicular radar, the last class of vehicular applications, has been deployed at millimeter-wave frequencies other than 60 GHz before; however, adaptive cruise control and automotive localization using the 60 GHz band have attracted interest in recent times.

Despite many advantages and attractive applications of short range gigabit per second wireless transmission at 60 GHz, a number of technical challenges related to design and performance need to be addressed. These can be broadly categorized into channel propagation issues, antenna technology, modulation schemes and integrated circuit technology and design.

In the last category, the choice of IC technology depends on the implementation aspects and system requirements. The former is related to the issues such as power consumption, efficiency, linearity and so on, while the latter is related to the transmission rate, cost and size, modulation etc. There are three competing IC technologies at mm-wave namely:

- Group III-V, such as Gallium Arsenide (GaAs) and Indium Phospide (InP). This technology offers fast, high gain and low noise circuits but suffers from poor integration and expensive implementation.
- Silicon germanium (SiGe) technology, such as heterojunction bipolar transistor (HBT) and BiCMOS are cheaper alternatives of GaAs and offer comparable performance.

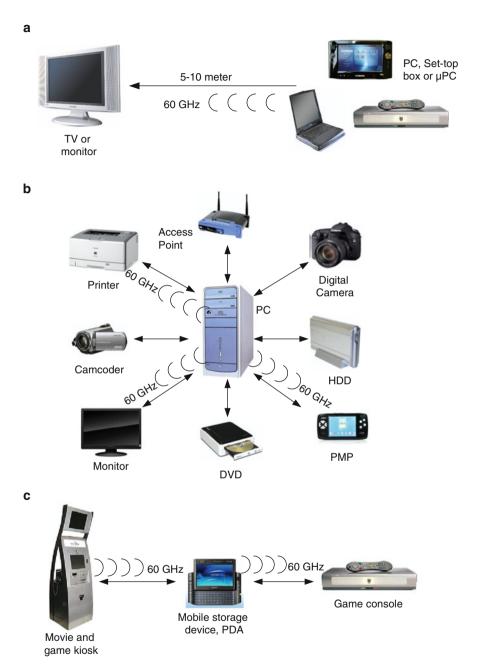


Fig. 1.4 Potential 60 GHz applications: point-to-point HDTV transmission (a), communication between a PC and different peripherals (b) and kiosk file downloading (c)

1 Introduction

• Silicon technology, such as CMOS and BiCMOS. As size and cost are key factors for mass market production and deployment, CMOS technology appears to be the leading candidate as it offers high level of integration and is economical as compared to other alternatives. The downside of using CMOS is performance degradation due to low gain, linearity constraints, poor noise, low transition frequency (f_T) etc. However, the recent advances in CMOS technology, like silicon-on-insulator (SOI) and silicon-on-anything (SOA), coupled with continuous down-scaling to sub-nanometer technologies is facilitating the implementation of integrated circuits at 60 GHz. Furthermore, high speed digital signal processing (DSP) capabilities required for processing gigabit per second data is also possible using CMOS.

In order to circumvent the abovementioned performance limitations of CMOS, especially for phase-locked loops (PLLs), number of transceiver architectures have been proposed [7–18]. These methods generally aim to reduce the working frequency of the PLLs so that up-conversion or down-conversion of the signals is carried out at a lower frequency or in two steps. Furthermore, depending on the envisioned applications, one architecture might be preferred over another.

At circuit level design, the challenges are multi-fold. Low frequency circuits are not easily scalable to 60 GHz as the foundry transistor models are usually not characterized uptil this frequency. The parasitic elements of transistors also contribute to reduced high frequency performance. Consequently, considerable design margins have to be maintained resulting in power and silicon area penalty. Furthermore, few initial dry-runs are required to characterize the devices resulting in increased design times. Similarly, passives such as inductors and transformers etc., though become affordable in terms of silicon footprint, pose modeling related uncertainties and require meticulous electromagnetic (EM)-simulations. The quality factor (Q-factor) of varactors, which are invariably employed for capacitive tuning in voltage controlled oscillators (VCOs), frequency dividers etc, becomes very low. Low-ohmic substrate is also a hindrance in high-Q passive design. The technology scaling to sub-nanometer technologies reduces the supply and breakdown voltages, whereas the threshold voltage of transistors does not scale with the same order, resulting in a limited choice of reliable circuit topologies.

At layout level, as the wavelength of on-chip signals approach circuit dimensions, the interconnect between components becomes crucial part of design. These interconnects have to be simulated in EM solvers to incorporate the affect on circuit performance. Depending on the type of interconnect, this step is generally time consuming especially if multiple metal layers and vias are included. Furthermore, due to close proximity of components the overall layout also needs to be simulated for unwanted coupling and losses. Layout parasitics are also a major contributor for frequency shift and performance degradation and demand careful RLC extraction. Asymmetric layout of the RF paths at 60 GHz is a potential issue especially in circuits requiring phase accuracy. The typical layout approach of "smaller the better" at 60 GHz is sometimes contradictory to the symmetry requirement and some compromise has to be adopted. The measurement of 60 GHz and millimeter wave circuits, pose a different set of challenges. Dedicated measurement equipment, components and setup is required for high frequency measurements. In some cases, when direct measurement of a parameter is not possible, in-direct methods are employed which are source of measurement errors. In order to shift the measurement plane to the device-under-test (DUT), accurate calibration and de-embedding is required. The losses and mismatch associated with cables, connectors, adapters have to be carefully accounted for. The stability and repeatability of accurate measurements is also an important challenge in high frequency measurements.

The challenges at 60 GHz related to circuit, layout, measurement and technology, mentioned in the preceding discussion, assist to select the set of problems which will be tackled in this book.

Firstly, due to the application dependence, there is no preferred transceiver architecture for 60 GHz. Thus, several different architectures can be expected in future. In order to cater for more than one application, a flexible synthesizer architecture will therefore be required. Moreover, such a multipurpose synthesizer will be expected to reuse some of its components to reduce design overhead. Secondly, a lack of design paradigm for 60 GHz is witnessed where the layout intricacies and measurement issues are understudied and lastly, the profound impact of parasitics necessitates the need of modification in the design flow of mm-wave integrated circuits. Adopting a top-down approach, this book addresses the above three problems by:

- System level analysis, design and realization of a flexible phase-locked loop suitable for a number of frequency up/down-conversion choices in a 60 GHz transceiver.
- Identifying the critical components of the synthesizer and characterizing them individually before complete system integration.
- Characterizing of passives, such as inductors, transformers and transmission lines that are extensively utilized in 60 GHz IC design.
- Revisiting the mm-wave IC design flow and incorporating the impact of parasitics (from circuit as well as layout) at an advanced stage of the design cycle.
- Identifying measurement issues for mm-wave circuits and providing possible solutions.

The structure of this book is illustrated in Fig. 1.5. In Chapter 2, after a brief overview of IEEE standardization for 60 GHz band and frequency conversion choices, a flexible PLL architecture is proposed. Based on theoretical analyses and system simulations of this architecture, target specifications are laid down for the PLL.

Chapter 3 discusses the layout and measurement techniques widely employed throughout this work. The circuit design of PLL components is divided in two chapters. The high frequency components, namely prescaler and voltage control oscillator (VCO) are discussed in Chapter 4. A variety of prescaler architectures are compared and two types are designed and measured. A number of VCOs are designed and measured with attention on improvement of tank quality factor,

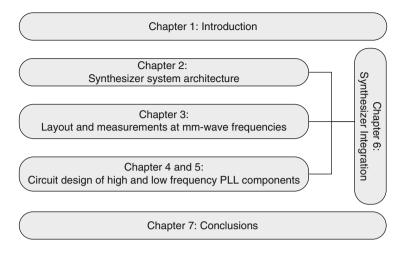


Fig. 1.5 Structure of the book

modeling of tank inductor and transformers, and compact and symmetrical layouting techniques. The low frequency components such as the feedback divider chain, phase frequency detector (PFD), charge pump (CP) and loop filter are presented in Chapter 5. Optimization techniques for feedback divider chain, dead-zone removal in PFD and accurate current matching in CP are also discussed in this chapter.

Chapter 6 presents the integration of the complete PLL and discusses solutions for different frequency conversion choices. It is observed that connecting different blocks with perfect frequency alignment is much more challenging than designing individual blocks. This is because any unexpected parasitic of the interface between the blocks can potentially cause significant shift in the VCO and dividers, causing reduction in PLL locking range or in worst case prohibiting the loop from locking. A comparison to target specifications is also included in this chapter. The conclusions of this book are presented in Chapter 7.

Chapter 2 Synthesizer System Architecture

Abstract This chapter discusses the system level aspects of frequency synthesizer design for 60 GHz. The IEEE 802.15.3c standard determines the frequency channelization of the 60 GHz band, based on which the frequency planning is carried out. A number of in-direct PLL architectures can be used for 60 GHz transceivers which are discussed in detail. Based on the proposed synthesizer architecture, the analytical calculations and system level simulations are presented. The chapter concludes by enlisting the target specifications for the proposed synthesizer.

Keywords IEEE 802.15.3c \cdot 60 GHz \cdot Phase-locked loop \cdot Frequency synthesizer \cdot Advanced design systems \cdot Phase noise \cdot Open-loop gain \cdot Phase margin

A phase-locked loop is an important block of transceivers and exists in the majority of wireless communication systems. Its application varies from generation, recovery and distribution of clock signals to jitter and noise reduction. They are also utilized to implement spread spectrum techniques to reduce interference with high-Q receivers and as a de-skewing block to phase match the clock in electronic systems. The most extensive use of PLLs is for frequency synthesis (also focus of this book), in which they are used to generate a local oscillator signal for up-conversion in a transmitter and down-conversion in a receiver as shown in Fig. 2.1. The requirements and architecture of a synthesizer depend on the system specifications which are based on the underlying regulatory standard. Performance parameters like tuning range, channel spacing or step size, spectral purity, phase noise, output power, settling time and spurious are some of the specifications required before the design phase.

The regulatory efforts for 60 GHz band are being carried at two fronts. IEEE has assigned a task group 3c for developing a millimeter-wave based alternative physical layer (PHY) for the existing 802.15.3 standard [19]. The second effort is by industrial consortiums such as WirelessHD[™] and ECMA International. The WirelessHD alliance has proposed a protocol that enables consumer devices to create a wireless video area network for streaming high-definition content between source and display devices [20]. ECMA International on the other hand published its 60

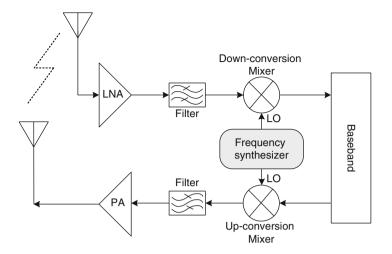


Fig. 2.1 A general transceiver block diagram

GHz industrial standard in December 2008. In addition to 60 GHz PHY, this standard includes MAC and HDMI PAL specifications for short range gigabit per second wireless transmission for both bulk data transfer and multimedia streaming [21]. Section 2.1 discusses the IEEE 802.15.3c channelization proposals with particular focus on PLL requirements.

Integrated circuits at 60 GHz involve significant challenges at system, circuit and layout levels as discussed in Chapter 1. However, some of these can be mitigated by taking advantage of the capabilities available at one level to relax the requirements imposed at another. For instance, to ease the requirements of a frequency synthesizer at system level, special transceiver architectures for up-conversion and down-conversion of data can be envisioned. Termed as frequency conversion (FC) techniques in this book they generally aim to operate the synthesizer at a sub-LO frequency and generate the 60 GHz LO signals indirectly. Adopting this approach makes a wide variety of architectures possible by selecting different LO frequency combinations along with the synthesizer. Consequently, each resulting architecture requires a specific synthesizer and a need for a flexible synthesizer is naturally felt. This chapter proposes a flexible PLL which can be utilized for a number of 60 GHz FC techniques. While minimizing overhead, the focus is to re-use a considerable portion of the PLL and provide flexibility at the same time. The 60 GHz FC techniques are categorized in Section 2.2, and Section 2.3 presents the proposed synthesizer architecture.

Analytical calculations and system simulations using tools such as Advanced Design System (ADS) provide a first insight into the required specifications of the PLL and its individual sub-components. Section 2.4 includes the theoretical analysis of the PLL system and, aided with simulations, leads to the target specifications mentioned in Section 2.6. The conclusions of the chapter are presented in Section 2.7.

2.1 IEEE 802.15.3c Channelization

The IEEE 802.15.3 Task Group 3c (TG3c) was formed in March 2005. It is developing a millimeter-wave-based alternative physical layer (PHY) for the existing 802.15.3 wireless personal area network (WPAN) standard 802.15.3-2003. The standard is still a work in progress, and when completed, is expected to provide the first widespread international physical layer framework to support consumer 60 GHz WPANs. In September 2007, after merging and narrowing down, the task group confined its selection for 60 GHz physical layer to two proposals. These two proposals offer different possibilities of spectrum occupancy, transmission modes, modulation schemes, packet and frame structure, beam forming etc.

The channelization proposals for the 60 GHz band are based on high rate PHY (HRP) and low rate (LRP). The use of each depends on the data rate requirement for a certain type of communication. The HRP, having a bandwidth of 2 GHz, is used for high definition video streaming, file transfer and similar applications where multi-gigabit per second data rate is required. The channelization is shown in Fig. 2.2. The LRP, on the other hand, is used for relatively low data rate asynchronous transfer such as compressed audio, control commands including pilot, beacon and acknowledgment signals, etc. There are two proposals for the low rate channelization of four 2 GHz channels either contains four 1 GHz channels or twelve 500 MHz channels. The channelization for LRP is shown in Figs. 2.3 and 2.4, respectively.

It can be noted that the center frequencies for 1 and 2 GHz channels are identical and only differ in the guard band between two adjacent channels. The spectrum utilization of the 500 MHz sub-channels is better than the 1 GHz ones and at least

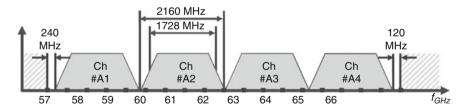


Fig. 2.2 High data rate channelization with 2 GHz bandwidth [19]

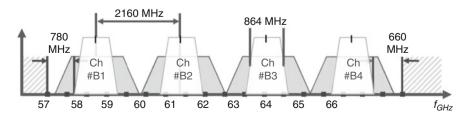


Fig. 2.3 Low data rate channelization with 1 GHz bandwidth [19]

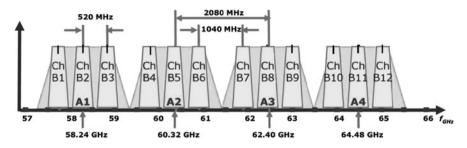


Fig. 2.4 Low data rate channelization with 500 MHz bandwidth [19]

nine out of 12 channels are available in all regions. The above mentioned channelization is important for a 60 GHz PLL design as it determines the frequencies required from the PLL and also some in-direct specifications such as reference frequency, loop bandwidth, etc. These proposals also indicate that, if such a channelization is finalized, the PLL should be able to generate all 2 GHz as well as all sub-channels of 1 GHz and 500 MHz.

2.2 60 GHz Frequency Conversion Techniques

As mentioned briefly in Chapter 1, the PLL (as frequency synthesizer) related challenges at millimeter wave frequencies is one of the dominating factors in transceiver design and necessitates the development of "synthesizer-friendly" transceivers. The generation, division and distribution of a mm-wave LO (signal used for up- and down-conversion) becomes so demanding that the choice of transmitter (TX) and receiver (RX) architectures become closely intertwined with the synthesizer design [22].

Therefore it is pertinent to categorize the approaches for up- and downconversion (or frequency conversion) of data for 60 GHz transceivers which will also determine the associated synthesizer architectures. The general aim is to reduce the operation frequency of the synthesizer while maintaining a robust overall system.

The first category in Fig. 2.5a illustrates a two step down-conversion method, a special case of which is referred to sliding-IF architecture. The incoming RF signal f_{RF} is first down-converted by mixing with the RF local oscillator signal f_{RF-LO} producing a difference (and sum) component at $f_{RF} - f_{RF-LO}$. The second down-conversion to baseband is achieved by using the output of the prescaler of the frequency synthesizer f_{IF-LO} . The factor 'M' refers to an integer frequency multiplier which can have a usually range between 1 and 3. The value of 1 implies a direct connection between the oscillator and the mixer whereas a value of 2 and 3 implies a frequency doubler and tripler, respectively. The factor 'P' is the