65-GHz Receiver in SiGe BiCMOS Using Monolithic Inductors and Transformers

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***Abstract* — This paper describes a single-chip 65-GHz SiGe BiCMOS radio receiver IC which includes an LNA, a transformer balun, a downconversion mixer, an IF amplifier, and a 65-GHz VCO. The single-ended downconversion gain is 21 dB with an input compression point of -22 dBm. The DSB receiver noise figure is a record 12 dB for IF frequencies in the 0 to 2 GHz range. By employing only transformers and inductors as matching elements, the die area, which includes all pads, is 790 µm x 740 µm.**

***Index Terms*— 65-GHz Radio, mm-wave receiver, mm-wave LNA, monolithic inductors and transformers.**

I. Introduction

65-GHz mm-wave radio components have recently become a topic of interest for silicon IC research. Several SiGe HBT and 130-nm CMOS building blocks have been reported [1-6]. The highest level of integration to date has been realized in the receiver where the LNA, downconvert mixer, and IF amplifier have been integrated on a single SiGe HBT [1] or 130-nm CMOS die [3].

The work presented in this paper integrates for the first time the VCO with the full receiver, seen in Fig. 1, which relies only on inductors and transformers, instead of area-intensive transmission lines or hybrid couplers [1-3], to minimize die area and cost. The circuits are fabricated in a commercial 0.18µm SiGe BiCMOS process with 160 GHz f_T/f_{MAX}. Given the limited performance margin of the technology at 65 GHz, the system level design goal was to maximize the dynamic range, a key factor in radio transceiver link budget. In an effort to minimize the overall noise figure, a weak spot for all state-of-the-art silicon technologies at this frequency, each building block has been designed following established low-noise amplifier design techniques [4].

The next section will discuss the individual receiver blocks. Section III presents the fully integrated receiver and its operation followed by conclusions in section IV.

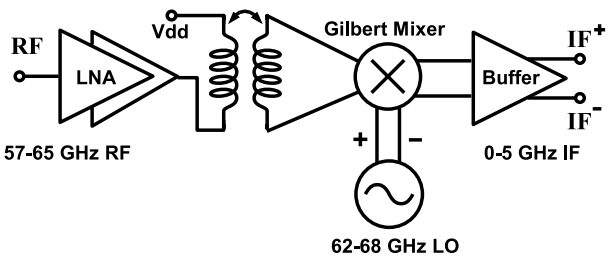

Fig. 1. Simplified 65-GHz receiver block diagram.

II. Building Blocks

A. Inductors and Transformers

Rather than employ wide metal lines and a large number of turns, as is common at RF frequencies, the designed mm-wave inductors have minimum width and spacing and feature a vertically stacked multi-metal structure which maximizes inductance per area. The resulting inductors have diameters smaller than 30 µm, lowering the substrate loss, the primary cause of Q degradation at these frequencies [7]. Due to their small size, these inductors exhibit higher Q and lower loss at mm-wave frequencies than T-lines with equivalent inductance.

A non-conventional inductor structure has been fabricated to study the effects of a continuous metal ground plane on its operation. This multi-metal inductor with a diameter of 26µm is shown in Fig. 2a. A metal-1 ground plane, similar to that used for microstrip T-lines, is placed under the inductor to shield it from the substrate. At first it would appear that this inductor structure would fail because of increased oxide capacitance and reduced inductance (given the reduced magnetic field at the Metal-1 interface). However due to the small size of the inductors and the relatively thick dielectric between the top and bottom metal layers (larger than the inner diameter

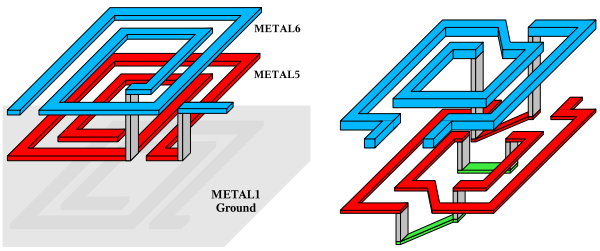

Fig. 2. (a) Spiral multi-metal inductor over metal-1 ground shield (b) symmetric stacked transformer.

of the inductor) these effects are less pronounced.

The L_{eff} and Q_{eff} extracted from measured Y-parameters are plotted in Fig. 3 comparing a traditional inductor over silicon and an inductor over metal. Q_{eff} and L_{eff} are reduced by only 15% when a metal ground plane is placed below the inductor while C_{ox} slightly increases to 9.9 fF from 7.9 fF. The main benefits of such a structure are reduced substrate coupling, simpler modeling due to the elimination of the lossy silicon substrate, and low-inductance ground plane routing for adjacent components, a non-trivial problem at 65 GHz.

The transformer features a vertically stacked 1:1 structure implemented in two adjacent metal layers (Fig. 2b) to increase coil coupling and minimize its area [7]. The measured single-ended power transfer characteristics of the transformer, S_{21}, are plotted in Fig. 4 demonstrating its suitability for operation in the 40 to 94 GHz range. This is the highest frequency monolithic transformer reported to date in any technology.

B. LNA

The schematic of the two-stage, single-ended 65-GHz cascode LNA and the corresponding die photo of the breakout circuit can be seen in Fig. 5. The cascode topology was chosen for its robustness to process and model variation, excellent isolation, and high gain. It has higher linearity when compared to common base [1] and common gate [3] configurations. Linearity and dynamic range are severely compromised in the latter two because of the low currents required for 50Ω-matching.

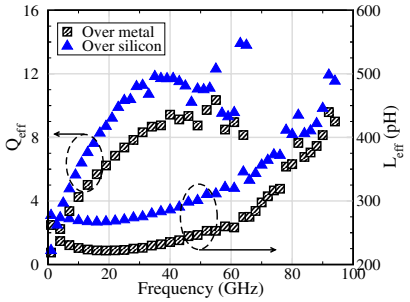

Fig. 3. Measured effective inductance and Q for the inductor with and without the metal ground plane.

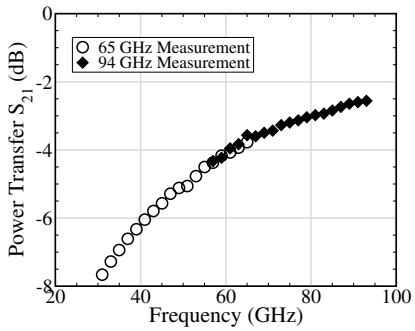

Fig. 4. Measured transformer coupling (single ended S_{21}).

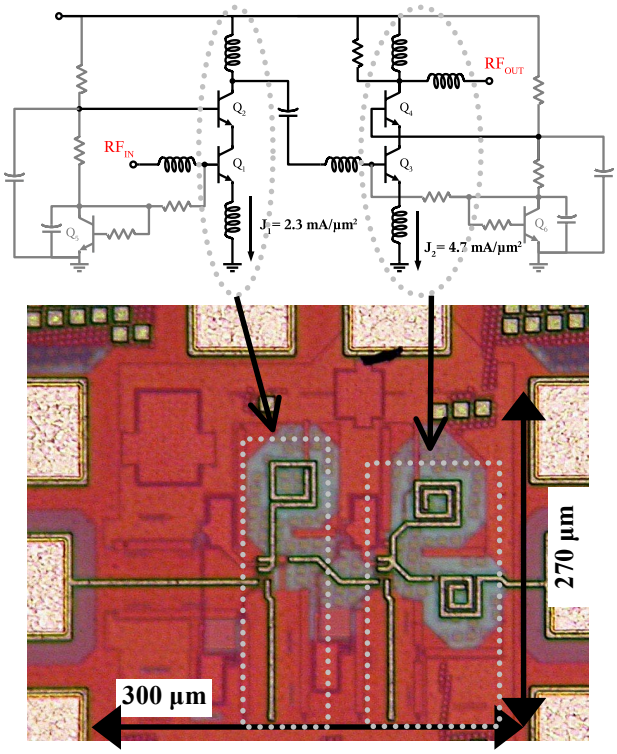

Fig. 5. Single-ended LNA (a) schematic and (b) die photograph

The first stage transistors of the LNA are biased at the minimum noise measure current density corresponding to 65-GHz operation. Their sizes have been designed for concurrent input impedance and noise matching, as described in [4]. The current density of transistors in the second stage was scaled up to maximize linearity.

The measured S-parameters of the LNA are plotted in Fig 6. The power gain, S_{21}, is 14 dB peaking at 65 GHz, S_{11} and S_{22} are < -15 dB, and the isolation is better than 30 dB. The circuit is biased from a 2.5-V supply and consumes 13.3 mA. The 1dB compression point of the LNA, plotted in Fig. 7, was measured using the Agilent E4448A spectrum analyzer and the Agilent 11970V downconversion mixer. The -4 dBm input compression of the measurement setup was de-embedded using the equation below resulting in a de-embedded LNA input P_{1dB} of -12.8 dBm

$$\frac{1}{P_{1\mathrm{dB},measured}} = \frac{1}{P_{1\mathrm{dB},LNA}} + \frac{G_{LNA}}{P_{1\mathrm{dB},setup}}$$

This LNA breakout circuit represents the first SiGe inductor-based and cascode LNA operating at 65 GHz.

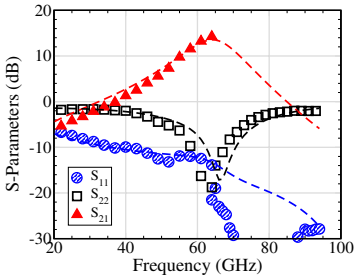

Fig. 6. Single-ended LNA S-parameter measurements (symbols) versus simulations (lines).

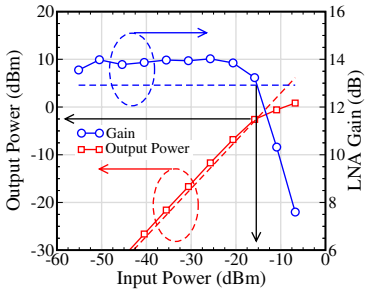

Fig. 7. Single-ended LNA input 1dB compression.

C. Down-conversion Mixer

The down-conversion mixer employs a Gilbert-cell topology, as shown in Fig 8(a). A symmetrical transformer, discussed earlier, operates as a balun at the input of the mixer to connect to the output of the single-ended LNA. The transformer has a center-tap on the secondary coil through which the DC bias is applied to the RF inputs of the Gilbert cell. The mixer has conversion gain of 7 dB with a simulated input P_{1dB} of -4 dBm. It operates with a tail current of 12 mA from a 3.3 V supply.

D. IF Amplifier

The IF amplifier in Fig 8(b) has the MOS differential pair biased at the peak f_T current density of 0.3mA/μm for increased bandwidth and linearity. The amplifier is output-matched to 50 Ω and was designed to handle 1 Gbps signals at IF frequencies up to 5 GHz. The tail current is 30 mA and it operates from a 3.3 V supply with a simulated single-ended input P_{1dB} of -1.3 dBm and a 3-dB bandwidth of 10 GHz.

E. VCO

The VCO uses a differential cascode Colpitts topology and was previously presented in [5]. It features an LC-varactor tank and has a wide tuning range of 13%. As a result of the low-noise amplifier techniques employed in its design the phase noise is -104 dBc/Hz at 1 MHz offset. The varactor size was slightly reduced from the original design to increase the VCO center frequency to 63 GHz.

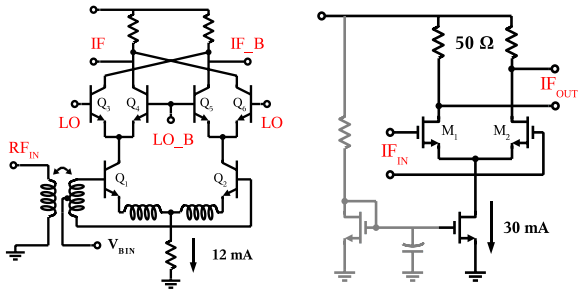

Fig. 8. (a) Downconvert mixer and (b) IF amplifier schematic.

III. Fully Integrated Receiver

The block diagram of the 65-GHz receiver is presented in Fig. 9. It includes the single-ended LNA, double-balanced mixer, differential Colpitts VCO, and IF amplifier. Single-ended to differential conversion is performed using the on-chip transformer balun. The gain and P_{1dB} compression points of the Rx blocks have been designed to optimize overall system linearity.

The die photo of the fully integrated receiver is shown in Fig. 10. The area, excluding pads is only 550μm x 440μm (0.25mm^2), 10x smaller than that of circuits using branch-line couplers [1] or coplanar waveguides (CPW) [2]. The compact layout results in reduced parasitics, which otherwise would lead to a significant degradation in performance at this frequency. The measured single-ended receiver gain is 21 dB, equivalent to 24 dB differentially. The measured DSB noise figure is 12 dB and remains flat versus IF frequency as seen in Fig 11. In this measurement, the LO frequency is fixed at 63 GHz.

Rx gain compression is plotted in Fig. 12, indicating an input P_{1dB} point of -22 dBm for an IF frequency of 2 GHz. The total power consumption of the receiver is 540 mW – 260 mW for the VCO, 100 mW for the VCO buffers, 80 mW for the LNA and mixer, and 100 mW for the IF amplifier. While the VCO is fixed at a 4 V supply, the rest of the receiver can be operated from as low as 2.5 V, consuming 450 mW. When operated from 2.5 V, the conversion gain is reduced to 15 dB and the noise is increased to 12.2 dB. The large VCO power is dictated by the requirement for low phase noise and to provide adequate voltage swing for the double-balanced mixer.

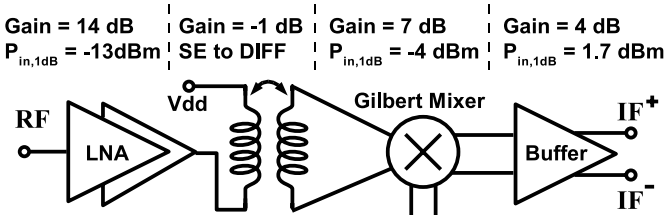

Fig. 9. Linearity and gain distribution in the 65-GHz Rx chain.

IV. Conclusion

A 65-GHz single-chip receiver was fabricated in a 0.18µm SiGe BiCMOS process having f_T and f_{MAX} of 160 GHz. Taking advantage of the RF backend, high density multi-metal spiral inductors and non-traditional inductor structures, placed above metal ground planes, the core receiver area was reduced to 550µm x 440µm or 790µm x 740µm with pads. This represents significant area savings as compared to previously reported circuits operating at this frequency and which rely on area intensive µ-strip and CPW transmission lines.

The receiver performance is summarized in Table 1 and is compared with that of other mm-wave radio blocks reported to date.

Acknowledgement

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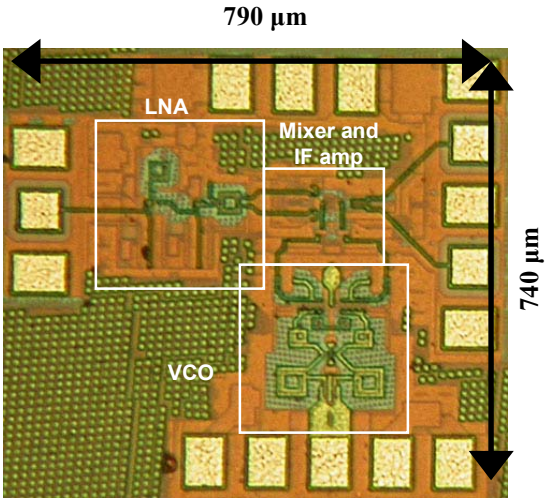

Fig. 10. Die photo of the fully integrated Rx.

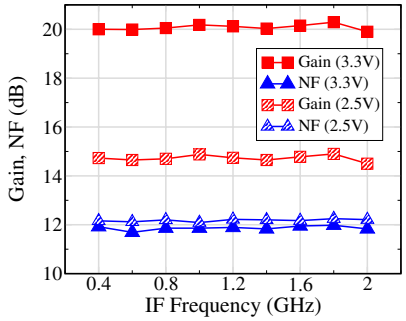

Fig. 11. Measured single-ended Rx gain and DSB noise figure.

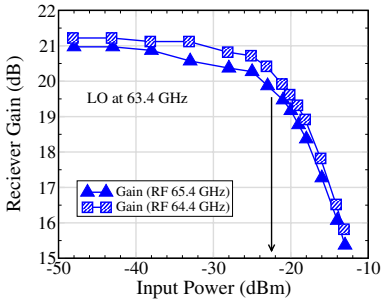

Fig. 12. Measured receiver 1-dB gain compression.

Table 1. Comparison of silicon mm-wave radio blocks

Technology	**0.12 µm SiGe Bipolar**	**0.13 µm CMOS**	**0.13 µm CMOS**	**0.18 µm SiGe Bipolar**	
Integration Level	LNA, mixer, branch-line coupler, tripler	LNA	LNA, µ-strip balun, quadrature mixer	LNA	LNA, mixer, VCO, transformer balun, IF amplifier
Freq.	61.5 GHz	60 GHz	60 GHz	65 GHz	65 GHz
Gain	16 dB	12 dB	28 dB Voltage gain	14 dB	24 dB
NF	14.8 dB	8.8 dB	12.5 dB	-	12 dB
P_{1dB}	-17 dBm	-11 dBm	-22.5 dBm	-12.8 dBm	-22 dBm
DC Power	300 mW (2.7V)	54 mW (1.5V)	9 mW (1.2V)	33 mW (2.5V)	540 mW (3.3V, 4V for VCO)
Die area	1.9 x 1.65 mm	1.3 x 1.0 mm	0.3 x 0.4 mm (no pads)	0.37 x 0.46 mm	0.79 x 0.74 mm
Reference	[1]	[2]	[3]	This work	This work