85nm Gate Length Enhancement and Depletion mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications

S. Datta, T. Ashley*, J. Brask, L. Buckle*, M. Doczy, M. Emeny*, D. Hayes*, K. Hilton*, R. Jefferies*, T. Martin*, T. J. Phillips*, D. Wallis*, P. Wilding* and R. Chau
Components Research, Technology and Manufacturing Group, Intel Corporation, Hillsboro, USA
*QinetiQ, Malvern Technology Center, Malvern, UK
Email: robert.s.chau@intel.com

Abstract

We demonstrate for the first time 85nm gate length enhancement and depletion mode InSb quantum well transistors with unity gain cutoff frequency, f_T, of 305 GHz and 256 GHz, respectively, at 0.5V V_{DS}, suitable for high speed, very low power logic applications. The InSb transistors demonstrate 50% higher unity gain cutoff frequency, f_T, than silicon NMOS transistors while consuming 10 times less active power.

Introduction

Indium antimonide (InSb) holds promise for ultra-fast, very low power digital logic applications as it has the highest electron mobility and saturation velocity of any known semiconductor. This performance potential was demonstrated before in a 200nm gate length (L_G) depletion mode InSb quantum well transistor (QWFET) with 150GHz f_T at 0.5V V_{DS} [1] and subsequently a 100nm L_G depletion mode device with 210GHz f_T [2]. In both cases, the transistors were fabricated on a semi-insulating GaAs substrate using a relaxed metamorphic buffer layer of $Al_yIn_{1-y}Sb$ to accommodate lattice mismatch, a compressively strained InSb quantum well confined between layers of $Al_xIn_{1-x}Sb$ and a Schottky barrier metal gate. The quantum well transistor architecture employs barrier layers with higher bandgap materials to mitigate the effect of the narrow bandgap InSb on device leakage and breakdown. For high speed direct coupled FET logic (DCFL) applications, both enhancement (i.e. positive V_T) and depletion mode devices are required. In this paper, we report, for the first time, on the fabrication and characterization of 85nm gate length enhancement (e-mode) and depletion mode (d-mode)InSb QWFETs. An enhancement mode InSb QWFET is demonstrated for the first time using a deep recess etch in the gate region, which shows a peak f_T of 305GHz at 0.5V V_{DS}. A depletion mode device is demonstrated at the same time utilizing a shallow recess gate with a peak f_T of 256GHz at 0.5V V_{DS}. The demonstration of both high performance depletion and enhancement mode InSb QWFETs makes the technology a promising candidate for future high speed, low power logic applications. Benchmarking with advanced silicon MOSFETs indicates that the InSb QWFETs can provide 1.5× faster switching speed with a simultaneous 6-10× reduced DC power dissipation. Due to the small gate to channel separation, the deep recess gate 85nm L_G e-mode devices exhibit excellent sub-threshold slope of 105 mV/dec and DIBL of 95mV/V, with maximum I_{ON}-I_{OFF} ratio of 330 limited by the gate leakage current. To improve the I_{ON}-I_{OFF} ratio, a promising high-k dielectric on the AlInSb/InSb device layers is identified here with moderate hysteresis, low frequency dispersion and four orders of magnitude reduction in gate leakage.

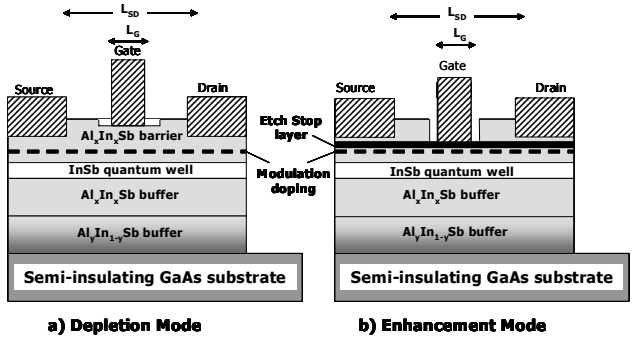

Fig. 1 Schematic of the depletion mode and enhancement mode InSb quantum well transistors

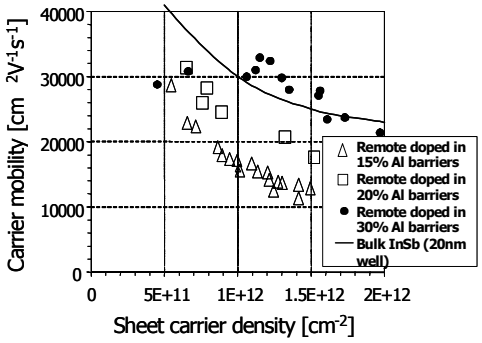

Fig. 2 Hall Mobility data on modulation doped 20nm thick InSb quantum wells with 15%, 20% and 30% Al in the $Al_xIn_{1-x}Sb$ barrier layer [1]

Enhancement and Depletion Mode InSb Transistors

Both depletion and enhancement mode InSb QWFETs were fabricated on semi-insulating GaAs substrates. The layers from the bottom to top consist of an accommodation layer, a 3μm $Al_yIn_{1-y}Sb$ buffer, a 20nm thick InSb quantum well, a 5nm thick $Al_{0.2}In_{0.8}Sb$ spacer, a single Te δ-doped donor layer (1-1.8×10^{12}cm^{-2} and μ=18-25000cm^{2}V^{-1}s^{-1}) and a 45nm thick $Al_{0.2}In_{0.8}Sb$ barrier layer with an optional etch-stop layer.

0-7803-9269-8/05/$20.00 (c) 2005 IEEE

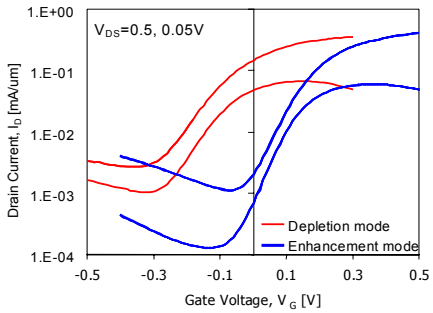

Fig. 3 I_D-V_G transfer characteristics of 130nm L_G depletion mode and enhancement mode InSb QWFETs

Increasing the Al percentage in the upper barrier to 30% would increase the QW room temperature electron mobility to 30,000cm^{2}V^{-1}s^{-1} with a sheet carrier density of 1.3×10^{12} cm^{-2} further demonstrating the potential for improved high speed performance (Fig. 2). For the e-mode devices, an increased δ doping level is used to reduce the access resistance and a highly selective etch chemistry to deep recess the gate. Fig. 3 compares the typical transfer characteristics of the 130nm L_G e- and d-mode devices with a threshold voltage, V_T, shift of 250mV. Fig. 4 shows that the e-mode devices have improved V_T roll-off characteristics and, hence, better short channel effects than the d-mode devices. This is further illustrated in Figs. 5 and 6, where the deep recess gate e-mode devices show much improved sub-threshold slope and DIBL characteristics over the depletion mode devices due to shorter gate to channel separation. This implies that small gate to channel separation is a key component of L_G scaling for future InSb based QWFETs. Fig. 7 compares the intrinsic (de-embedded) cut-off frequency, f_T, of 85nm gate length depletion and enhancement mode devices with a fixed source to drain separation, L_{SD}, of 0.75µm. The e-mode devices show higher performance due to lower access resistance from the increased δ-doping level. The effect of access resistance on f_T resulting from the finite source to drain separation is illustrated in Fig. 8 where the peak f_T decreases monotonically as a function of L_{SD} for both depletion and enhancement mode devices.. Figs. 9 and 10 show the DC output and transfer characteristics of the enhancement mode devices which show the I_{ON}-I_{OFF} ratio limited by the reverse

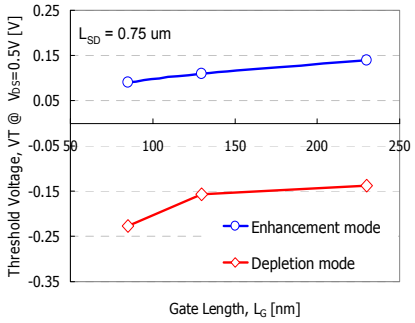

Fig. 4 Threshold voltage roll-off as a function of gate length for depletion and enhancement mode InSb QWFETs

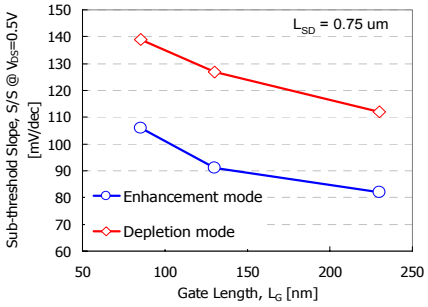

Fig. 5 Sub-threshold slope as a function of gate length for depletion and enhancement mode InSb QWFETs

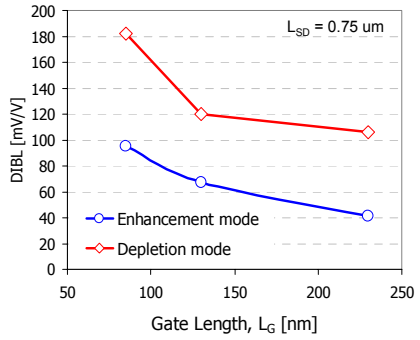

Fig. 6 DIBL as a function of gate length for depletion and enhancement mode InSb QWFETs

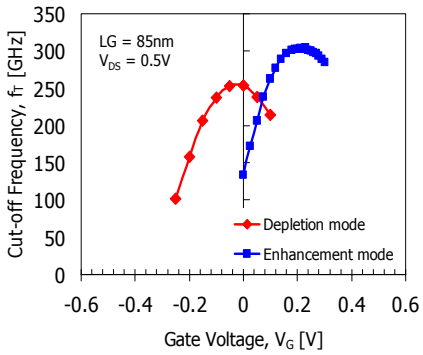

Fig. 7 Intrinsic (de-embedded) cut-off frequency, f_T, for 85nm gate length depletion and enhancement mode InSb QWFETs at 0.5V V_{DS}

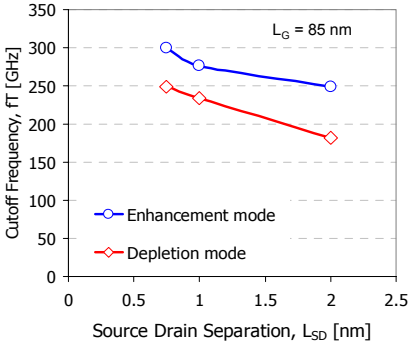

Fig. 8 Peak f_T as a function of source drain separation, L_{SD}, for 85nm L_G depletion and enhancement mode InSb QWFETs at 0.5V V_{DS}

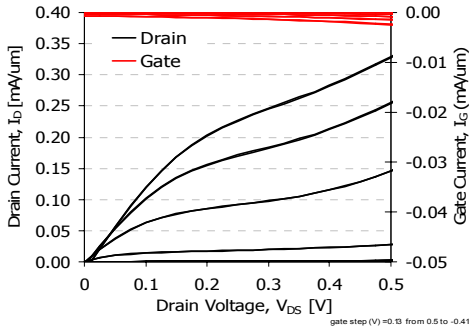

Fig. 9 Output characteristics of 85nm L_G e-mode InSb QWFET with L_{SD}=0.75 µm (V_{GS}=0.5V to -0.41V in 0.13V steps)

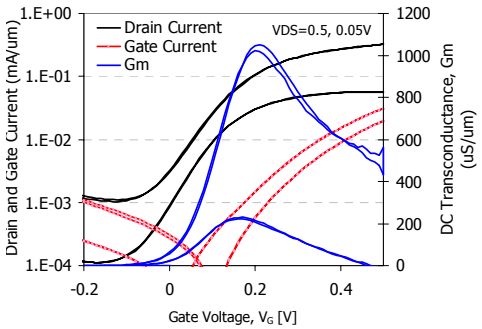

Fig. 10 Transfer characteristics of 85nm L_G e-mode InSb QWFET with L_{SD}=0.75 µm (V_{DS}=0.5 and 0.05V)

biased Schottky gate leakage. Scaled, high-performance InSb QWFETs with reduced gate leakage are required for future low power logic applications and could be achieved using an ultra-thin metal gate/high-k dielectric stack [3].

High-K Gate Dielectric on AlInSb/InSb

In the past 25 years of digital III-V technology, the lack of a high quality native oxide coupled with the limited barrier height of Schottky metal gate from surface Fermi level pinning, has posed serious challenges for III-V based DCFL implementation. We report, for the first time, promising results on high-k dielectric development on AlInSb/InSb device layers. Figs. 11 and 12 show the effect of two cases of AlInSb surface pre-treatment on the room temperature C-V frequency dispersion characteristics of high-k/metal gate stack on AlInSb/InSb. The high-k dielectric, in this case, is Al_2O_3 (alumina) deposited using a low temperature atomic layer deposition (ALD) process. XPS results indicate that the surface pre-treatment A oxidizes the AlInSb surface forming indium oxide, which results in a high density of interface states. The surface pre-treatment B mitigates the oxidation process, resulting in much reduced frequency dispersion in the accumulation region. The frequency dispersion in the inversion region is a combination of a) minority carrier generation in low bandgap AlInSb/InSb material system and b) the generation/recombination from the surface traps. The room temperature C-V characteristics with the more optimized process exhibits a moderate level of hysteresis, as shown in the

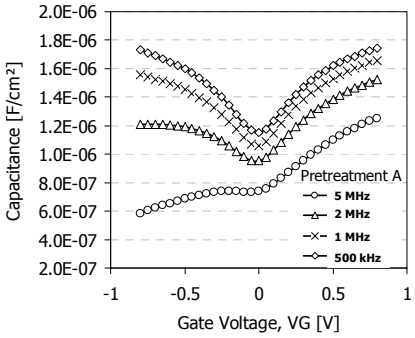

Fig. 11 Room temperature C-V characteristics of Al/Al_2O_3/AlInSb/InSb MOSCAP with surface pre-treatment A

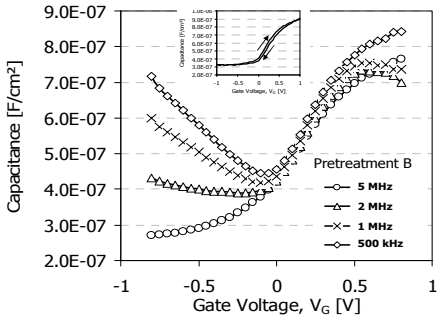

Fig. 12 Room temperature C-V characteristics of Al/Al_2O_3/AlInSb/InSb MOSCAP with surface pretreatment B

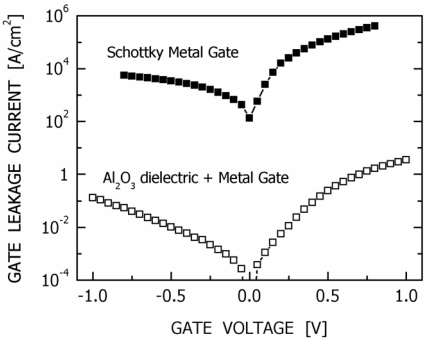

Fig. 13 Room temperature gate to channel leakage characteristics for ALD Al_2O_3 high-k dielectric and Al metal gate stack on AlInSb/InSb device layers showing four orders of magnitude reduction in leakage compared to Schottky metal gate

inset of Fig. 12, which is believed to be from elemental antimony acting as hole traps [4]. The high-k/metal gate stack results in four orders of magnitude reduction in the gate leakage current compared to the Schottky metal gate stack (Fig. 13).

Summary

At this early stage of development, 85nm L_G enhancement mode InSb QWFETs show 50% higher intrinsic switching frequency and a simultaneous 10× reduction in DC power dissipation compared to the advanced Si MOSFETs (Fig 14).

Fig. 15 plots the intrinsic gate delay (CV/I) vs. gate length trend of InSb QWFETs benchmarked against the historical and future Si nMOS transistor scaling trend. It shows that, for a given physical gate length, the InSb devices offer 2.8× reduction in gate delay. Fig. 16 shows that for a given physical gate length, the InSb devices also offer more than an order of magnitude improvement in the energy-delay product over the Si transistors. For the first time, we have demonstrated high performance enhancement and depletion mode InSb QWFETs with record fT of 305 and 256 GHz, respectively, at V_{DS} = 0.5V and scalability down to 85nm L_G.

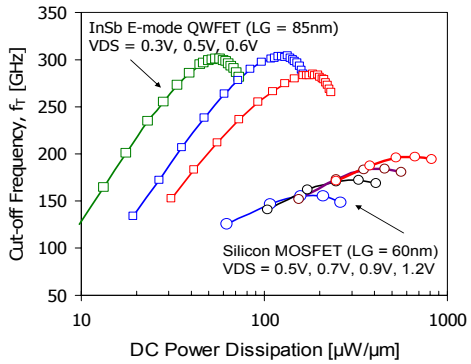

Fig. 14 Measured f_T vs DC power dissipation (normalized to the transistor width) for 85nm L_G InSb QWFETs and 60nm L_G silicon nMOS transistors

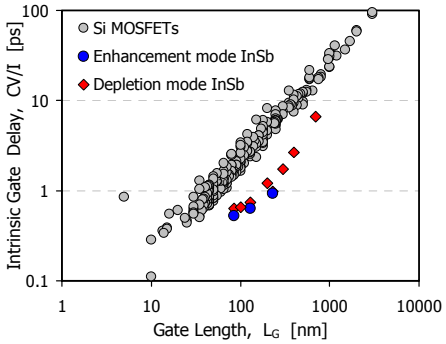

Fig. 15 Transistor Gate delay (CV/I) versus gate length for InSb QWFETs at V_{DS} = 0.5V benchmarked against state-of-the-art silicon nM OS transistors

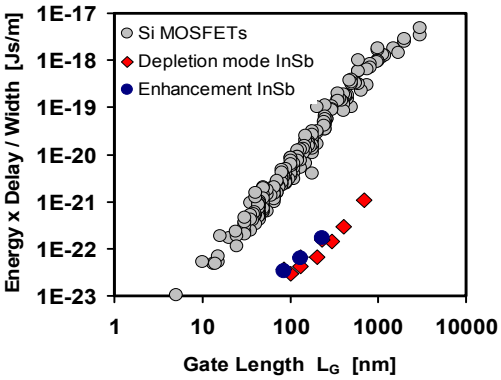

Fig. 16 Transistor Energy-Gate delay product (CV/I) versus gate length for InSb QWFETs at V_{DS} = 0.5V benchmarked against state-of-the-art silicon nM OS transistors

References

(1) T. Ashley et al,. Proc. 7th Intl. Solid State and Integrated Circuits Tech. Conf., Beijing, China, pp. 2253-2256, 2004

(2) T. Ashley et al., Proc. 2005 International Conference on Compound Semiconductor Manufacturing Technology, New Orleans, 2005

(3) R. Chau et al, IEEE Transactions on Nanotechnology, pp 153-158, 2005

(4) Z. Calahorra et al., J. Vac. Sc. Tech. B, pp 1195-1202, 1986