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99.1 % Efficient 10 kV SiC-Based Medium Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage

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***Abstract*—Due to their extremely high energy demand, data centers are directly supplied from a medium voltage (MV) grid. However, a significant part of this energy is dissipated in the power supply chain, since the MV is reduced step-by-step through multiple power conversion stages down to the chip voltage level. In order to increase the efficiency of the power supply chain, the number of conversion stages must be substantially reduced. In this context, Solid-State Transformers (SSTs) are considered as a possible solution as they could directly interface the MV AC grid to a 400 V DC bus, whereby server racks with a power consumption of several tens of kilowatts could be directly supplied from an individual SST. With a focus on the lowest system complexity, the SST ideally should be built as simple two-stage system consisting of an MV AC/DC PFC rectifier stage followed by an isolated DC/DC converter. Accordingly, this paper focuses on the design and realization of a 25 kW, 3.8 kV single-phase AC to 7 kV DC PFC rectifier unit based on 10 kV SiC MOSFETs. By simply adding an LC-circuit between the switch nodes of the well-known full-bridge-based PWM AC/DC rectifier, the integrated Triangular Current Mode (*i*TCM) concept is implemented, which only internally superimposes a large triangular current ripple on the AC mains current and therefore enables zero voltage switching (ZVS) over the entire AC mains period. Special attention is paid to the realization of the MV inductors and their electrical insulation, the AC-input LCL-filter to limit EMI emissions, and the challenges arising due to cable resonances when connecting the SST to the MV grid via a MV cable. Despite the large insulation distances required for MV, the realized 25 kW MV PFC rectifier achieves an unprecedented power density of 3.28 kW/L (54 W/in^3) and a full-load efficiency of 99.1 %, determined using a calorimetric measurement setup, which is discussed in detail in the Appendix.**

***Index Terms*—Medium-voltage, AC/DC, soft-switching, ZVS, 10 kV SiC MOSFETs, calorimetric measurement.**

I. Introduction

One of today's largest and fastest growing energy consumers is the information and communication technology (ICT) sector, which currently consumes 10 % of the world's generated electric energy [1]. Especially the continuous processing and provisioning of data by data centers is highly energy demanding. E.g. in 2014, the 14 million installed servers in the U.S. consumed 1.8 % of the national electric energy generation [2]. Furthermore, it is reported that 12 ... 27 % of the energy provided to data centers at medium voltage (MV) level is dissipated in the power conversion stages which convert the voltage from several kilovolts down to the chip voltage level [3]–[5]. Therefore, for economical and ecological reasons, the interest of research institutions and industry on more efficient data center power supplies has grown rapidly over the past decade. In order to increase the efficiency and to reduce the complexity (and therewith the probability of failure) of the conventional multi-stage power supply chain of data centers, a shift to a 380/400 V DC distribution system is considered [4] and partly already implemented [6]. As a next step, Solid-State Transformer (SST) technology is considered to provide a direct power electronic interface from the MV AC grid to 400 V DC, in order to improve the efficiency and the power density also of this part of the conversion chain [5], [7], [8]. Thereby, the power supply of each server rack (which can reach power demands in the range of 20 ... 40 kW, [3], [9], [10]) with a separate SST is intended. In this case, the power could be distributed on MV level (e.g. 6.6 kV phase-to-phase rms, i.e. 3.8 kV rms phase-to-neutral) with the advantage of substantially lower realization efforts and/or cable cross sections and lower ohmic losses compared to low-voltage(LV) distribution. Individual single-phase SSTs (single-phase for a low complexity) could then convert the MV into 400 V DC and feed individual server racks or clusters, whereby the three phases of the MV utility grid could be symmetrically loaded. For a cost-effective construction of the building, it would be important that the SSTs are compact and lightweight. For the

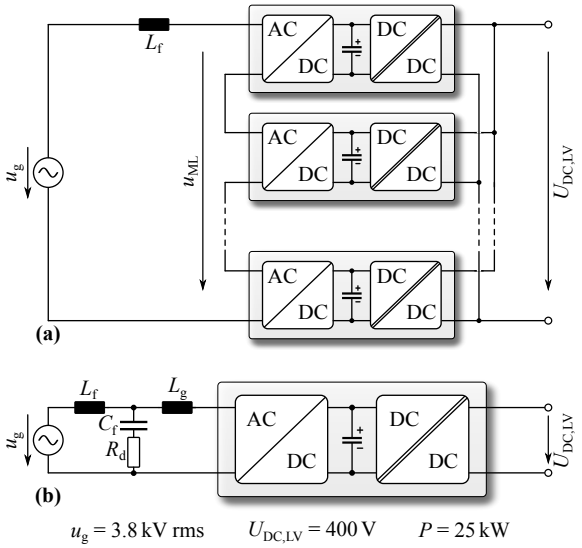

Fig. 1: (a) Multi-cell and **(b)** single-cell realization of a MV AC to 400 V DC SST.

sake of completeness, it should be mentioned that this kind of SST would also be well suited for high power battery charging in transportation applications [11], [12] and for the integration of renewable energy, e.g. photovoltaic power plants, into the MV grid [13].

Up to now, interfaces to the MV grid are typically built as multi-cell converters with an input-series output-parallel connection of multiple converter cells e.g. based on $1200\,\mathrm{V}\ldots1700\,\mathrm{V}$ SiC MOSFETs, i.e. wide bandgap devices with the highest blocking voltages commercially available at the moment. Thereby, the individual converter cells consist of a PFC AC/DC converter stage and a series-connected isolated DC/DC stage, as shown in **Fig. 1(a)**. In order to minimize the boost inductance, the AC/DC converters can be operated with phase-shifted carriers, resulting in a switched multi-level AC voltage u_{ML}, which closely follows the MV grid voltage u_{g}, and therefore leads to a small input current ripple. Such a system with a total power of $25\,\mathrm{kW}$ has been presented by industry in [14] and achieves a full-load efficiency of $96\,\%$ from $2.4\,\mathrm{kV}$ AC to $54\,\mathrm{V}$ DC. Even though multi-cell converters can achieve a high conversion performance, they are also highly complex due to the high number of switches, gate drivers, isolated auxiliary supplies, and voltage/current measurements.

As an alternative, with the new generation of $10\,\mathrm{kV}$ SiC MOSFETs, it is possible to interface the MV grid directly with a single-cell converter, consisting of a single-cell AC/DC PFC rectifier followed by an isolated single-cell DC/DC converter, as shown in **Fig. 1(b)**. The EMI noise injected into the MV grid is then limited by an additional LCL-filter in front of the PFC rectifier, which is a typical filter structure used for MV converters [15]. Due to the greatly reduced complexity compared to the multi-cell approach, a higher reliability and higher power density is expected. In order to prove this statement and to explore the limits in efficiency and power density of the single-cell approach, a bidirectional $25\,\mathrm{kW}$, $3.8\,\mathrm{kV}$ AC to $400\,\mathrm{V}$ DC SST with an intermediate $7\,\mathrm{kV}$ DC-link is realized, where the focus of this paper is on the AC/DC converter stage, the LCL-filter, and the challenges arising from interfacing the SST to the MV grid via a MV cable, which could be subject to undesired oscillations that need to be avoided by a termination network.

Due to the high blocking voltage of the utilized $10\,\mathrm{kV}$ SiC MOSFETs, a simple full-bridge-based PWM AC/DC converter topology is chosen. However, without further measures, hard-switching and thus high switching losses would occur [16]–[20]. Consequently, the achievable efficiency and power density would be strongly restricted, since the switching losses define an upper limit for the switching frequency, and hence inhibit a possible downsizing of passive components. The most effective strategy to reduce the switching losses is to apply soft-switching techniques and to profit from the typically much lower soft-switching losses compared to hard-switching. Additionally, EMI can be significantly reduced with soft-switching, since the $\mathrm{d}u/\mathrm{d}t$ values are typically much lower than for hard-switching.

Soft-switching can be achieved e.g. with the Triangular Current Mode (TCM) concept [21]–[24], where the boost inductance value is reduced to such extent, that the large high-frequency (HF) triangular current ripple superimposed to the instantaneous low-frequency (LF) grid current leads to a reversal of the current direction in the semiconductors in each switching cycle and accordingly enables zero-voltage switching (ZVS) for each switching transition, resulting in extremely low switching losses compared to hard-switching. On the other hand, however, with the TCM operation the boost inductor design becomes more challenging since both, the HF and the LF current, are flowing through the same inductor. In order to keep the HF losses in the inductor low, the employment of HF litz wire with thin strand diameter and HF core materials (e.g. ferrite) is necessary. Unfortunately, litz wire features a low copper filling factor and also the saturation flux density of HF core materials is typically low. However, in order to keep also the LF losses low, a winding with a high copper filling factor (i.e. solid copper wire) and a core material with a high saturation flux density (e.g. amorphous iron, iron powder or nanocrystalline core material) would be needed. Hence, with TCM operation, a reasonable trade-off between HF and LF losses has to be found in the design of the boost inductor.

In order to overcome this disadvantage, the concept of the *integrated* Triangular Current Mode (*i*TCM) operation is utilized for the realization of the considered $25\,\mathrm{kW}$, $3.8\,\mathrm{kV}$ single-phase AC to $7\,\mathrm{kV}$ DC converter [25], [26]. By adding an LC-circuit between the switch nodes of the full-bridge PWM AC/DC converter, the TCM current can be split into HF and LF current components, which are then flowing through two separate inductors, cf. **Fig. 2(a)**. A similar concept has been presented in [27] for high power density $400\,\mathrm{V}$ DC/DC applications. Advantageously, the large TCM ripple current then does not flow towards the grid (as usual for TCM topologies) but is kept internally in the circuit. Accordingly, this concept is called *integrated* Triangular Current Mode (*i*TCM). Since the superposition of HF and LF current, i.e. the TCM current, is only needed in the semiconductor devices to guarantee soft-switching, this current separation enables a dedicated design of the two inductors, i.e either optimized for LF or HF currents, and thus results in an expected efficiency improvement. A further advantage of the *i*TCM concept is, that the well-known PWM modulation scheme still can be applied and no additional control or measurement circuitry, e.g. current zero crossing detection as needed in TCM operation, is required.

This paper is organized as follows: **Section II** gives a brief overview over the *i*TCM converter topology and its modulation. In **Section III**, the design procedure of the individual components of the converter is presented. Special attention is paid to the design of MV inductors and their insulation, as well as the connection of the SST to the MV grid without exciting oscillations in the supplying MV cable. **Section IV** shows the experimental setup together with the experimental results, including waveforms and the calorimetrically measured converter efficiency and loss distribution. Finally, conclusions are drawn in **Section V** and a detailed explanation and error analysis of the applied calorimetric efficiency measurement methods is given in the **Appendix**.

II. The Integrated Triangular Current Mode (*i*TCM) Concept

The *i*TCM converter topology consists of a MOSFET full-bridge, an LCL-filter and the aforementioned LC-branch as shown in **Fig. 2(a)**. In order to not expose the AC-source (which could be e.g. a secondary winding of a MV transformer) to HF common mode (CM) voltages, the bridge leg $\{S_{21}, S_{22}\}$ is operated as unfolder with mains frequency, i.e. $50/60\,\mathrm{Hz}$, whereas the bridge leg $\{S_{11}, S_{12}\}$ is PWM modulated. However, the *i*TCM concept would also work in case both bridge legs would be PWM modulated. The corresponding duty cycles d_{HF} and d_{LF} of the HF and the LF bridge legs, respectively, are shown in **Fig. 2(c)**. Besides the mains input current i_{Lg} flowing through L_{g}, the LC-branch consisting of C_{b} and L_{b} now draws a triangular (inductive) HF current i_{b}, such that the sum of these currents i_{A}, which flows out of the switch node A, changes its sign during each switching cycle, enabling soft-switching as shown in **Fig. 2(b)**. Thereby, the task of the capacitor C_{b} is to block any LF AC current flow through L_{b}. The boost inductor L_{g} is dimensioned in such a way, that it carries only a small current ripple $\Delta i_{\mathrm{Lg,pp}}$, while the current ripple in L_{b} has to be chosen such that i_{A} reaches a negative value of at least $-I_{\mathrm{ZVS}}$ in the corresponding switching transitions, in order to guarantee soft-switching over the whole mains period. Thereby, the current I_{ZVS} is the desired turn-off current of the HF bridge leg which can be calculated based on the effective output charge Q_{OSS} of the switching devices required to charge/discharge the output capacitances C_{OSS} of the power MOSFETs (and further parasitic capacitances), and the maximum allowed duration of this resonant switching transition (i.e. the dead time duration T_{dt}), which also defines the minimum and maximum duty cycles of the converter [24]. Hence, in order not to limit the duty cycle range and/or to be able to control the input/output voltage in a wide range, T_{dt} has to be small, e.g. $k = 1\,\%$ of the switching period T_{p}. The minimum required current I_{ZVS} can roughly be calculated as

$$I_{\mathrm{ZVS}} = Q_{\mathrm{OSS}}/T_{\mathrm{dt}} = Q_{\mathrm{OSS}}/\left(k \cdot T_{\mathrm{p}}\right). \tag{1}$$

The critical point, where the highest current in L_{b} is needed, is located at the peak of the mains current. The inductance values of L_{b} and L_{g} can be dimensioned in such a way that a turn-off current of $-I_{\mathrm{ZVS}}$ is achieved in this operating point. However, the goal is to achieve a constant ZVS current over the whole mains period to reduce the rms current in the LC-branch and the MOSFETs, which is not possible when the switching frequency is kept constant [25]. Therefore, the switching frequency has to be varied within the mains period, whereby a minimum switching frequency f_{min} is defined at the peak of the mains current and is set to $f_{\mathrm{min}} = 35\,\mathrm{kHz}$ for the converter at hand (cf. **Fig. 2(d)**). With the known minimum switching frequency and the purpose of achieving a turn-off current of $-I_{\mathrm{ZVS}}$ at the peak of the mains current, the inductance of L_{b} can be calculated as a function of the peak-to-peak current ripple r (in % of the peak mains current)

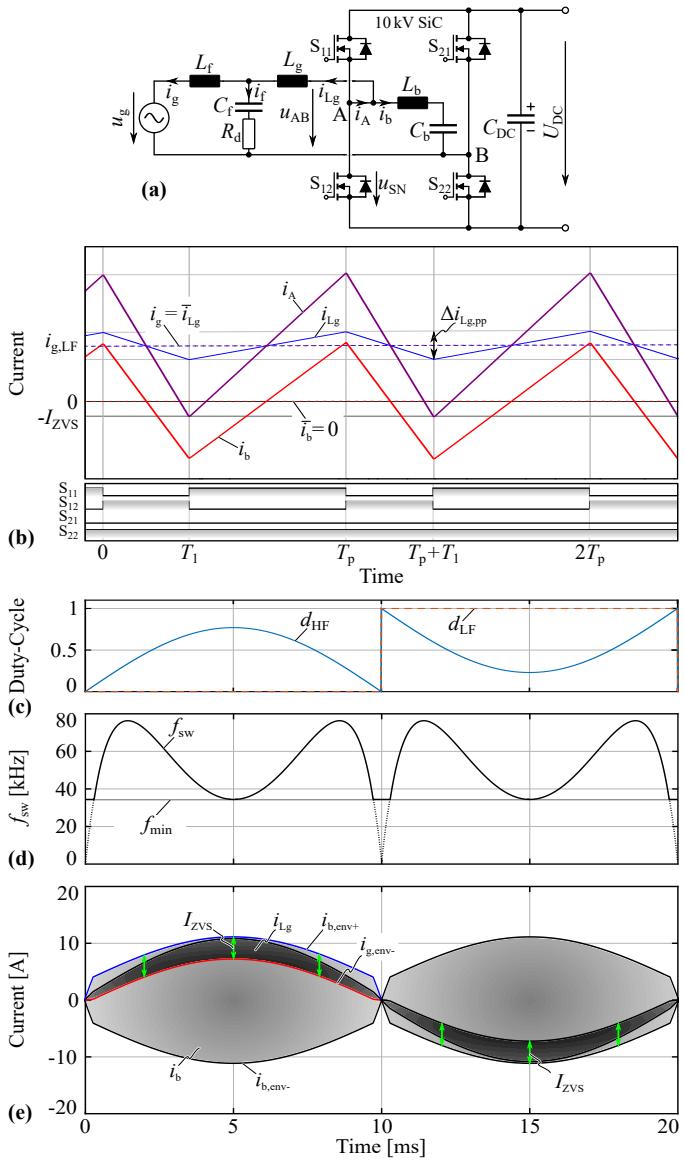

Fig. 2: **(a)** Circuit diagram of the MV PFC rectifier with AC-side LCL-filter and additonal LC-branch consisting of L_{b} and C_{b} to implement the *integrated* TCM operation, which enables soft-switching over the entire AC mains period. **(b)** Detailed view of the inductor current waveforms i_{b} and i_{Lg} together with the current $i_{\mathrm{A}} = i_{\mathrm{b}} + i_{\mathrm{Lg}}$ flowing out of the HF bridge leg $\{S_{11}, S_{12}\}$. **(c)** Duty cycles d_{HF} and d_{LF} of the HF and LF bridge legs. **(d)** Variable switching frequency f_{sw} required to guarantee a constant ZVS current. **(e)** Envelopes of the currents i_{b} and i_{Lg} over a mains period.

in the boost inductor L_{g} as

$$L_{\mathrm{b}} = \frac{\hat{u}_{\mathrm{g}}^2}{2P\left(2-r\right) + 2I_{\mathrm{ZVS}}\hat{u}_{\mathrm{g}}} \left(1 - \frac{\hat{u}_{\mathrm{g}}}{U_{\mathrm{DC}}}\right) \frac{1}{f_{\mathrm{min}}}, \tag{2}$$

whereby $\hat{u}_{\mathrm{g}}$ denotes the peak AC grid voltage ($\hat{u}_{\mathrm{g}} = \sqrt{2} \cdot u_{\mathrm{g}}$), U_{DC} denotes the DC-link voltage, and P denotes the system power. Furthermore, the inductance of the boost inductor L_{g}, dimensioned for a maximum current ripple r, can be found as

$$L_{\mathrm{g}} = \frac{\hat{u}_{\mathrm{g}}^2}{2r f_{\mathrm{min}} P} \left(1 - \frac{\hat{u}_{\mathrm{g}}}{U_{\mathrm{DC}}}\right). \tag{3}$$

The condition of a constant ZVS current I_{ZVS} can be visualized e.g. during the positive half-cycle of the mains period as

the difference of the upper envelope $i_{\mathrm{b,env+}}$ of the current in L_b and the lower envelope $i_{\mathrm{g,env-}}$ of the current in L_g, as shown in **Fig. 2(e)** (if an offset-free current i_b is assumed, i.e. $i_{\mathrm{b,env+}} = -i_{\mathrm{b,env-}}$). The function to describe the variable switching frequency to achieve a constant ZVS current (derived in more detail in [25]) can be found as

$$f_\mathrm{sw} = \frac{A\left(t\right)\hat{u}_\mathrm{g}^2}{4P\left|\sin\left(\omega_\mathrm{g}t\right)\right| + 2\hat{u}_\mathrm{g}I_\mathrm{ZVS}} \cdot \left(\frac{1}{L_\mathrm{g}} + \frac{1}{L_\mathrm{b}}\right), \tag{4}$$

whereby

$$A\left(t\right) = \left|\sin\left(\omega_\mathrm{g}t\right)\right| \cdot \left[1 - \frac{\hat{u}_\mathrm{g}}{U_\mathrm{DC}} \cdot \left|\sin\left(\omega_\mathrm{g}t\right)\right|\right]. \tag{5}$$

However, this function holds only for an LF current which is in phase with the grid voltage (i.e. a pure sine current in this case). Due to the capacitors C_b and C_f (as well as C_t which will be introduced in Section III-G), the converter has to deliver a small amount of reactive power, i.e. small LF cosine currents are superimposed on the inductor currents i_b and i_Lg. In order to still maintain a constant ZVS current, this deviation from the ideal waveforms has to be compensated by the switching frequency,

$$f_\mathrm{sw} = \left(\frac{1}{L_\mathrm{g}} + \frac{1}{L_\mathrm{b}}\right) \cdot \frac{A\left(t\right)\hat{u}_\mathrm{g}^2}{4P\left|\sin\left(\omega_\mathrm{g}t\right)\right| + 2\left(\hat{u}_\mathrm{g}I_\mathrm{ZVS} + \hat{u}_\mathrm{g}^2\omega_\mathrm{g}C_\mathrm{equ} \cdot \cos\left(\omega_\mathrm{g}t\right)\right)}, \tag{6}$$

whereby $C_\mathrm{equ} = C_\mathrm{b} + C_\mathrm{f}$ is the equivalent capacitance causing the LF cosine current. **Fig. 3** shows the simulated current waveforms for a peak-to-peak ripple of $r = 40\,\%$ in L_g together with the adapted switching frequency pattern, whereby the capacitors C_b and C_f are taken into account. As can be seen, the LF current $i_{\mathrm{f,50\,Hz}}$ causes a slight phase-shift between the grid current i_g and the boost inductor current i_Lg. Nevertheless, with the adapted switching frequency pattern, the turn-off current I_ZVS can be kept constant, as can be seen in the envelope of the current $i_\mathrm{A} = i_\mathrm{b} + i_\mathrm{Lg}$ flowing out of the HF bridge leg.

It should be noted that the maximum switching frequency increases with increasing reactive power, i.e. for excessive reactive power levels, ZVS might be lost if e.g. due to efficiency reasons an upper limit for the maximum switching frequency is defined. The converter at hand is designed to handle reactive powers of approximately $\pm 30\,\%$ of the nominal power. Nevertheless, compared to the conventional hard-switched PWM topology with a constant switching frequency of $10\,\mathrm{kHz}$, with the *i*TCM concept, the semiconductor losses can be significantly reduced, while at the same time the average switching frequency is increased by more than a factor of five, resulting in both, a higher efficiency and a higher power density [25].

III. System Design

In the following, the design of the individual components of the converter is presented, whereby **TABLE I** summarizes the specifications of the system as a basis for the design process.

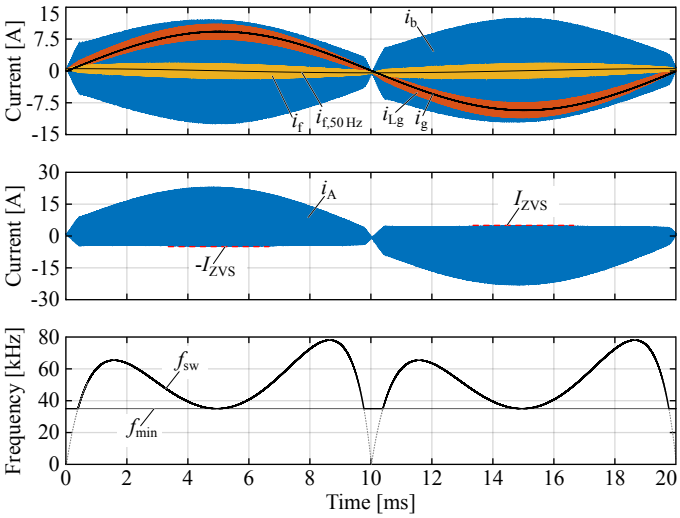

Fig. 3: Ideal current waveforms of the *i*TCM converter considering the capacitive line-frequency currents through C_b and C_f which cause a slight asymmetry of the current ripples in L_b and L_g. In order to maintain a constant turn-off current (as can be seen in the current i_A), the switching frequency pattern becomes asymmetric within one mains half-period.

TABLE I: System Specifications.

Parameter	Value	Parameter	Value
P	25 kW	f_min	35 kHz
U_AC	3.8 kV rms	I_ZVS	4.5 A
U_DC	7 kV	f_g	50 Hz

A. General MV SiC-Based Converter Design Considerations

In the following analysis, the *i*TCM converter with its DC-link voltage of 7 kV and its power rating of 25 kW is compared to a 400 V system with the same power rating, in order to point out an important fundamental difference between the design of MV converters and LV converters regarding parasitic inductances and capacitances.

For each power electronic converter, a switching impedance, i.e. the ratio between the switched voltage and the switched current can be defined [28]:

$$Z_\mathrm{sw} = U_\mathrm{DC}/I_\mathrm{L}. \tag{7}$$

This switching impedance is a useful quantity to analyze the impact of parasitics on the switching behavior of a bridge leg. For the analysis of the impact of parasitic inductances, the schematic and the idealized waveforms given in **Fig. 4(a)** are considered. If the low-side MOSFET turns off the current I_L in a fixed switching time t_s, a certain voltage u_σ is induced across the parasitic commutation loop inductance L_σ, which represents the sum of the MOSFET package inductances, the PCB inductances, and the parasitic inductance of the DC-link capacitor. This induced voltage is superimposed on the low-side switch voltage u_S and causes a voltage overshoot, as shown in **Fig. 4(a)**. If the impedance of the parasitic commutation loop inductance L_σ is in the same order of magnitude as the switching impedance Z_sw, the magnitude of the voltage overshoot across the switch is for its part in the same order of magnitude as the switched voltage. Consequently, to limit the voltage overshoot to a certain value, e.g. $k_\mathrm{u} = 10\,\%$ of the DC-link voltage, an upper limit for the

value of L_σ can be defined. The induced voltage overshoot and the limiting condition can be expressed as

$$u_\sigma = L_\sigma \frac{I_\mathrm{L}}{t_\mathrm{s}} \leq k_\mathrm{u} \cdot U_\mathrm{DC}. \tag{8}$$

Reformulating this equation by using (7) results in the maximum allowed commutation loop inductance L_σ that leads to the given voltage overshoot in dependency of the switching impedance Z_sw and the switching time t_s:

$$L_\sigma \leq k_\mathrm{u} \cdot t_\mathrm{s} \cdot Z_\mathrm{sw}. \tag{9}$$

To show the difference between a MV and a LV converter from a parasitics point of view, the switching impedance of the *i*TCM converter at hand and the switching impedance of a similar converter with $400\,\mathrm{V}$ DC-link voltage are calculated. While the $7\,\mathrm{kV}$ system shows a switching impedance of

$$Z_\mathrm{sw,7kV} = 7\,\mathrm{kV}/22.5\,\mathrm{A} = 311\,\Omega \tag{10}$$

(in case of an AC/DC converter the maximum switched current is considered and can be read off in **Fig. 3**), the $400\,\mathrm{V}$ system would show a switching impedance of

$$Z_\mathrm{sw,400V} = \left(\frac{400\,\mathrm{V}}{7\,\mathrm{kV}}\right)^2 \cdot Z_\mathrm{sw,7kV} \approx 1\,\Omega. \tag{11}$$

Furthermore, for the $7\,\mathrm{kV}$ converter, the typical switching time of a $10\,\mathrm{kV}$ SiC MOSFET bridge leg is between $t_\mathrm{s} = 100\,\mathrm{ns}$ and $t_\mathrm{s} = 500\,\mathrm{ns}$ [29], while typical switching times for a $400\,\mathrm{V}$ converter are in the range of $t_\mathrm{s} = 10\,\mathrm{ns}$ and $t_\mathrm{s} = 50\,\mathrm{ns}$.

The graph in **Fig. 4(a)** shows the impact of Z_sw on L_σ for the aforementioned switching times and $k_\mathrm{u} = 0.1$. Furthermore, the impedances $Z_\mathrm{sw,400V}$ and $Z_\mathrm{sw,7kV}$ are indicated with a blue and a red line, respectively. As can be seen, the allowed commutation loop inductance for a $400\,\mathrm{V}$ system has to be kept very low in the range of $1\ldots5\,\mathrm{nH}$, i.e. the parasitic inductances of the MOSFET packages, the DC-link capacitor, and the circuit layout have to be minimized [27]. In contrast, the allowed commutation loop inductance for the $7\,\mathrm{kV}$ converter at hand is in the range of $3\ldots15\,\mu\mathrm{H}$. This means that the PCB and busbar inductances as well as the parasitic MOSFET package inductances (apart from the gate loop inductance, which is not affected by these considerations and should always be minimized) are relatively uncritical for this particular converter due to its high impedance or in other words due to its relatively low power considering the high input and output voltages.

A similar analysis can be conducted in order to demonstrate the impact of parasitic capacitances that are (schematic-wise) connected between the switch node of the bridge leg and ground, as shown representatively in form of C_p in the schematic in **Fig. 4(b)**. Such capacitances are, besides the nonlinear output capacitances C_OSS of the MOSFETs, e.g. parasitic capacitances from the MOSFET chips to the heat sink, parasitic capacitances of inductive components connected to the switch node, and also the coupling capacitance of the high-side gate driver supply and signal transmission. If an ideal switching transition is assumed again, i.e. the DC-link voltage U_DC is switched within the time t_s, as shown in the waveforms in **Fig. 4(b)**, the voltage slope across the parasitic capacitance

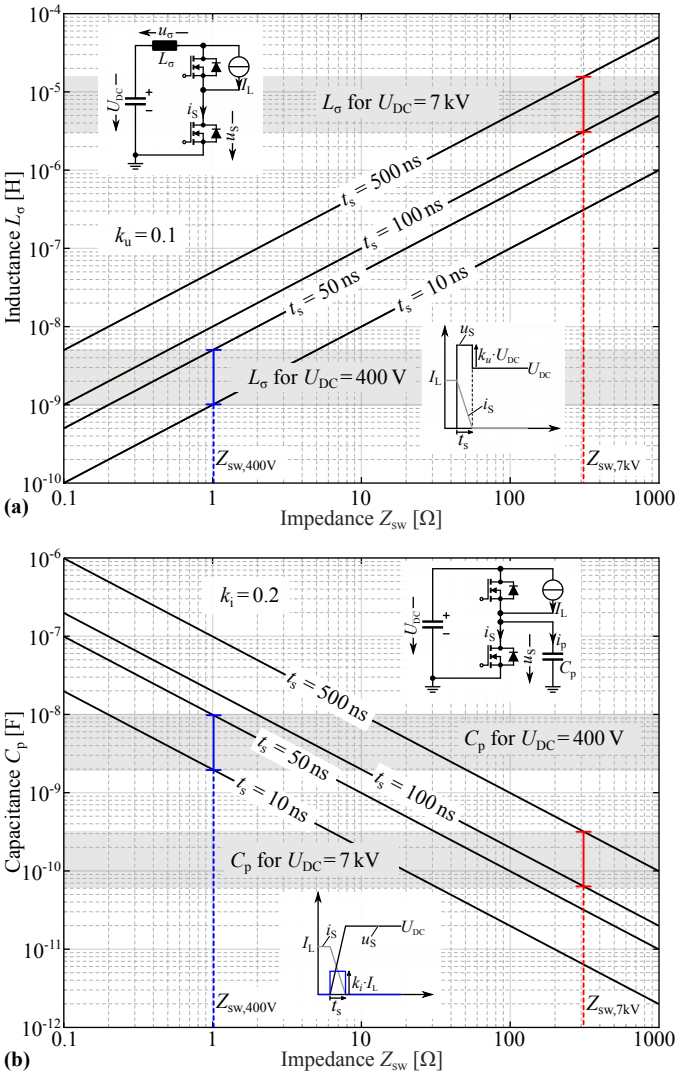

Fig. 4: **(a)** Highest allowed inductance L_σ in the commutation path for a maximum allowed voltage overshoot of $k_\mathrm{u} = 10\,\%$ of the switched voltage U_DC in dependency of the switching impedance Z_sw and the switching time t_s. A constant $\mathrm{d}i/\mathrm{d}t$ is assumed. **(b)** Highest allowed parasitic capacitance C_p connected to the switch node for a maximum capacitive current of $k_\mathrm{i} = 20\,\%$ of the switched current I_L in dependency of the switching impedance Z_sw and the switching time t_s. A constant $\mathrm{d}u/\mathrm{d}t$ is assumed. The typical switching speeds ($10\ldots100\,\mathrm{ns}$ for LV devices and $100\ldots500\,\mathrm{ns}$ for MV SiC devices) as well as the switching impedances $Z_\mathrm{sw,400V}$ and $Z_\mathrm{sw,7kV}$, and the resulting inductance/capacitance ranges are highlighted.

C_p causes a certain current i_p and in case the impedance of C_p is in the same order of magnitude as the switching impedance Z_sw, the magnitude of i_p is in the same range as the switched current I_L. However, for a proper operation of the converter and to reduce EMI, this capacitive current should be limited to e.g. $k_\mathrm{i} = 20\,\%$ of the switched current, which leads to

$$i_\mathrm{p} = C_\mathrm{p} \frac{U_\mathrm{DC}}{t_\mathrm{s}} \leq k_\mathrm{i} \cdot I_\mathrm{L}. \tag{12}$$

By inserting (7) in this equation, the highest allowed parasitic capacitance C_p, which leads to the defined maximum capacitive current, is given in dependency on the switching impedance Z_sw and the switching time t_s as

$$C_\mathrm{p} \leq \frac{k_\mathrm{i} \cdot t_\mathrm{s}}{Z_\mathrm{sw}}. \tag{13}$$

The limits for the parasitic capacitance C_p are shown in **Fig. 4(b)**, again for the typical switching speeds for a $400\,\mathrm{V}$ system ($t_\mathrm{s} = 10\,\mathrm{ns} \ldots t_\mathrm{s} = 50\,\mathrm{ns}$) and the $7\,\mathrm{kV}$ system ($t_\mathrm{s} = 100\,\mathrm{ns} \ldots t_\mathrm{s} = 500\,\mathrm{ns}$). As can be seen (blue line), a rather high capacitance in the range of $2 \ldots 10\,\mathrm{nF}$ can be allowed for the $400\,\mathrm{V}$ system, and therefore parasitic capacitances are mostly uncritical for LV applications (apart from an increased CM filter effort).

However, considering the $7\,\mathrm{kV}$ converter (red line), the maximum allowed capacitance is only in the range between $65\,\mathrm{pF}$ and $320\,\mathrm{pF}$, which is a factor of 30 less than in case of a $400\,\mathrm{V}$ converter. Consequently, it is very important to design the MV converter with the goal to minimize parasitic capacitances, whereas parasitic inductances play a minor role as shown above. E.g. for the PCB design, this means that coplanar tracks or coplanar polygons must be avoided (also due to the fact that the PCB material would hardly be able to reliably insulate the high voltages). Instead, PCB tracks on jumping potential should be separated from other potentials as far as possible in order to minimize parasitic capacitances.

B. Inductor Design

As already mentioned, the triangular current i_A flowing through the full-bridge is the sum of the currents in the inductors L_b and L_g (as shown in **Fig. 2 (a) & (b)**), which in total has to reach a certain value $-I_\mathrm{ZVS}$ at the turn-off switching instant to guarantee soft-switching of the MOSFETs. However, the sharing of the required current ripple among the two currents i_b and i_g to achieve $-I_\mathrm{ZVS}$ is a free parameter, which can be optimized e.g. regarding power density and losses of the two inductors. A priori, it is not clear whether a high or a rather low current ripple in L_g leads to the smallest overall volume and losses. Therefore, optimizations of the inductors L_b and L_g regarding power density and losses have been carried out with an arbitrary sweep over the following parameters:

- peak-to-peak ripple r in L_g;
- core dimensions;
- ferrite, amorphous, and nanocrystalline core material;
- number of turns;
- litz wire / solid wire diameter;
- strand diameter,

whereby the insulation distances between the winding and the core are fixed (cf. Section III-B2).

The results of the optimization indicate that the best L_b designs consist of a ferrite core material with HF litz wire windings, as expected for a pure HF AC flux. On the other hand, however, the best L_g designs utilize nanocrystalline core material and also HF litz wire windings but with a rather thick strand diameter. Due to the HF ripple and the high switching frequency, solid copper wire is subject to relatively high HF losses (mainly due to the fringing field of the air gap) and therefore inferior to HF litz wire. **Fig. 5(a)** shows the Pareto fronts of the optimization results for inductor L_b, whereby the labels depict the peak-to-peak current ripple r in L_g which is set between $20\,\%$ and $80\,\%$ of the peak grid current. As can be seen, the current ripple r has almost no influence on the

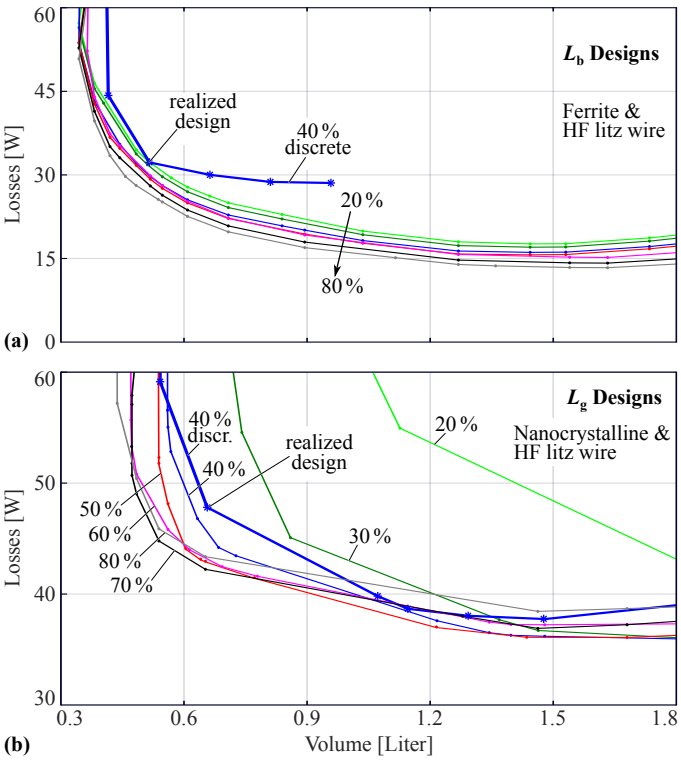

Fig. 5: Volume/loss optimization of the inductor L_b **(a)** and L_g **(b)** for different peak-to-peak current ripples in L_g (referenced to the peak mains current). The core size, the litz wire, and the strand diameter are freely swept, in order to explore the theoretical limits. The curves marked with '40 % discrete' show designs with discrete available cores and litz wires for a $40\,\%$ peak-to-peak current ripple in L_g.

inductor losses and volume, which is why the Pareto fronts for different ripples are very close to each other. This can be explained by the fact that the peak current in L_b, which is given as $\hat{i}_\mathrm{Lb} = \frac{P}{U_\mathrm{g}} \cdot \sqrt{2} - \Delta i_\mathrm{Lg,pp}/2 + I_\mathrm{ZVS}$, decreases only from $12.9\,\mathrm{A}$ to $10.1\,\mathrm{A}$ when the ripple in the other inductor L_g is increased from $20\,\%$ to $80\,\%$. This means that it is possible to find a good design of L_b for any current ripple $\Delta i_\mathrm{Lg,pp}$ in L_g between $20\,\%$ to $80\,\%$, whereby designs with higher ripples in L_g are slightly beneficial.

As shown in the optimization results for inductor L_g in **Fig. 5(b)**, a clear trend towards more efficient and more compact designs can be seen for an increasing current ripple in L_g (also observed in [30]). From this perspective, a large current ripple in L_g would be beneficial in terms of power density and efficiency of both inductors L_b and L_g. However, a large current ripple in L_g would also result in a higher filtering effort and therefore in an increased size of the remaining input filter components C_f and L_f of the LCL-filter. E.g. a current ripple of $r > 200\,\%$ would actually mean usual TCM operation (i.e. the LC-branch would not be needed any more), but therefore, the full triangular current ripple would flow towards the MV grid and has to be attenuated by $C_\mathrm{f}/L_\mathrm{f}$ or even an additional filter stage to obtain a smooth grid current. The opposite extreme, i.e. a very small current ripple of $r \leq 5\,\%$ would lead to a very high inductance value L_g and therefore to a large volume of L_g. As a trade-off, a current ripple in L_g of $r = 40\,\%$ peak-to-peak is selected, since the $40\,\%$ Pareto

TABLE II: Realized inductors L_b and L_g.

Ind.	Type	Core mat.	Core	Turns	HF litz
L_b	E-core	Ferrite N87	3xE65	3x17	270x0.071 mm
L_g	C-core	Finemet	4xF3CC-25	4x29	150x0.1 mm

front shows a much better performance than the designs with 20 % and 30 % current ripple, and at the same time it is only slightly worse than the 50 % to 80 % Pareto fronts (+15 % only in volume and losses compared to the Pareto optimal designs). With the selected ripple in L_g of $r = 40\,\%$, the inductance values of L_b and L_g can be calculated with (2) and (3). For the system at hand, the values are $L_\mathrm{b} = 1.49\,\mathrm{mH}$ and $L_\mathrm{g} = 9.55\,\mathrm{mH}$.

For the realization of the inductors L_b and L_g, discrete designs with available core shapes and HF litz wire have to be determined. Therefore, instead of a continuous optimization sweep, an optimization with available core shapes and available HF litz wires has been carried out for a ripple of $r = 40\,\%$. The results for discrete L_b and L_g designs are shown in **Fig. 5(a)** and **(b)**, respectively. It can be seen that the discrete designs come very close to the designs with freely swept parameters. Both of the chosen designs are located in the bend of the Pareto fronts, i.e. they represent the best compromise between low volume and low losses. **TABLE II** lists the parameters of the realized inductors.

1) Inductor Voltage Stresses: For the design of the electrical insulation of the two inductors L_b and L_g, the voltage stresses between their terminals, as well as the voltage stresses between each of their terminals and ground have to be determined in a first step. However, since the voltage stresses of L_b and L_g are equal, the analysis is only carried out for L_b. Therefore, **Figs. 6(a)** and **(c)** show the possible arrangements of L_b and C_b between the HF switch node A and the LF switch node B of the full bridge from the *i*TCM topology shown in **Fig. 2(a)**. Although L_b and C_b are connected in series in both cases (forming the midpoint T), there is a significant difference in the terminal voltage stress u_T of L_b depending on whether L_b is connected to switch node A or B. In practice, the voltage u_T will be applied between one terminal of L_b and its ferrite core, which is typically tied to ground potential. Therefore, the electrical insulation between the core and the winding has to be designed accordingly and it is important to choose the configuration which leads to the lowest terminal voltage stress in order to minimize the occurring electrical fields and the insulation effort. Since L_b and C_b form an LC-filter, the voltage u_Cb across C_b is (apart from the small HF ripple) equal to the averaged PWM voltage, i.e. the grid voltage u_g. Consequently, the terminal voltage u_T for the configuration shown in **Fig. 6(a)** can easily be identified as $u_\mathrm{T} = u_\mathrm{Cb} + u_\mathrm{rec}$ and is shown in **Fig. 6(b)**. Since the LF bridge leg is switched at the zero crossing of u_Cb, u_T is always positive and does not exceed the DC-link voltage of $U_\mathrm{DC} = 7\,\mathrm{kV}$. However, the terminal voltage u_T in the configuration shown in **Fig. 6(c)** is now the difference of the HF switch node voltage u_SN and the line-frequency capacitor voltage u_Cb, i.e. $u_\mathrm{T} = u_\mathrm{SN} - u_\mathrm{Cb}$. As can be seen in **Fig. 6(d)**, u_T reaches a peak value of $U_\mathrm{DC} + \hat{u}_\mathrm{g} = 7\,\mathrm{kV} + 5.4\,\mathrm{kV} = 12.4\,\mathrm{kV}$ which is almost

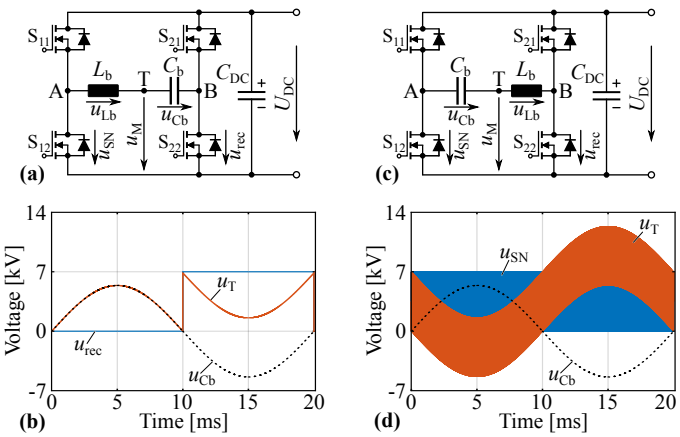

Fig. 6: The two possible arrangements of L_b and C_b between the HF bridge leg (switch node A) and the LF rectifier bridge leg (switch node B) in **(a)** and **(b)**, together with the respective terminal voltages u_T in **(c)** and **(d)**.

twice the maximum value achieved in the configuration from **Fig. 6(a)**. Hence, inductor L_b must be connected to the switch node of the HF bridge leg in order to minimize its terminal voltage stess. Furthermore, it is directly evident from the schematic that the differential mode (DM) voltage u_Lb does not exceed U_DC. For this reason, both the terminal and the DM voltage stresses of L_b and L_g are below or equal to $U_\mathrm{DC} = 7\,\mathrm{kV}$. In order to guarantee its functionality also in case of any undesired overvoltages, the terminal and the DM insulations are designed for 15 kV.

2) Winding Arrangement: In order to achieve soft-switching of the MOSFETs over the entire grid period, the output capacitances of the MOSFETs have to be charged and discharged in each switching transition. According to equation (1), the ZVS current is proportional to the charge in the nonlinear parasitic output capacitances of the commutating bridge leg. However, any additional capacitances, such as the layer-to-layer or winding-to-core capacitances of the inductors L_b and L_g connected to the switch node, also have to be charged and discharged in each switching transition, slowing down the rise and fall times. Therefore, besides the proper electrical insulation, it is also important to minimize the parasitic capacitances of the inductors. From the inductor optimization, the number of layers and the number of turns for L_b and L_g is already given. However, the arrangement of the windings within the winding window can be optimized for low parasitic capacitances. **Fig. 7** shows the electric field distribution (obtained from a FEM simulation) of four different winding arrangements of L_b in combination with the list of the corresponding parasitic capacitances C_CM (winding to core capacitance), C_DM (terminal to terminal capacitance), and the total capacitance $C_\mathrm{tot} = C_\mathrm{CM} + C_\mathrm{DM}$. As can be seen, the CM capacitance C_CM stays constant, independently of the winding arrangement. However, with a multi-chamber arrangement (cf. **Fig. 7(b)-(d)**), the DM capacitance C_DM can be reduced by more than a factor of three compared to the single-chamber winding. However, comparing the total capacitance C_tot of the multi-chamber arrangements, the arrangements in **Fig. 7(c) & (d)** do not show significantly reduced capacitances compared to the arrangement shown in **Fig. 7(b)**, while being much

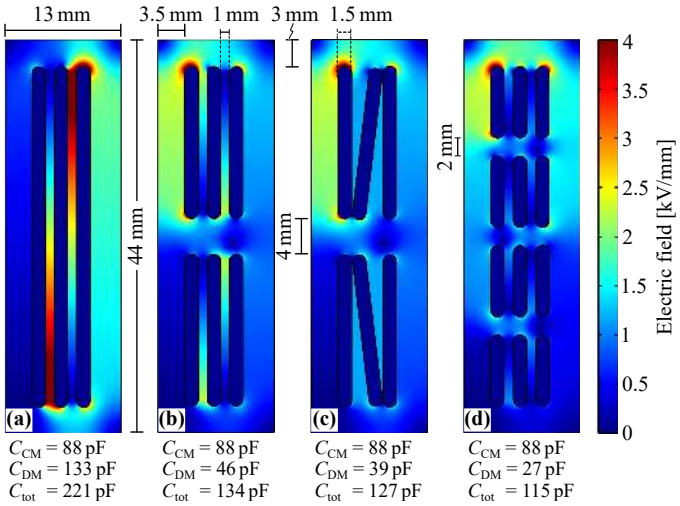

Fig. 7: Electric field distribution in the winding window of the inductor L_b for different winding arrangements. **(a)** Three-layer single-chamber winding; **(b)** Three-layer two-chamber winding; **(c)** Three-layer two-chamber conical winding; **(d)** Three-layer four-chamber winding.

more complicated in construction. Hence, the arrangement in **Fig. 7(b)** is selected for the final realization of L_b. Inductor L_g is realized with a four-layer, two-chamber winding for the same reasons. Furthermore, the insulation distances between the layers, the chambers, and to the core are given in **Fig. 7(b)**. The maximum electric field strength is $4\,\mathrm{kV/mm}$ (for $7\,\mathrm{kV}$ DM voltage), which is well below the $24\,\mathrm{kV/mm}$ breakdown field strength of the utilized silicone in order to be able to handle overvoltages during fault conditions and to guarantee a high reliability of the MV converter.

3) Selection & Application of the Insulation Material: Usually, epoxy resins are used for the dry-type insulation of inductors and transformers in power electronic converters. In state-of-the-art MV converters, the typical switching frequencies are in the lower kHz range due to the significant switching losses of MV IGBTs, GTOs or even hard-switched MV SiC devices [17]. However, with the new generation of $10\,\mathrm{kV}$ and $15\,\mathrm{kV}$ SiC MOSFETs combined with soft-switching techniques, switching frequencies in the range of $75\,\mathrm{kHz}$, as demonstrated in this paper, are possible. Therefore, the dielectric losses $P_\mathrm{ins} \propto E^2 \cdot f_\mathrm{sw} \cdot \tan\delta$ of the insulation material start playing a role [31]. Additionally, the winding losses have to be extracted through the rather thick insulation material layer, which completely surrounds the winding. Consequently, an insulation material with a high thermal conductivity, a low dissipation factor $\tan\delta$, and a high electric breakdown field strength is required. Unfortunately, the thermal conductivity of epoxy resins is rather low. Therefore, a two-component silicone compound (containing thermally conductive particles) of type *TC-4605 HLV* from Dow Corning is used. The properties of this material are listed in **TABLE III**. An additional advantage compared to epoxy resin is the mechanical flexibility of the silicone, which prevents it from cracking during the curing process.

Besides the advantages of the utilized silicone, its curing process is highly sensitive to other materials such as amines, amides, nitriles, and alcohols, among others. These substances, which might be contained e.g. in adhesives used during the construction of the winding, act as cure inhibitors. Consequently, the silicone will not cure properly, preventing it from developing its dielectric properties [32]. Hence, it is advised to test the compatibility of the silicone and any materials contained in the winding package before constructing the winding. For example, it has been found that cyanoacrylate-based instant adhesives and UV adhesives prevent the silicone from curing. However, two-component instant adhesives, such as *LOCTITE 3090*, for example, have been tested and were used successfully.

In order to attain a cavity-free insulation, a vacuum pressure potting (VPP) process is applied. Thereby, the devolatilized silicone is pressed into the 3D-printed coil former under vacuum (not lower than $30\,\mathrm{mbar}$ in order to not vaporize any ingredients of the silicone). After the coil former is completely filled, the pressure is slowly increased to atmospheric pressure, compressing possible vacuum cavities. In a second step, the silicone has to be cured for several hours with a temperature of $120\,^\circ\mathrm{C}$ in order to activate the adhesion to other materials. The best results regarding adhesion are achieved when the temperature is applied directly after the VPP process, although the curing itself does not require an increased temperature. However, if the temperature is only applied after the curing at room temperature, the silicone might detach from the coil former, leading to vacuum or air cavities between coil former and silicone, which are undesired considering insulation aspects.

C. Dimensioning of the Capacitor C_b

The capacitor C_b in series to L_b is needed to block any LF AC or DC current flowing through the LC-branch. Since for low frequencies C_b is quasi connected in parallel to the grid (the impedance of the inductors is negligible at the mains frequency), C_b leads to an additional reactive power consumption from the AC grid, resulting also in an asymmetric switching frequency pattern, as already mentioned. For this reason, and to minimize the volume of C_b, the capacitance value should be kept small. On the other hand, in order to achieve soft-switching, a certain minimum inductive current through the LC-branch is required. Consequently, the capacitance of C_b has to be selected sufficiently large such that the capacitor voltage ripple stays small, or in other words, the LC-resonance frequency has to be well below the switching frequency range. A selection of the resonance frequency too close to the minimum switching frequency would cause a deviation from a purely inductive behavior, since the impedance of C_b would be in a similar range as the one of L_b. Therefore, the influence of the capacitor C_b on the current amplitude should

TABLE III: Properties of the utilized silicone *Dow Corning TC-4605 HLV*.

Property	Value
Dielectric strength	$24\,\mathrm{kV/mm}$
Dielectric constant ε_r	< 4.1 for $f > 50\,\mathrm{kHz}$
Dissipation factor $\tan\delta$	$< 0.8\,\%$ for $f > 50\,\mathrm{kHz}$
Thermal conductivity	$1\,\mathrm{W/(m\,K)}$

be kept small such that I_{ZVS} is not changed by more than e.g. $d_{\mathrm{IZVS}} = 10\,\%$.

$$C_{\mathrm{b}} \geq \frac{\hat{i}_{\mathrm{b}}}{4\pi^2 f_{\mathrm{sw,min}}^2 L_{\mathrm{b}} I_{\mathrm{ZVS}} \cdot d_{\mathrm{IZVS}}} \tag{14}$$

With the design equation (14) derived in [25], a minimum value of $C_{\mathrm{b}} \geq 184\,\mathrm{nF}$ can be found, while the (HF) rms current flowing through the LC-branch is $i_{\mathrm{b,rms}} = 5.3\,\mathrm{A}$. Thus, for practical reasons (sufficient current carrying capacity and appropriate voltage rating), a series connection of four $1\,\mu\mathrm{F}$ film capacitors is used, resulting in a total capacitance of $C_{\mathrm{b}} = 250\,\mathrm{nF}$.

D. DC-Link

Due to the fact that the system at hand is a single-phase AC/DC converter, the power fluctuation with twice the mains frequency has to be buffered in the DC-link capacitor. Especially for MV applications, where electrolytic capacitors are not applicable due to their low voltage rating, the DC-link capacitor is one of the physically largest hardware parts. However, to keep the required volume to a minimum and to still attain a highly compact converter, a peak-to-peak DC-link voltage ripple of $10\,\%$ is selected, leading to a capacitance of $C_{\mathrm{DC}} = 16.2\,\mu\mathrm{F}$. For the mentioned practical reasons, the DC-link is realized with a series connection of six $100\,\mu\mathrm{F}$ film capacitors, whose voltages are passively balanced with high-ohmic resistors ($10\,\mathrm{M\Omega}$) in parallel to the capacitor.

E. Semiconductors

For the design of the *i*TCM converter, it is important to determine the losses of the utilized $10\,\mathrm{kV}$ SiC MOSFETs (*Wolfspeed CPM3-10000-0350*). Since there is one HF and one LF bridge leg, only the HF bridge leg generates switching losses, while both bridge legs generate the same conduction losses due to the same rms currents. During full-load operation, the rms current in the MOSFETs is $I_{\mathrm{FET,rms}} = 6.3\,\mathrm{A}$ which leads to $P_{\mathrm{c}} = 79.4\,\mathrm{W}$ of total conduction losses, if an on-state resistance of $R_{\mathrm{DS,on}} = 500\,\mathrm{m\Omega}$ at a junction temperature of $100\,^{\circ}\mathrm{C}$ (datasheet value) is assumed.

In contrast to the conduction losses of the MOSFETs, the soft-switching losses have to be determined by measurements, since these values are not available from the datasheet.

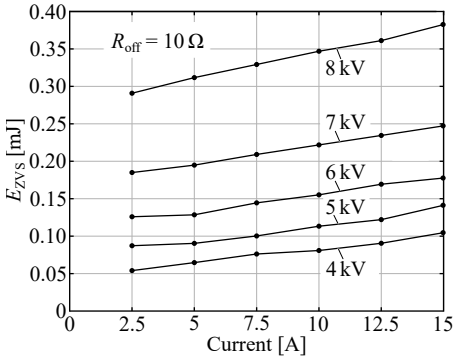

Fig. 8: Calorimetrically measured soft-switching losses with an external turn-off gate resistor of $10\,\Omega$, taken from [29].

Fig. 8 (originally presented in [29]) shows the measured soft-switching losses (SSL) of the utilized $10\,\mathrm{kV}$ SiC MOSFETs for different voltages and switched currents. As can be seen, the SSL show a certain DC voltage dependent offset and rise only slightly and linearly with increasing current, i.e. the SSL are a linear function of the switched current. Based on this, the calculation of the SSL of the *i*TCM converter, where both, the switching frequency and the switched current vary according to **Fig. 3**, simplifies to a multiplication of the average switching frequency with the SSL E_{ZVS} at the average switched current, i.e. $P_{\mathrm{sw}} = \bar{f}_{\mathrm{sw}} \cdot E_{\mathrm{ZVS}}\,(\bar{i}_{\mathrm{sw}})$. With $\bar{f}_{\mathrm{sw}} = 52.6\,\mathrm{kHz}$, $\bar{i}_{\mathrm{sw,S11}} = 15.4\,\mathrm{A}$, and $\bar{i}_{\mathrm{sw,S12}} = 4.1\,\mathrm{A}$ in the positive half-cycle, the switching losses are $P_{\mathrm{sw,S11}} = 13.1\,\mathrm{W}$ and $P_{\mathrm{sw,S12}} = 10.1\,\mathrm{W}$, respectively.

F. LCL Input Filter Design

An important requirement of power electronic converters connected to the grid is the compliance with grid harmonic standards in order to guarantee a stable operation of all devices connected to the grid. However, up to now, existing standards such as the IEEE Std 519 [33] do not cover frequencies higher than $2.5\,\mathrm{kHz}$, i.e. there are no official harmonic limits for MV converters with high switching frequencies, since typically low-frequency transformers or converters with low switching frequencies are used at MV level. Nevertheless, it is known from literature that voltages with high harmonic content cause dielectric heating and ageing of insulation materials or excite grid resonances [34], [35]. In [36], it is proposed to extend the IEEE 519 harmonic standard towards higher frequencies. Hence, the LCL-filter (which is a common filter type in MV applications [15]) of the *i*TCM converter is designed such that the current harmonics stay within these limits. Since the inductance $L_{\mathrm{g}} = 9.55\,\mathrm{mH}$ is already defined by the maximum current ripple (cf. Section III-B), the remaining components are L_{f}, C_{f}, and the filter damping resistor R_{d}. Due to the fact that the filter capacitance causes reactive power and results in an asymmetric switching frequency pattern over a grid period (cf. **Fig. 3**), a small capacitor value C_{f} is desired. If it is assumed that a reactive power of $5\,\%$ due to C_{f} is allowed, its value can be calculated according to [37] and is equal to $274\,\mathrm{nF}$, whereas for practical reasons, $C_{\mathrm{f}} = 250\,\mathrm{nF}$ is selected. The value of L_{f} is now varied until the current harmonics comply with the limits of the extended IEEE 519 standard, which results in $L_{\mathrm{f}} = 1\,\mathrm{mH}$. Due to the small current ripple, a core material with a high saturation flux density (such as amorphous iron) and a solid wire can be used. Thus, L_{f} is realized with one Metglas AMCC-4 tape-wound core and 3 layers of 21 turns with $1.2\,\mathrm{mm}$ solid copper wire. Since the DM voltage across L_{f} is below $100\,\mathrm{V}$, L_{f} is only insulated for the terminal voltage between the winding and the core. Finally, in order to dampen the filter resonance below $-40\,\mathrm{dB}$ (cf. **Fig. 9(a)**), a damping resistor of $R_{\mathrm{d}} = 10\,\Omega$ is used, leading to $P_{\mathrm{Rd}} = 7.35\,\mathrm{W}$ of losses caused by the current ripple in L_{g}. **Fig. 9(a)** shows the simulated and measured transfer function of the LCL-filter $|G_{\mathrm{LCL}}|$ with shorted grid-side, i.e. the grid is assumed with zero impedance. As can be seen, the measurement and the simulation match very

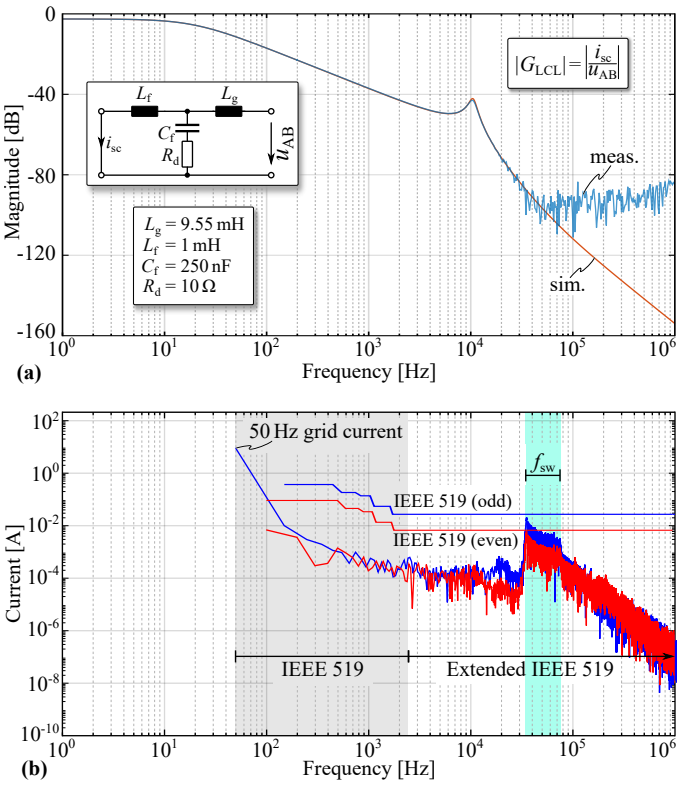

Fig. 9: **(a)** Simulated and measured transfer function of the implemented LCL-filter $|G_{\mathrm{LCL}}|$. **(b)** Extended IEEE 519 harmonic standard limits together with the grid-current spectrum of the *i*TCM converter.

well apart from the fact that the utilized measurement device *Omicron Lab Bode 100* cannot measure attenuations lower than $\approx -100\,\mathrm{dB}$. Furthermore, **Fig. 9(b)** shows the limits for the odd and even harmonics of the extended IEEE 519 standard together with the simulated spectrum of the grid current of the *i*TCM converter. Due to the variable switching frequency, the spectrum does not show the typical discrete harmonics but is rather blurry, while it never exceeds the IEEE 519 limits, as desired.

G. Connection to the MV Grid

As already mentioned, the *i*TCM converter at hand is intended as AC/DC front end of an SST to supply e.g. data center applications or high power battery charging facilities. Thereby, the power is typically delivered from a substation via a MV cable, which, from a high-frequency point of view, can be seen as practically undamped transmission line [38]. Consequently, the cable itself is an oscillatory system with distinct resonances, depending on the length of the cable. **Fig. 10** shows the frequency of the first cable resonance of a 1x400 RM/35, Type N2XS2Y 6/10 kV cable [39] with $L' = 290\,\mu\mathrm{H/km}$ and $C' = 550\,\mathrm{nF/km}$. Translated into transmission line parameters, these values result in a characteristic impedance of $Z_c = 23\,\Omega$ and a propagation delay of $t_p = 6.3\,\mu\mathrm{s}$ for an assumed cable length of $500\,\mathrm{m}$. As can be seen in **Fig. 10**, there is a critical range of the cable length, such that the first resonance frequency of the cable is located within the switching frequency range of the *i*TCM converter. Although

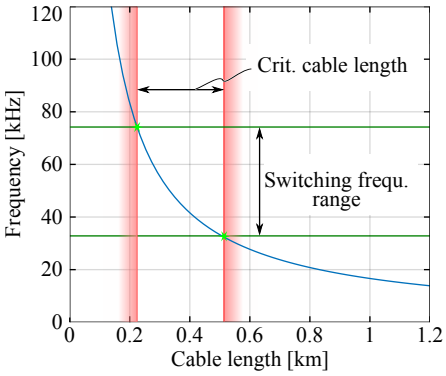

Fig. 10: Frequency of the first resonance peak of a MV cable depending on its length together with the switching frequency range of the *i*TCM converter.

the harmonics of the converter are due to the LCL-filter only in the range of $10\,\mathrm{mA}$ (cf. **Fig. 9(b)**), it has to be ensured that there is no oscillatory interaction of the *i*TCM converter and the MV cable. In case of resonances in the cable, dielectric heating and overvoltages might cause ageing and destruction of the cable insulation, as already mentioned. **Fig. 11(a)** shows the schematic diagram of the LCL-filter and the cable, together with the transfer functions $|G_{\mathrm{Cable}}|$ of the cable with a length of $500\,\mathrm{m}$, the LCL-filter $|G_{\mathrm{LCL}}|$ (cf. **Fig. 9(a)**), and the total transfer function $|G_{\mathrm{tot}}| = \left|\frac{i_g}{u_{AB}}\right|$ from the converter voltage to the grid current, while the grid is assumed to be a short-circuit. It can be seen that the first cable resonance lies within the switching frequency range of the *i*TCM converter and causes a resonance peak in the total transfer function as well. As a consequence, when the switching frequency approaches the critical range $f_{\mathrm{crit.}}$, undesired oscillations in the grid current can be observed, as shown in **Fig. 11(b)**. This behavior can be explained by wave reflections in the cable, since it is not terminated with its characteristic impedance Z_c on neither side. The oscillations can e.g. be damped by another LC-filter stage, as described in [40]. However, this does not change the behavior of the cable, but only reduces the excitation, and in case several (different) converters are connected to the same MV cable, interactions between the filter stages might occur. Therefore, to completely circumvent wave reflections and oscillations independently of the cable length and other connected converters, an RC termination network (TN) is added between the LCL-filter and the MV cable, as shown in the schematic in **Fig. 11(c)**. Thereby, $C_t = 400\,\mathrm{nF}$ acts as a blocking capacitor for line frequency currents in order to not cause undesired low-frequency losses. If now R_t is selected to be equal to Z_c, for high frequencies (where C_t is a quasi short-circuit), the cable is terminated with its characteristic impedance $R_t = Z_c$, which impedes any wave reflections. As can be seen in **Fig. 11(c)**, the transfer function of the cable with the TN is almost flat, i.e. the cable is not interfering any more with the converter and its LCL-filter, which results in a smooth total transfer function. The grid current waveforms of the *i*TCM converter with the TN are shown in **Fig. 11(d)** and as expected from the transfer functions, the grid current i_g is smooth and free of any oscillations. As already mentioned, due to the additional capacitance C_t, the asymmetry in the

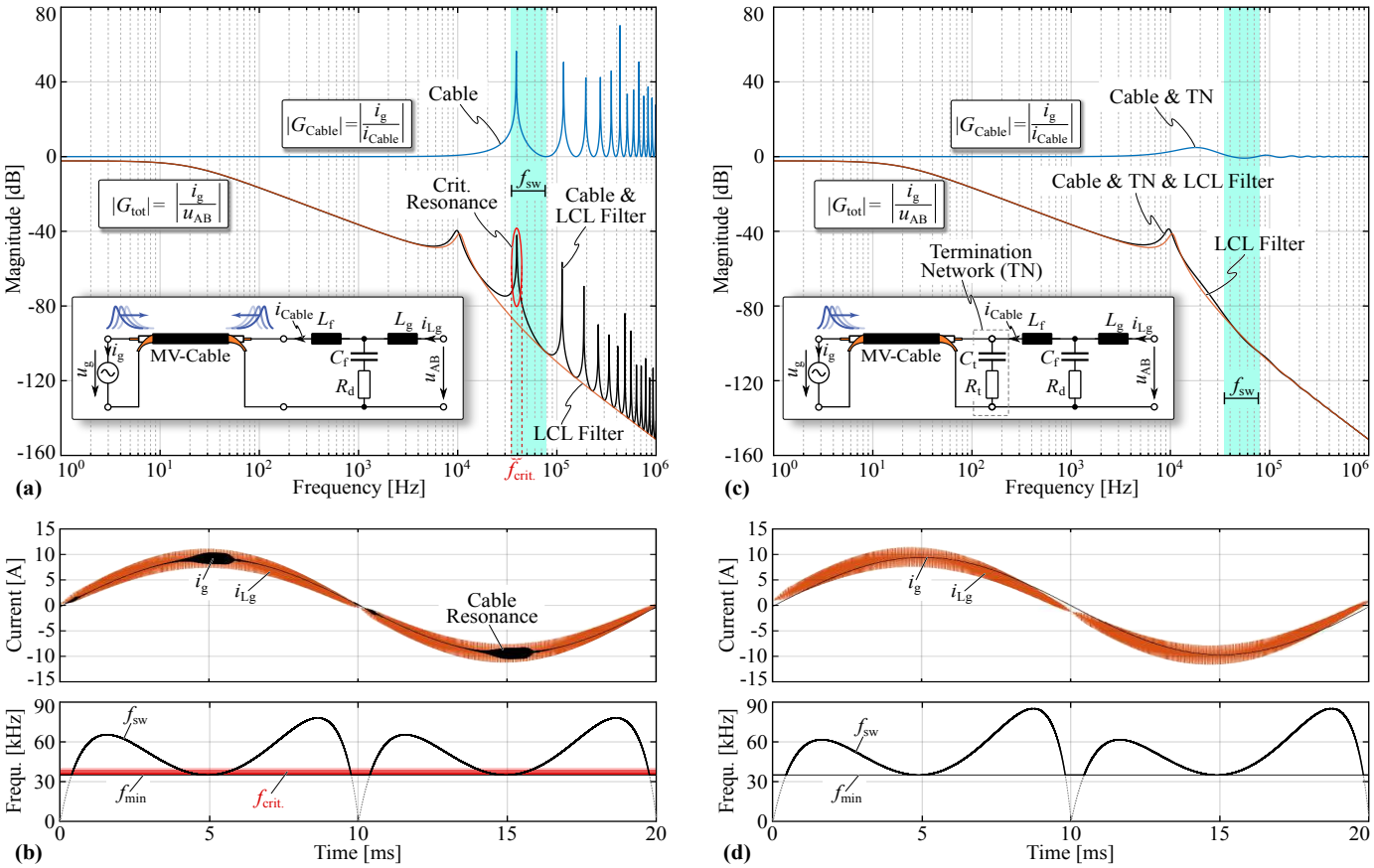

Fig. 11: **(a)** Transfer functions of the MV cable, the LCL-filter, and their combination, i.e. the total transfer function from the converter voltage u_{AB} to the grid current i_{g}. The first resonance peak of the cable lies within the switching frequency range of the *i*TCM converter, leading to oscillations in the grid current i_{g} when the switching frequency approaches the critical range, as can be seen in **(b)**. **(c)** By adding a termination network (TN) between the LCL-filter and the MV cable, the cable resonances can be damped, leading to a smooth grid current as shown in **(d)**.

switching frequency pattern is slightly more pronounced, as can be observed in **Fig. 11(d)**. The reader should note that the hardware demonstrated in this paper does not contain the TN, since this is not necessary in the laboratory where the load is directly connected to the converter without a MV cable.

H. iTCM Hardware Prototype

For the experimental verification of the *i*TCM concept, a hardware prototype has been realized with the goal to achieve a highly compact design, even though large distances for the electrical isolation of the MV are required. These distances can be distinguished into creepage (shortest path between two conductive parts, measured along the surface of the insulation) and clearance distances (shortest distance between two conductive parts, measured through air). According to the IEC 60950-1 International Standard [41], for a sustainable operation, the required creepage distance for $7\,\mathrm{kV}$ is $d_{\mathrm{cr}} = 32\,\mathrm{mm}$, and the minimum clearance distance is $d_{\mathrm{cl}} = 17.5\,\mathrm{mm}$. Consequently, during the PCB layout and especially during the 3D CAD design, it has to be ensured that these distances are respected, although a highly compact design is desired.

Fig. 12 shows the constructed *i*TCM converter seen from its left side and its right side, respectively. It consists of a top-side PCB, which interconnects the DC-link with the HF bridge leg, and a bottom-side PCB, which holds the LF bridge leg as well as the filter capacitors C_{b} and C_{f}, and the inductors L_{b}, L_{g}, and L_{f}. As explained in Section III-A, the PCB layouts are optimized for the lowest possible parasitic switch node capacitance and as can be seen, the high-side gate driver (on $7\,\mathrm{kV}$, $35...75\,\mathrm{kHz}$ switched potential) is separated from the low-side gate driver (GND potential) with a creepage slot in the PCB in order to break the creepage path (which increases the breakdown voltage since $d_{\mathrm{cl}} < d_{\mathrm{cr}}$). These creepage slots can also be found on the bottom PCB and the acrylic glass side walls, which together with the top and bottom PCBs form an air channel for the cooling of the components. The necessary air flow is provided by four $70\,\mathrm{mm}$ fans blowing through the heat sinks of the four MOSFETs, from where the air flow continues across the inductors and capacitors, leaving the converter through a perforated acrylic plate. Since the base plates of the $10\,\mathrm{kV}$ SiC MOSFETs are on the respective drain potentials, the best solution for the lowest parasitic capacitance (cf. Section III-A) is to attach the four heat sinks directly to the MOSFETs' base plates instead of grounding and isolating them with e.g. an aluminum nitride plate. Therefore, the heat sinks are also on the same potential as the drain terminal of the respective MOSFETs and have to be separated from each other and the surrounding parts such as the fans, the DC-link capacitors, and the inductors, as shown in **Fig. 12**. Only the heat sinks of the two high-side MOSFETs (visible in the lower

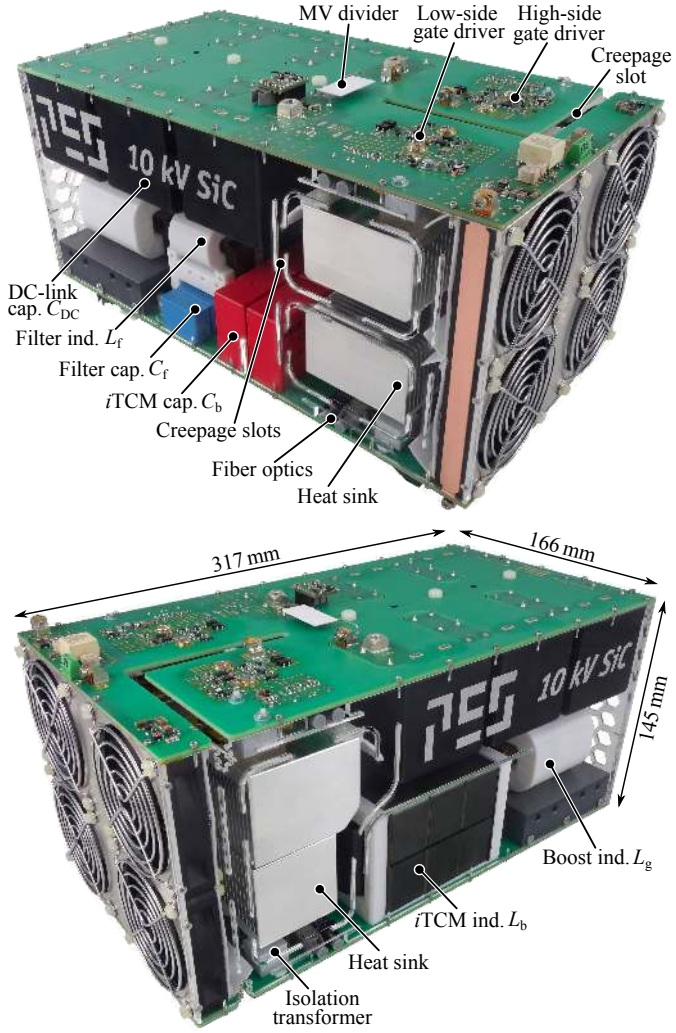

Fig. 12: Photos of the realized *i*TCM converter. Despite the large required isolation distances for 7 kV, a highly compact design with a power density of 3.28 kW/L (54 W/in^3) is achieved, whereby all clearance and creepage distances comply with the IEC 60950-1 International Standard [41].

picture) are on the same potential U_{DC} and do not have to be separated from each other. Although the fans are separated from the heat sinks for the aforementioned reason, they are shielded from the HF electric field of the heat sinks with a steel net tied to GND in order not to disturb the fan motor electronics.

Additionally, the *i*TCM converter is equipped with Hall-effect current sensors for the measurement of i_b and i_{Lg}, as well as MV voltage dividers for the measurement of U_{DC} and u_g. The measurement is performed on each gate driver with floating source potential and the measurement signals as well as the gate signals are transferred via optical fibers to a control PCB (with a *Texas Instruments TMS320F28335* DSP). Furthermore, as an important feature, the gate drivers are equipped with an ultra-fast overcurrent/short-circuit protection, which features a reaction time of 22 ns and turns off all MOSFETs safely in case of an overcurrent, even in case of a flashover [42]. In order to achieve a system without the need of external isolated auxiliary power supplies, ultra-compact auxiliary insulation transformers with an insulation rating of 20 kV have been developed and are utilized in the *i*TCM converter [42].

Given the fact that the realized converter shown in **Fig. 12** is a 7 kV single-phase AC/DC converter, it features an unprecedented power density of 3.28 kW/L (54 W/in^3).

IV. Experimental Setup and Results

To test the functionality and to measure the efficiency of the realized *i*TCM converter, an appropriate experimental setup is required. Due to the bidirectionality of the converter, the power can basically be supplied either from the AC or the DC-side, whereby the efficiency is equal for both directions. Therefore, as shown in **Fig. 13**, the *i*TCM converter is supplied from a bidirectional isolated 400 V to 7 kV DC/DC converter, which is fed from its 400 V side by two parallel 0...500 V, 0...40 A power supplies (*Regatron TopCon Quadro TC.P.16.500.400.S*). The DC/DC converter will be presented in a future publication and forms together with the *i*TCM converter at hand a 25 kW, 3.8 kV AC to 400 V DC SST, as already shown in **Fig. 1(b)**.

During the tests, the *i*TCM converter is operated in open loop (apart from a feed-forward term to compensate for the DC-link voltage ripple) in order to demonstrate the simplicity of the *i*TCM concept, i.e. no additional control is required. During operation, the currents and the HF switch node voltage are measured with *Pearson* current transformers and *LeCroy PPE 20 kV* voltage probes, whereby the 50 Hz AC output voltage is measured with a *LeCroy HVD3605* differential voltage probe. To obtain a high measurement quality and accuracy, a *LeCroy HDO4054A* 12-bit oscilloscope is used.

A. Experimental Results

In order to verify the proper operation of the *i*TCM converter and to determine its performance, the converter has been operated at different power levels, while the current and voltage waveforms and the efficiency have been measured. For the *i*TCM converter at hand, it is especially interesting to see whether or not soft-switching is achieved over the whole grid period in open loop operation.

1) Measured Waveforms: **Fig. 14** shows the measured waveforms of the switch node voltage u_{SN} of the HF bridge leg together with the AC output voltage u_g, the currents i_b, i_{Lg}, i_g, and the current i_A flowing out of the HF switch node A (cf. **Fig. 2(a)**) during full-power (25 kW) operation. As can be seen, the AC output voltage u_g and the AC output current i_g are nicely sinusoidal and in phase to each other, as desired. Furthermore, it can be observed in the envelope of i_A, that the switched current is almost constant at ≈ -4.5 A during

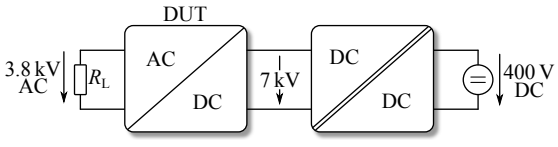

Fig. 13: Block diagram showing the experimental setup for the operation of the realized *i*TCM converter. The AC/DC and DC/DC converters together form a 25 kW bidirectional 3.8 kV AC rms to 400 V DC SST. For the laboratory operation, the power is fed into the 400 V DC side of the SST and dissipated in a resistive load on the MV AC side.

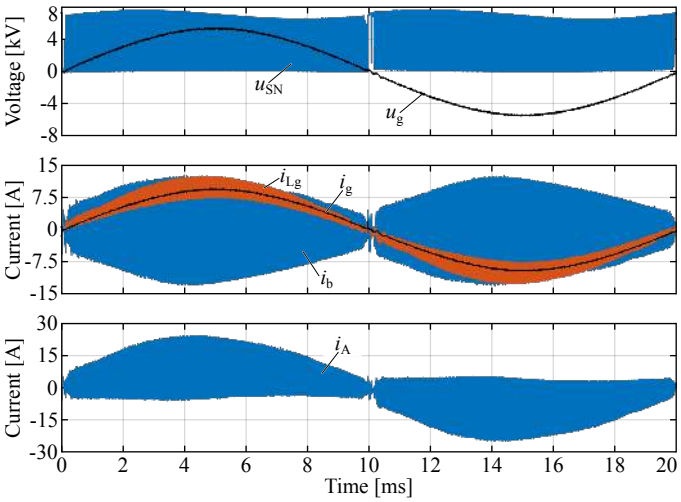

Fig. 14: Measured current and voltage waveforms over a full grid period during full-power (25 kW) operation of the *i*TCM converter. A smooth sinusoidal output voltage and current is achieved, while the MOSFETs are soft-switching over the full grid period, as can be seen from the current i_A flowing out of the $\{S_{11}, S_{12}\}$ bridge leg and showing an almost constant turn-off value of $I_{ZVS} = 4.5\,A$.

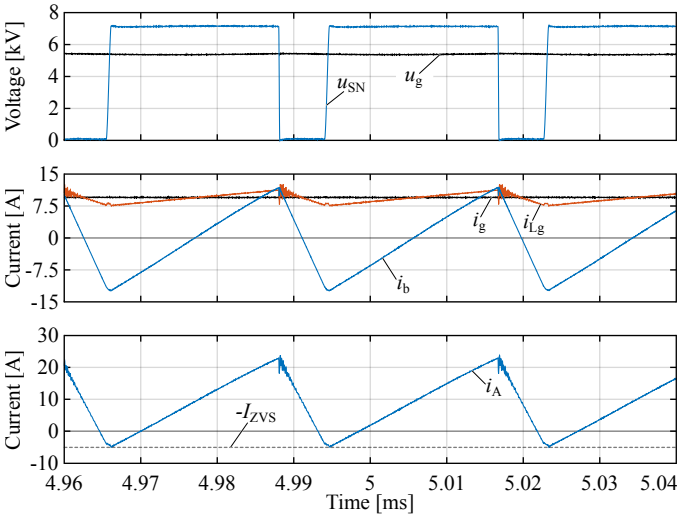

Fig. 15: Measured current and voltage waveforms during the peak of the grid period at full-power (25 kW) operation of the *i*TCM converter. It can be seen that both, the rising and the falling voltage transitions are soft-switched. Furthermore, the current i_A reaches a value of $-I_{ZVS} = -4.5\,A$ to guarantee soft-switching.

the positive, and $\approx +4.5\,A$ during the negative half period, respectively. This means that soft-switching is achieved over the whole grid period and proves that the *i*TCM concept is working nicely, even without any feedback control.

For a better insight into the waveforms, the two most interesting points, namely region around the peak and the zero crossing of the grid voltage, are shown in more detail in the following. The measured waveforms around the peak of the grid voltage are plotted in **Fig. 15**. It can be observed that the waveforms are very smooth and symmetric, which is a result of a careful design of the converter (i.e. low commutation loop inductance in the HF path and low parasitic capacitances of the inductors). Furthermore, the ZVS current $-I_{ZVS} = -4.5\,A$ proves that the converter is operated under

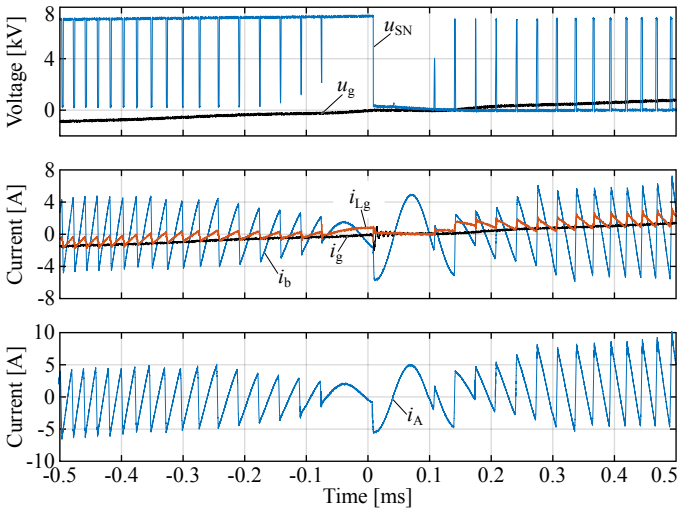

Fig. 16: Measured current and voltage waveforms during the zero crossing of the grid period at full-power (25 kW) operation of the *i*TCM converter. Both duty cycles of the bridge legs $\{S_{11}, S_{12}\}$ and $\{S_{21}, S_{22}\}$ are changing from 1 to 0, i.e. the switch node voltages change from 7 kV to 0 V. Except for the switching transition at $t = 0\,ms$, the other switching transitions are soft-switched as can be seen from the current i_A.

soft-switching conditions. The second interesting point within the grid period is the zero crossing of the grid voltage, where the LF bridge leg commutates and the duty cycle of the HF bridge leg changes abruptly from 1 to 0, as shown in **Fig. 16**. Thereby, it is of high importance that the commutation of the HF and the LF bridge legs are synchronized precisely in order not to falsely create undesired current spikes. However, due to the different switching speeds of the HF and LF bridge legs (the LF bridge leg is hard-switched with a rather high gate resistance of $47\,\Omega$ in order to achieve smooth transitions), a negative current builds up in L_b, followed by an oscillation between L_b and C_b for approx. 100 ns until the HF bridge leg starts switching again. Nevertheless, the amplitude of this oscillation is small and the grid current is not affected. As can be seen in the current i_A, apart from the ZCS transition at the time instant $t = 0\,ms$, all the other switching transitions are soft-switched.

2) Efficiency Measurements: As already mentioned, the efficiency of power electronic converters operated e.g. in battery charging or data center applications is of high importance due to environmental and economical aspects and it is desired that the efficiency is high for a wide power range. **Fig. 17** shows the calorimetrically measured efficiency curve of the *i*TCM AC/DC converter, whereby the applied calorimetric loss measurement methods are explained in detail in the Appendix. As can be seen, the efficiency increases with the power, reaching a peak efficiency of 99.1 % at full load. At 50 % load, the efficiency is still 98.8 %, making the converter also suitable for partial load operation. Comparing these values to existing 10 kV or 15 kV SiC MOSFET-based topologies [16]–[20], a significantly higher efficiency, switching frequency and thus power density are achieved by the *i*TCM converter due to ZVS.

Additionally, the efficiency curve of the also realized isolated DC/DC converter and the complete SST are shown. With

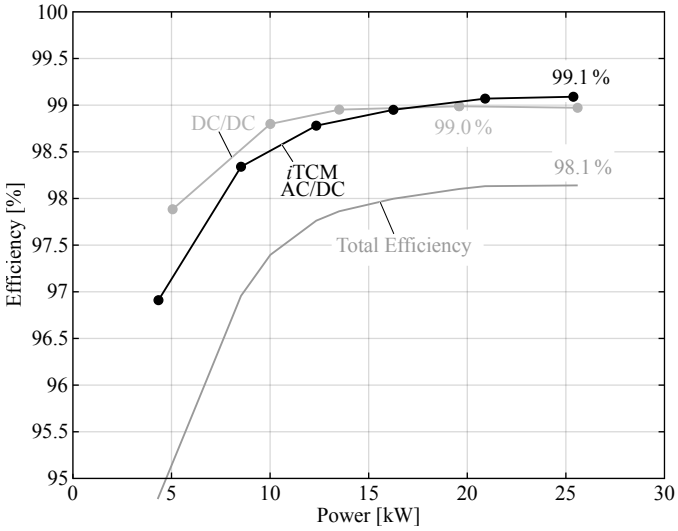

Fig. 17: Calorimetrically measured efficiency of the realized *i*TCM converter. A peak efficiency of 99.1 % is achieved at full load. Together with the also realized isolated DC/DC converter, a full-load efficiency of the complete SST-system (cf. **Fig. 1(b)**) of 98.1 % is reached.

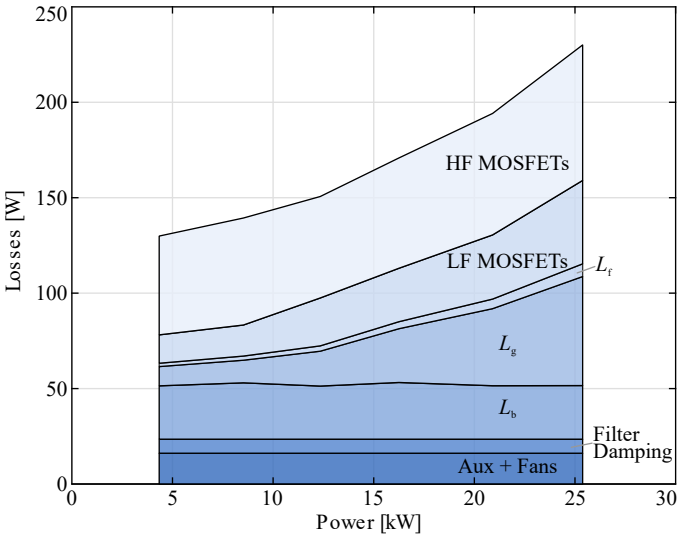

Fig. 18: Measured loss distribution of the *i*TCM converter for different powers.

a DC/DC full-load efficiency of 99.0 %, the total efficiency of the 3.8 kV AC to 400 V DC SST is 98.1 %. Compared to the 25 kW multi-cell system presented in [14] with a full-load efficiency of 96 %, the SST at hand features a 2.1 % higher efficiency, or in other words, generates only half the losses. At the same time, the power density is approximately a factor of four higher, which shows that the single-cell approach with 10 kV SiC MOSFETs is superior to the even much more complex multi-cell approach.

Finally, in **Fig. 18** the loss distribution among the different components is shown, whereby the losses of the inductive components and the semiconductor devices have been measured calorimetrically (cf. Appendix), while the auxiliary and fan powers were measured electrically and the comparably small losses of the filter inductor L_f are taken from the inductor optimization. It can be observed that (besides the constant filter damping and auxiliary losses, which include the control board and the gate drivers etc.) the losses of L_b are constant, as expected. Furthermore, at full power, the difference between the losses of the HF MOSFETs (S_{11} and S_{12}) and the LF MOSFETs (S_{21} and S_{22}), i.e. the switching losses, is 27.3 W. This is in good accordance with the 23.2 W of switching losses calculated in Section III-E (especially considering that the HF anf LF bridge losses also include conduction losses of MOSFETs with strong variations in $R_{\mathrm{DS,on}}$ from device to device). According to the calculation in Section III-E, the total conduction losses should sum up to 79.4 W, whereby the measured conduction losses (twice the LF bridge losses) are 87.4 W. Given the fact that not all MOSFETs are on the same junction temperature, the error of 9 % between measurement and calculation is acceptable. Furthermore, for the inductor L_b, a good agreement of the measured losses (29 W in average) and the calculated losses (32.4 W, cf. **Fig. 5(a)**) can be noted. For L_g, the difference between the measured losses (57 W) and the calculated losses (48 W, cf. **Fig. 5(b)**) is slightly higher but within 16 % which is still very accurate, given that the parameter uncertainties of e.g. the core material are already in this range [43].

V. Conclusion

In this paper, a bidirectional 25 kW, 3.8 kV AC rms to 7 kV DC PFC AC/DC converter based on the the *integrated* Triangular Current Mode (*i*TCM) concept is demonstrated. The *i*TCM concept is a simple method to achieve soft-switching over the entire AC grid period by adding an LC-circuit to the well-known full-bridge PWM AC/DC converter. It is demonstrated that a constant ZVS current and therewith soft-switching over the whole grid period can be achieved even in open loop operation, i.e. no current zero crossing detection, as in case of TCM, is required.

With the help of the switching impedance, the impact of parasitic inductances and capacitances on the design of MV converters is analyzed and compared to the impact on LV converters. Thereby, an elementary difference can be observed, namely that parasitic inductances play a minor role for MV converters, whereas it is very important to minimize parasitic capacitances. Therefore, e.g. coplanar PCB layouts should be avoided in MV applications and the tracks should be separated as far as possible from each other to minimize parasitic capacitances.

The design of all main power components of the converter is presented, whereby the focus is set on the MV inductors and their electrical insulation. Pareto optimizations show that a 40 % peak-to-peak current ripple in the boost inductor is a reasonable trade-off between the highest efficiency/power density and the input filter effort. Different winding arrangements are analyzed to minimize the electric field stress and the parasitic capacitances of the inductors. Furthermore, the selection of the insulation material and the vacuum pressure potting of the winding is described.

For a proper integration of the SST into the MV AC grid, an LCL-filter is designed in order to comply with the extended IEEE 519 harmonic standard and the connection of the converter to a MV cable is analyzed. It can be shown

that, without further measures, oscillations occur due to cable resonances, which are excited by the remaining converter harmonics. These oscillations can be avoided by adding a simple RC termination network between the LCL-filter and the MV cable.

Furthermore, the performed efficiency measurement error analysis shows that electrical efficiency measurements are not suited for converter efficiencies $\geq 99\,\%$, whereas calorimetric efficiency measurement methods show much higher accuracies. Therefore, calorimetric methods for the measurement of the converter loss distribution and the efficiency are presented. The measured full-load efficiency of the realized *i*TCM converter reaches a value of $99.1\,\%$, which in combination with a power density of $3.28\,\mathrm{kW/L}$ ($54\,\mathrm{W/in^3}$) demonstrates an unprecedented performance for a MV single-phase PFC AC/DC converter.

APPENDIX
EFFICIENCY MEASUREMENT METHODS

One of the key performance indicators of a power electronic converter is its efficiency, which is especially important in data center applications, where energy losses directly translate into elevated operating costs. For this reason, an accurate measurement of the *i*TCM converter efficiency is essential. In the following, it is shown that an electrical efficiency measurement achieves only a low and insufficient accuracy. Thus, a calorimetric measurement of the loss components with a much higher accuracy is presented and applied to the converter at hand.

A. Electrical Efficiency Measurement Error Analysis

Typically, converter efficiencies are measured electrically by measuring the input and the output power: $\eta = \frac{P_\mathrm{out}}{P_\mathrm{in}}$. However, for an expected efficiency of $\eta_\mathrm{exp} = 99\,\%$, already very small errors e_p in the input and output power measurements cause significant errors in the measured efficiency value η_meas. If an efficiency measurement error of $e_\mathrm{eff} \leq 0.1\,\%$ is desired (i.e. for a converter efficiency of $99\,\%$, the measured efficiency should be in the range of $98.9\,\% \ldots 99.1\,\%$), the input and output powers have to be measured with an accuracy of $e_\mathrm{p} = 0.05\,\%$ each [44], as can be calculated with (15) and is illustrated in **Fig. 19 (a)**,

$$e_\mathrm{P} = \frac{e_\mathrm{eff}}{2 \cdot \eta_\mathrm{exp} + e_\mathrm{eff}} \approx \frac{e_\mathrm{eff}}{2}. \tag{15}$$

Even a high precision power analyzer, such as the *Yokogawa WT3000*, is unable to reach this accuracy. According to the datasheet, the error of the power analyzer is $e_\mathrm{Y,DC} = 0.05\,\%$ of the reading Y plus $e_\mathrm{X,DC} = 0.1\,\%$ of the power range X (voltage range multiplied by the current range) for DC power measurements and $e_\mathrm{Y,AC} = 0.02\,\%$ of the reading plus $e_\mathrm{X,AC} = 0.04\,\%$ of the power range for AC power measurements. However, the voltages would have to be divided by e.g. a $div = 1:100$ voltage divider, which is accounted with an error of $e_\mathrm{div} = 0.1\,\%$. Furthermore, on the AC-side, since both AC terminals are on potential, a differential voltage measurement is required, leading to an error of already $2 \cdot e_\mathrm{div} = 0.2\,\%$. In addition, for the same reason, the AC current would have to be measured with a current transformer which provides galvanic insulation and is accounted with $e_\mathrm{CT} = 0.1\,\%$. On both sides, the voltage range must be set to $X_\mathrm{U} = 100\,\mathrm{V}$ (due to the voltage division by a factor of 100). For the DC-side, a current range of $X_\mathrm{I,DC} = 5\,\mathrm{A}$ is sufficient, while the AC current has to be measured with a range of $X_\mathrm{I,AC} = 10\,\mathrm{A}$. These values lead to the following AC and DC power measurement errors:

$$\begin{aligned} P_\mathrm{DC,m} &= (U_\mathrm{DC} \cdot div \cdot (1 \pm e_\mathrm{div}) \cdot I_\mathrm{DC}) \\ &\quad \cdot (1 \pm e_\mathrm{Y,DC}) + X_\mathrm{U} \cdot X_\mathrm{I,DC} \cdot e_\mathrm{X,DC} \qquad (16) \\ e_\mathrm{DC,m} &= 1 - \left(\frac{P_\mathrm{DC,m}}{div \cdot P_\mathrm{DC}}\right) = \pm 0.35\,\% \qquad (17) \\ P_\mathrm{AC,m} &= (U_\mathrm{AC} \cdot div \cdot (1 \pm 2e_\mathrm{div}) \cdot I_\mathrm{AC} \cdot (1 \pm e_\mathrm{CT})) \\ &\quad \cdot (1 \pm e_\mathrm{Y,AC}) + X_\mathrm{U} \cdot X_\mathrm{I,AC} \cdot e_\mathrm{X,AC} \qquad (18) \\ e_\mathrm{AC,m} &= 1 - \left(\frac{P_\mathrm{AC,m}}{div \cdot P_\mathrm{AC}}\right) = \pm 0.48\,\%. \qquad (19) \end{aligned}$$

Thus, the total worst case efficiency measurement error is $\pm\left(|e_\mathrm{DC,m}| + |e_\mathrm{AC,m}|\right) = \pm 0.83\,\%$, which for a $99\,\%$ efficient converter would lead to a measured efficiency in the range of $98.17 \ldots 99.83\,\%$. Even without the errors caused by the MV dividers and the current transformer (e.g. for a $99\,\%$ efficient $400\,\mathrm{V}$ system), the measurement error (only caused by the power analyzer) is $\pm 0.43\,\%$, which is totally unacceptable.

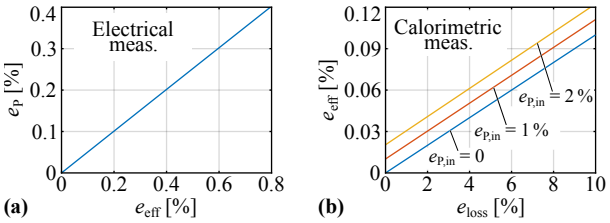

Fig. 19: **(a)** Allowed power measurement error e_P as a function of the desired efficiency measurement error e_eff in case of an electrical efficiency measurement. **(b)** Achieved efficiency measurement error e_eff as a function of the converter loss measurement error e_loss for different input power measurement errors $e_\mathrm{P,in}$ in case of a calorimetric efficiency measurement.

B. Calorimetric Efficiency Measurement

Due to the large measurement errors in case of an electrical efficiency measurement, a more accurate measurement method is required. Instead of measuring the input and output powers and relating them to each other, the converter losses can be measured directly in a calorimetric manner, leading to a much higher accuracy. The efficiency can then be calculated by only measuring the DC input power electrically and deducing the output power from the electrical input power and the calorimetrically measured losses. **Fig. 19(b)** shows the achieved efficiency measurement error e_eff depending on the error of the converter loss measurement e_loss for different errors $e_\mathrm{P,in}$ in the electrical DC input power measurement. If the DC input power can be measured with an error of $e_\mathrm{P,in} = 1\,\%$, the losses of the converter need to be measured with an accuracy of $e_\mathrm{loss} = 10\,\%$ in order to achieve an efficiency error of $e_\mathrm{eff} = 0.1\,\%$.

Typically, for the calorimetric measurement of the converter losses, the converter could e.g. be operated inside a calorime-

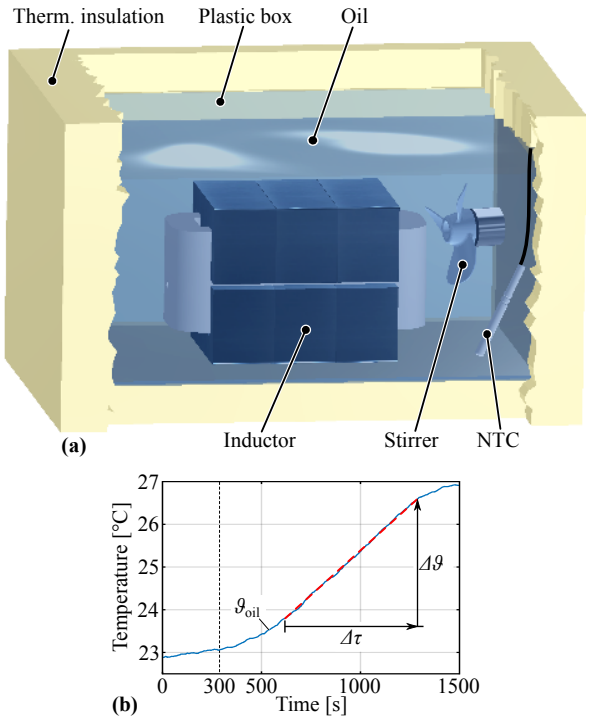

Fig. 20: **(a)** Calorimetric measurement setup for the determination of the losses of the MV inductors L_b and L_g. The inductors are placed in oil-filled and thermally insulated boxes and dissipate their losses into the homogeneously mixed oil whose temperatures are measured via NTCs. **(b)** Measured temperature profile of the oil during full-power operation of the *i*TCM converter for the determination of the losses of inductor L_b. The losses are determined from the temperature rise $\Delta\vartheta/\Delta\tau$ in combination with the thermal capacitance of the whole calorimeter known from calibration measurements with constant power.

ter, which measures the dissipated heat. However, the time constant of such a calorimeter to reach steady state is in the range of several hours. Moreover, only the total converter losses can be measured and no information about the loss distribution can be given. To measure also the loss distribution among the components in an even shorter measuring time, the losses of the MOSFETs and the inductors are measured separately with calorimetric methods, as shown in **Figs. 20 & 21** and explained in the following sections. The remaining loss components, such as the auxiliary power for the gate drives, the DSP, the fans, and the filter damping resistor R_d can be measured electrically. Furthermore, the losses of the grid-side filter inductor L_f are very small and are taken from the inductor simulations, since even a large error in these small losses would not influence the accuracy of the total loss measurement significantly. For the capacitors, it can be calculated from the dissipation factor, that the losses are smaller than 1 W, hence these losses are neglected.

1) Calorimetric Inductor Loss Measurement: In order to measure not only the converter efficiency, but also the loss distribution among the individual components (whereby the inductors L_b and L_g, as well as the MOSFETs are the main contributors), the inductors L_b and L_g were separated from the converter setup shown in **Fig. 12** and are operated outside the converter to measure the pure inductor losses. The measurement of inductor losses under real operating conditions is a difficult task, especially when a high accuracy is desired. Therefore, several calorimetric measurement methods have been developed in literature [45]–[47]. Thereby, steady state measurement methods [30], [46] and transient measurement methods [45] are used. For the sake of a short measurement time, a transient measurement method is preferred in order not to dissipate the system power of 25 kW into the laboratory for several hours. Therefore, the inductors L_b and L_g are externally placed in separate oil calorimeters, i.e. thermally insulated oil tanks equipped with a stirrer (to ensure a homogeneous temperature in the oil) and an NTC temperature sensor. **Fig. 20(a)** gives an insight into the oil calorimeter. The silicone oil (*Bluesil Fluid 604V50* usually used for transformer insulation) fulfills two tasks in the calorimeter: On the one hand, it extracts the losses out of the core and the winding such that the inductor together with the oil are at the same temperature, and on the other hand it provides electrical insulation. Due to the thermal insulation of the oil calorimeter towards the ambient, adiabatic conditions can be assumed. From calibration measurements with constant DC power injection into the inductor winding, the thermal capacitance C_{Th} of the calorimeter can be determined. Finally, for the measurement of the inductor losses, the oil temperature is measured during the operation of the *i*TCM converter, as shown in **Fig. 20(b)**. As can be seen, after a certain settling time (converter operation starts at time 300 s), a linear temperature profile can be observed, as expected for constant inductor losses and a constant thermal capacitance C_{Th}. The total inductor losses can thus be determined as

$$P_{ind} = C_{Th} \cdot \frac{\Delta\vartheta}{\Delta\tau}. \tag{20}$$

As can be seen in **Fig. 20(b)**, the temperature slightly increases before the converter operation is started at time 300 s. This can be explained by the losses of the stirrer motor (6.77 W in the L_b calorimeter and 7.53 W in the L_g calorimeter) which are measured electrically and subtracted from the calorimetrically measured losses in order to obtain the pure inductor losses.

With a temperature measurement resolution of $e_{NTC} = 0.1\,\mathrm{K}$ (mainly limited by EMI noise during converter operation) and a temperature difference of $\Delta\vartheta = 2.8\,\mathrm{K}$ (cf. **Fig. 20(b)**), the measurement error is 7.1 %, if a perfect time measurement is assumed. During the calibration with DC, no EMI noise is present and the resolution of the temperature measurement is 0.05 K. Therefore, the error in the measurement of the thermal capacitance C_{Th} is 3.5 % which leads to a total worst case measurement error of $e_{oil} = 10.6\,\%$ (i.e. the algebraic sum of the losses, which is even worse than the geometric sum of 7.9 % obtained with the propagation of uncertainty) for the oil calorimeters. The conducted experiments show that the difference between the highest and the lowest measured losses of L_b (which are independent of the processed power, cf. **Fig. 18**) diverge by 6.75 %. This value matches well with the predicted 7.1 % from above.

2) Calorimetric Semiconductor Loss Measurement: The loss measurement of the utilized 10 kV SiC MOSFETs has been extensively described in [29], where brass blocks have

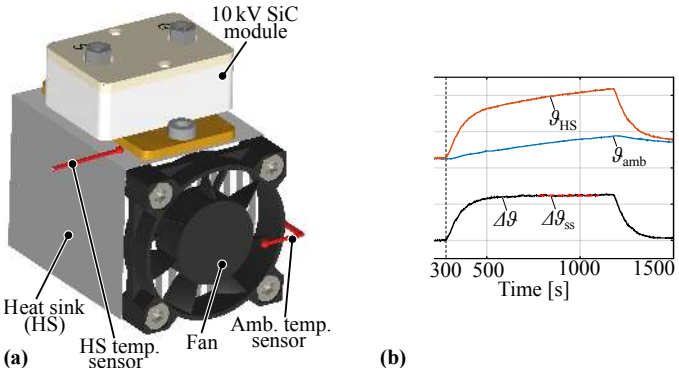

Fig. 21: **(a)** Calorimetric setup for the measurement of the semiconductor losses. Each of the four utilized 10 kV SiC MOSFET modules is mounted on a separate heat sink whose temperature is measured via a fiber-optic temperature measurement system (*Optocon FOTEMPMK-19"*). **(b)** Measured temperature profiles during 25 kW operation of the converter. With the measured temperature difference $\Delta\vartheta$ and the thermal resistance $R_{\mathrm{Th,HS}}$ of the heat sink (known from calibration measurements with constant power), the losses of the 10 kV SiC module can be determined.

been used as adiabatic heat sinks with a defined thermal capacitance in order to measure the transient temperature response for the loss determination, similar to the oil calorimeter described above. However, the MOSFETs are now placed on separate and actively cooled heat sinks, as can be seen in **Fig. 12**. The thermal system is thus dominated by the convective cooling instead of the thermal capacitance of the heat sinks. Furthermore, the thermal time constant of the heat sinks together with the 10 kV MOSFETs is in the range of only 100 s, i.e. the time for the heat sinks to reach steady state is approximately 10 min. For these reasons, the semiconductor losses are measured via the steady state temperature difference $\Delta\vartheta_{\mathrm{ss}}$ between the heat sink and the ambient. **Fig. 21(a)** shows the basic setup with a single 10 kV module mounted on a heat sink which is actively cooled by the air flow of a fan. As already mentioned, the heat sinks in the constructed *i*TCM converter (cf. **Fig. 12**) are on the respective drain potential, which is why the fans are separated from the heat sink in reality. However, for the explanation of the loss measurement concept, this is not shown in the schematic drawing in **Fig. 21(a)**. The (switched) potentials on the heat sinks imply that the heat sink temperature measurement sensors must be galvanically isolated. Hence, a fiber optic temperature measurement system (*Optocon FOTEMPMK-19"*), which measures the temperature at the tip of up to 10 non-conductive optical fibers, is used. As shown in **Fig. 21(a)**, one optical fiber is placed on the heat sink and one in front of the fan for the measurement of the air temperature. The thermal resistances $R_{\mathrm{Th,HS}}$ of the four heat sinks are measured separately by injecting a constant DC-power into the respective MOSFET and measuring the temperature difference between the heat sink and the air temperature in front of the fan. Thereby, the system must be in exactly the same conditions as in case of the converter operation (e.g. the fan voltage must be kept constant and the geometry must not be changed, i.e. the side walls must remain closed and the temperature sensor position must not change). This ensures that the measured thermal resistances of the heat sinks are exactly the same during the calibration and the efficiency measurements. The reader should note that the cross-coupling between the different heat sinks has been analyzed and can be neglected.

Fig. 21(b) shows the measured ambient and heat sink temperature profiles ϑ_{amb} and ϑ_{HS} together with the temperature difference $\Delta\vartheta$ during the converter operation at 25 kW. The converter operation is started at time 300 s, as can be seen from the temperature increase. Due to the fact that the converted power is dissipated in the laboratory, the room temperature also rises slowly. However, the time constant of the heat sink is much smaller than the time constant of the room, which can be seen at time 1200 s where the converter is turned off and the heat sink temperature decreases much faster than the ambient temperature. For this reason, the temperature difference $\Delta\vartheta$ between the heat sink and the ambient reaches a steady state value $\Delta\vartheta_{\mathrm{ss}}$, and the losses of the semiconductor modules can be determined as

$$P_{\mathrm{semi}} = \frac{\Delta\vartheta_{\mathrm{ss}}}{R_{\mathrm{Th,HS}}}. \tag{21}$$

For a resolution of 0.2 K of the fiber optic temperature measurement and a steady-state temperature difference of $\Delta\vartheta_{\mathrm{ss}} = 12.4\,\mathrm{K}$, the measurement error is 3.2 %. Together with an assumed deviation of the thermal resistance of 5 %, the maximum expected error (for this operating point) is $e_{\mathrm{HS}} = 8.2\,\%$ (with the propagation of uncertainty, the error would only be 5.9 %).

3) Calorimetric Efficiency Measurement Accuracy: In order to determine the total accuracy of the applied efficiency measurement, the errors of the individual measurement methods are weighted with the respective measured losses and to calculate the worst case are summed up. If the following errors are assumed for the losses (L_{F}: 15 % since it is calculated; R_{d}: 10 % due to 5 % error on the current measurement and $R_{\mathrm{d}} \cdot I^2$; Auxiliary: 0.5 % due to low voltage, low current DC power measurement with multimeters), the total weighted loss measurement accuracy is 9 %. Combined with a converter DC input power measurement error of 2 % due to the measurement of the MV DC-link voltage, a total efficiency measurement error of 0.11 % is obtained from **Fig. 19(b)**.

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