99-dB high-performance delta-sigma modulator for 20-kHz bandwidth

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Abstract

In this paper, we present a fourth-order single-bit delta-sigma modulator with wide dynamic range. This modulator is suitable for distributed sensor and audio codec applications. This chip was fabricated in a 0.18-μm one-poly, four-metal CMOS technology, and occupies 1.22-mm^2 active area. The circuit is clocked at 3.2 MHz and the overall power consumption is 5.6 mW from a 3.0 V power supply. Experimental results show a maximum dynamic range of 99 dB within a 20-kHz bandwidth.

1. Introduction

During the last two decades, delta-sigma modulators have found their way into many different applications due to their superior performance. Delta-sigma modulators with high resolution are used in various areas, from distributed sensor applications such as seismic detection for oil exploration to digital audio equipment such as DVD recording systems. These delta-sigma modulators for high resolution systems must have the properties of wide dynamic range (*DR*) and low distortion in order to capture an analogue input signal in its most original form. Low power consumption is also an important factor, often just as critical as *DR*.

Several different modulator architectures have been used in order to achieve high resolution and low power consumption. In this paper, the modulator architecture selected for distributed sensor and audio codec applications is a single-loop, single-bit, delta-sigma modulator which has a mixed loop topology incorporating both feedback and feed-forward paths. This enables the modulator to combine the advantages of both distributed feed-forward and distributed feedback topologies. We will provide the figure-of-merit (*FOM*) of this modulator as compared with other state-of-the-art modulators.

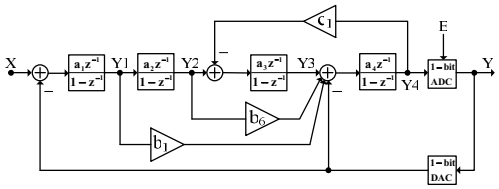

Figure 1. Single-bit 4th-order delta-sigma modulator block diagram [1]

2. Modulator system-level design

In the complete design of a delta-sigma modulator, there are three major steps to be followed. First, a suitable architecture must be selected according to the requested system-level specifications: signal-to-noise ratio (SNR), signal bandwidth, etc. Then, we have to make several decisions within the constraints thus imposed; there is some degree of freedom in the actual design. Finally, the circuit topology must be selected for each section, and sized to meet the required circuit specifications.

The *DR* is determined primarily by the over-sampling ratio (*OSR*), the loop order (*n*), and the quantizer resolution (*B*). The *DR* of the modulator is defined as the ratio of the power in a full-scale input to the power of a sinusoidal input for which the signal-to-noise ratio is one (0 dB). The search for an optimal delta-sigma modulator topology is performed by varying *OSR*, *n*, and *B* in an attempt to achieve the ideal, or target *DR*. The *DR* is related to *OSR*, *n*, and *B*, according to [2]:

$$DR = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right) OSR^{2n+1}\left(2^{B}-1\right)^{2} \qquad (1)$$

In order to achieve a *DR* of more than 100 dB, we chose the single-bit single-loop modulator with an *OSR*=80 and *n*=4.

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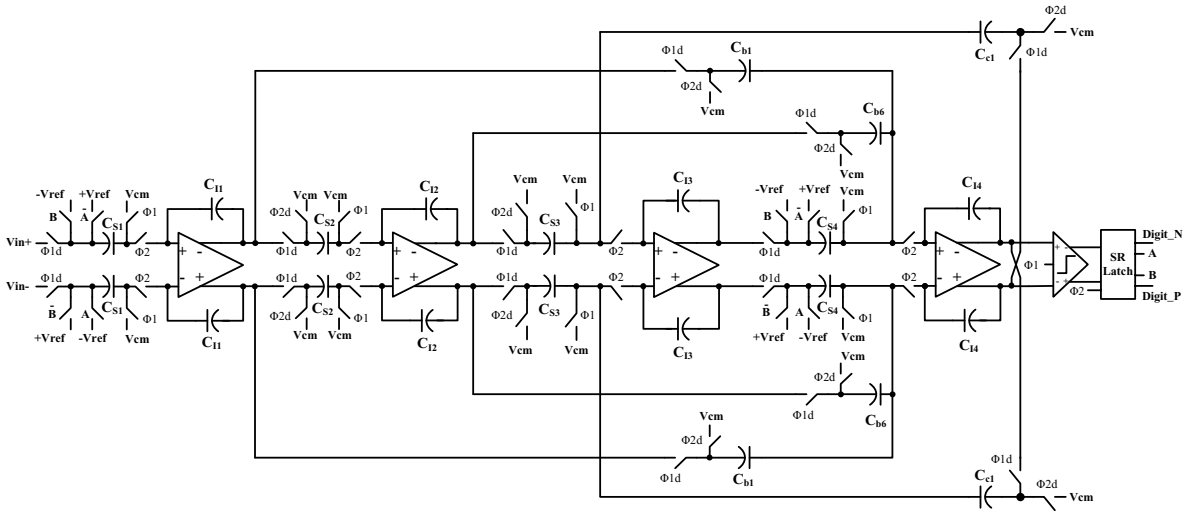

Figure 2. The designed Single-bit 4th-order delta-sigma modulator

The *DR* is determined not only by the systematic factors mentioned above but is also limited by *kT/C* noise; the noise level in the signal band is determined by the white *kT/C* noise, as discussed in [3]. The first integrator is the one most responsible for the overall performance in a single-loop modulator. The *DR* of a delta-sigma modulator, where the resolution is limited by the *kT/C* noise of the first switched-capacitor integrator stage, is given by [2]:

$$DR = \frac{S_S}{S_{kT/C}} = \frac{(V_{SW})^2 \times OSR \times C_S}{8kT} \qquad (2)$$

In the above equation, S_S and $S_{kT/C}$ are the power of a full-scale sinusoidal input and the power of the *kT/C* noise, respectively. V_{SW} is the amplitude of a full-scale sinusoidal input to the modulator, and is set to 3 V in this paper. k is Boltzmann's constant, T is the absolute temperature, and C_S is the sampling capacitance of the first integrator. In order to achieve 110-dB *DR* in equation (2), sampling capacitance should be 4.6 pF, but we used 5 pF, taking into consideration reasonable margin.

A block diagram of a single-bit, 4th-order delta-sigma modulator is given in figure 1. In this figure, X, Y, and E respectively represent input, output, and quantization error. The outputs of the first integrator and the second integrator are connected to the input of the fourth integrator through the feed-forward paths. The feed-forward factors are b_1 and b_6. The feedback around the last two integrators forms a local resonator. By choosing the appropriate feedback factor c_1, the complex zeros can be located in order to give optimum noise suppression in the signal band. The loop coefficients in figure 1 are as follows:

$$a_1 = \frac{1}{3}, a_2 = \frac{3}{25}, a_3 = \frac{1}{10}, a_4 = \frac{1}{10}, b_1 = \frac{6}{5}, b_6 = 1, c_1 = \frac{1}{6}$$

Here, a SIMULINK model was used to perform the behavioural simulation of the single-bit 4th-order delta-sigma modulator.

3. Circuit design

3.1. Switched-capacitor integrator

After behavioural level simulations were performed, we had enough parameters for transistor level implementation. All required analogue blocks were designed and simulated.

The proposed delta-sigma modulator is implemented using fully differential switched-capacitor techniques. Fully differential topology has basically two advantages: a higher immunity to environmental noise and a wider dynamic range.

The modulator in figure 2 is controlled by two-phase, non-overlapping clocks: Φ1 for the sampling phase and Φ2 for the integration phase. Delayed clocks of the two phases (Φ1d and Φ2d) are used to reduce the effects of charge injection in the switched-capacitor circuits.

The input signal is sampled from the sampling capacitance during Φ1. During Φ2, a charge transfer takes place from the sampling capacitance to the integration capacitance to perform the integration function. The input and feedback gains of the first

Table 1. Simulated result of opamps

Parameter	Opamp1	Opamp2
Power supply voltage [V]	3	3
DC gain [dB]	73.6	73.5
Phase Margin [deg]	87.7	86.3
Slew Rate [V/μs]	34.6	21
Unity Gain Freq, F_u [MHz]	23	22
Output Swing [Vpp]	± 2.2	± 2.2
Power Consumption [mW]	3.165	0.822

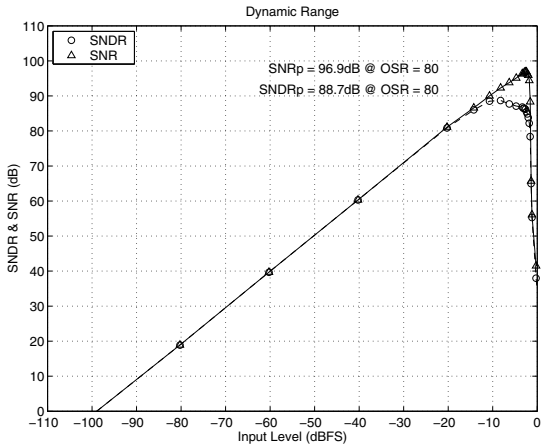

Figure 3. Measured *SNR* and *SNDR*

integrator have the same value, which allows the same capacitor to be used for input and feedback sampling. This choice leads to a reduction in the silicon area and in the coefficient mismatch.

The modulator consists of four non-inverting delaying integrators to avoid the double-settling problem. In figure 2, both the first and fourth integrators use two symmetrical reference voltages, +Vref and −Vref, which are equal to the supply voltages (3 V and 0 V). Lowering the feedback levels would reduce the dynamic range of the converter. The switches in this design were implemented using transmission gates, NMOS transistors, and PMOS transistors. Advantages of using transmission gates include the simplicity of the circuit and the power savings. The NMOS and PMOS transistors were sized appropriately to keep their on-resistance low enough to limit harmonic distortion. In our modulator, there is no need to use a clock bootstrapping circuit to boost the driving voltage, since the supply voltage is sufficiently high.

3.2. Operational amplifier (Opamps)

Although all analogue components are important, the most critical circuit in determining the settling speed and noise performance of the integrator is the operational amplifier (opamp). We used a fully differential folded cascode opamp with a switched capacitor common mode feedback (SCCMFB). The SCCMFB is based on the use of switched-capacitors, and has an advantage in power reduction, because no static current is consumed to generate the mid-point of the differential swing.

The important specifications for the design of an opamp are: open-loop dc gain, unity gain frequency (Fu), phase margin (PM), slew-rate, and output swing. In our design, we used two versions of the opamp, which consumed different current. Opamp1 denotes the opamp used at the first integrator and opamp2 indicates the opamp used with the rest of the integrators. For opamp2, the total quiescent currents are reduced by a factor of four. Table 1 shows the simulated results of opamps obtained using the HSPICE tool.

3.3. Comparator

The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effect of those impairments is attenuated by noise shaping. Therefore, we employed a simple dynamic regenerative comparator.

The comparator used in this design does not include a pre-amplifier or an offset cancellation circuit as used in [3]. This comparator includes input transistors, clock transistors, and pre-charge transistors, plus cross-coupled transistors, which form a positive feedback loop.

4. Experimental results

The delta-sigma modulator has been implemented using a one-poly, four-metal (1P 4M) 0.18-μm standard CMOS process. The chip core size is 1.22 mm^2. The designed modulator operates at a single 3.0 V supply voltage, a Fs of 3.2 MHz, and an *OSR* of 80.

Figure 3 shows the signal-to-noise-plus-distortion ratio (SNDR) as well as SNR, both plotted against the normalized input amplitude. The input frequency used to measure the modulator was 6.25 kHz. In order to effectively measure SNR and SNDR, we increased the input amplitude by 20 dB steps from −100 dB to −10 dB. Next, we increased the input amplitude by 1 dB

Table 2. Measured result

Specification	Value
Technology	0.18 μm CMOS 1P 4M
Supply	3 V
Core area	1.22 mm^2
Power dissipation	5.6 mW
Sampling frequency	3.2 MHz
Number of orders	4
Signal bandwidth	20 kHz
Peak SNDR	88.7 dB
Peak SNR	96.9 dB
Dynamic range	99 dB

Table 3. A comparison of *FOM*

Architecture	BW (kHz)	DR (dB)	VDD (V)	P (mW)	FOM (dB)
ΔΣ: 2 (32-b) SC [4]	20	102	3.3	70.4	156.5
ΔΣ: 2 (4-b) Hybrid [5]	20	102	3.3	37.3	159.3
ΔΣ: 2 (4-b) Hybrid [6]	20	106	3.3	18	166.5
ΔΣ: 3 (1-b) SC [7]	25	88	1	0.95	162
ΔΣ: 2 (1.5-b) - 2 (1-b) SC [8]	24	82	0.6	1	155.8
ΔΣ: 4 (1-b) SC [This work]	20	99	3	5.6	164.5

steps from −10 dB to 0 dB in order to obtain more detailed data.

Table 2 summarizes the measured performance of the chip. The *DR* is 99 dB in the 20-kHz bandwidth. The peak-SNR reaches 96.9 dB while the peak-SNDR reaches 88.7 dB. Total power consumption of the modulator is 5.6 mW.

FOM of a delta-sigma modulator is defined as [2]:

$$FOM = DR_{dB} + 10\log\left(\frac{Signal\ bandwidth}{Power}\right) \quad (3)$$

Our proposed modulator has 164.5-dB *FOM*. Table 3 shows the performance comparison of several designs for state-of-the-art switched-capacitor delta-sigma modulators with the same bandwidth.

5. Conclusion

A single-bit 4^{th}-order delta-sigma modulator for a 20-kHz bandwidth has been implemented. We obtained a 99-dB maximum *DR* from the proposed modulator with a loop filter composed of both feedback and feed-forward paths. The design is suitable for both audio codec and distributed sensor applications.

The modulator is fabricated in a 0.18-μm CMOS 1P 4M process, and consumes approximately 5.6 mW from a 3.0 V supply voltage. The performance has been achieved through proper system design, which involves optimizing topology parameters, modeling circuit non-idealities, and suitably scaling the overall system.

Compared to the other delta-sigma modulators listed in Table 3, our modulator achieves a good *FOM*, which indicates that both power and performance are well optimized.

6. Acknowledgement

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7. References

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